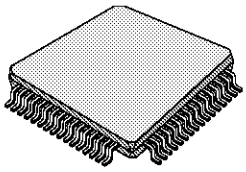
SGS-THOMSON MICROELECTRONICS

L6237

5V SPINDLE MOTOR DRIVER

PRODUCT PREVIEW

- OPERATES FROM 5V SUPPLY
- 1.5A MAXIMUM START-UP CURRENT
- INTEGRATED PHASES COMMUTATION SEQUENCER
- PROGRAMMABLE SLEW RATE
- BACK EMF COMPARATOR OUTPUT
- BRAKE FUNCTION INPUT WITH USER CONFIGURABLE DELAY
- LOW POWER CONSUMPTION MODE
- OVER TEMPERATURE PROTECTION

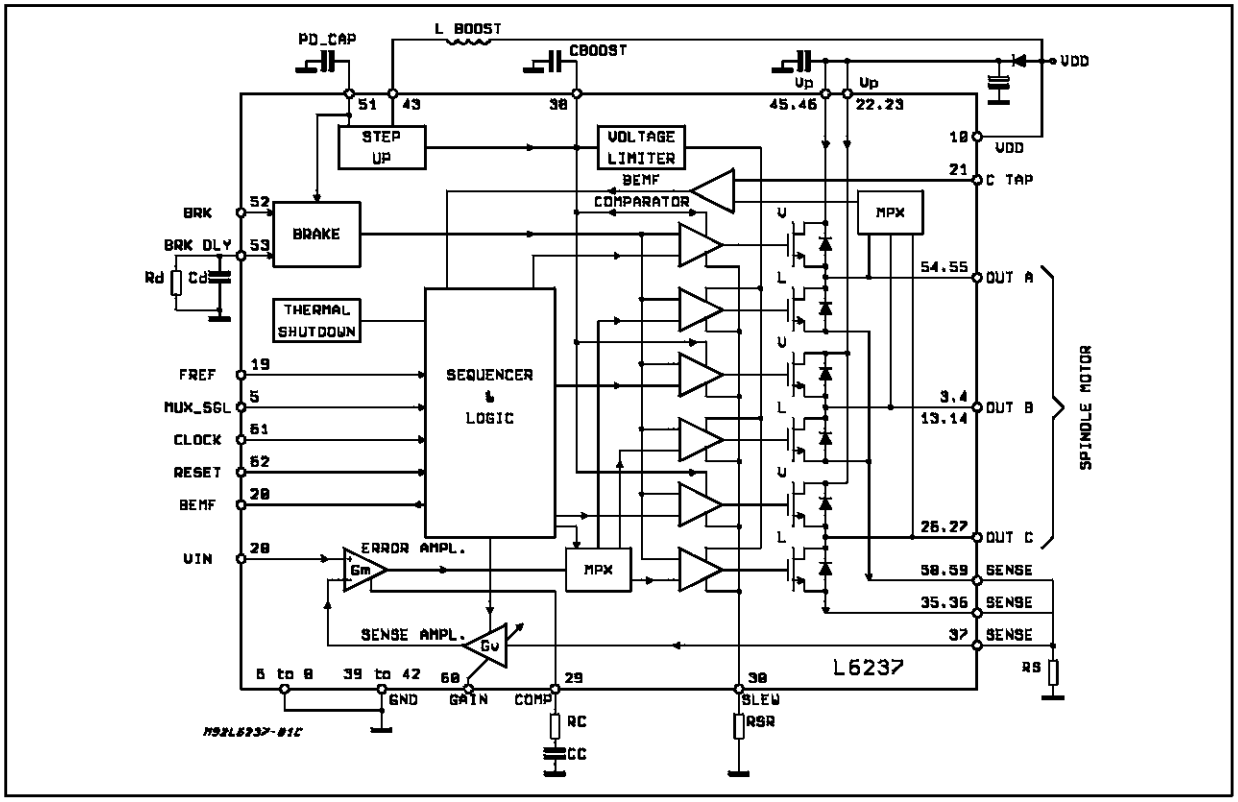


TQFP64L

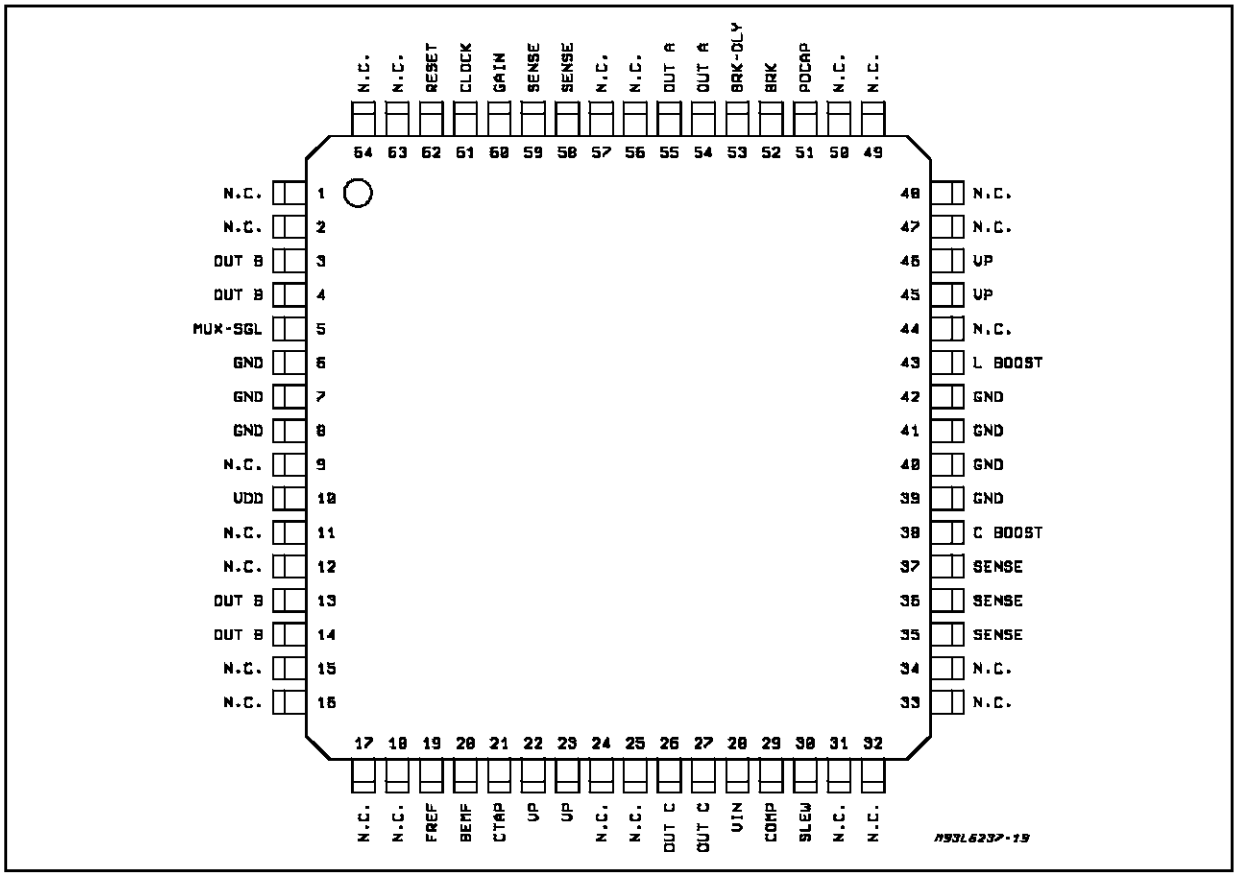
DESCRIPTION

The L6237 is a Triple Half bridge Driver intended for use in brushless DC motor applications. The device is designed to drive a Three Phase, Brushless DC Motor, Typically used in Rigid Disk Drives. Power drivers are fabricated in DMOS Technology and feature Fast Internal Recirculation Diodes. All logic inputs are CMOS/TTL compatible, and an internal Transconductance Loop is included for linear motor speed control. Upper N-Channel DMOS Transistors are driven via an Internal Step-Up Converter. The IC will be manufactured in a plastic TQFP64 surface mount package.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DS(sus)}$	Output Sustaining Voltage	14	V
V_P	Supply Voltage	7	V
V_I	Logic Input Voltage Range	-0.3 to V_P	V
V_{IN}	Transconductance Loop Input Voltage Range	-0.3 to VP	V
I_{PEAK}	Peak Current (Pulsed: T_{ON} = 5ms; D.C. = 10%) Tj = 25°C	2.0	A
T_{jmax}	Maximum Junction Temperature	145	°C
I_{max}	Maximum Current (D.C.)	1.2	A
Ptot	Total Power Dissipation at T_{amb} = 70°C	0.85	W
T_{amb}	Operating Ambient Temperature	-0 to 70	ÉC
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-Ambient (*)	90	°C/W

(*) Mounted on board with minimized copper area.

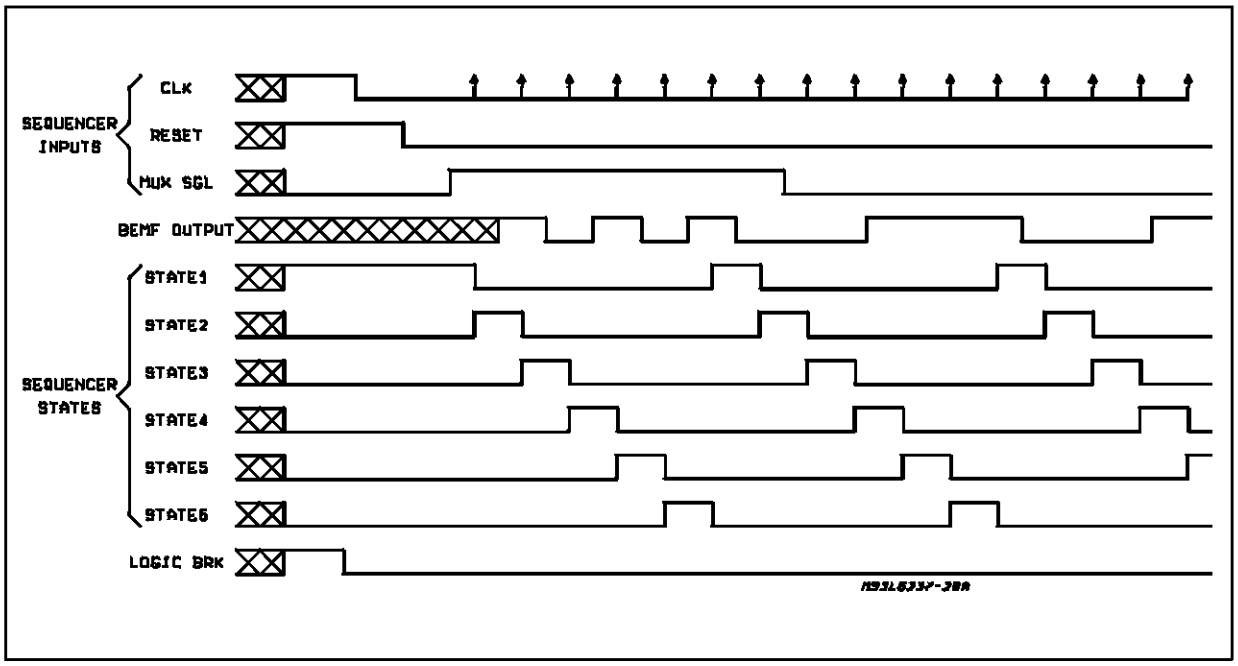
PIN FUNCTIONS

N.	Name	Function
1, 2, 9, 11, 12, 15, 16, 17, 18, 24, 25, 31, 32, 33, 34, 44, 47, 48, 49, 50, 56, 57, 63, 64	N.C.	Not Connected.
3, 4, 13, 14	OUT B	The outputs of the three DMOS half bridge drivers.
26, 27	OUT C	
54, 55	OUT A	
5	MUX_SGL	Logic input used to configure BEMF output to be multiplexed (high) or a single output (low).
6, 7, 8, 39, 40, 41, 42	GND	Ground.
10	V_{DD}	Power supply for internal circuitry. 5V power supply must be connected directly to pin.
19	FREF	Used as time reference for internal period and mask counters.
20	BEMF	Output for BEMF comparator.
21	CTAP	Input for center tap of motor.
22, 23, 45, 46	VP	5V power supply for the DMOS drivers. Series Schottky diode may be used in applications where BEMF voltage must be used for head parking.
28	V_{IN}	Input for motor current control voltage.
29	COMP	A capacitor and resistor are connected to this pin for external compensation of the transconductance loop.
30	SLEW	Input for connection of a resistor for configuration of the output slew rate during commutation.
35, 36, 37, 58, 59	SENSE	Pin for connection of RSENSE, an external resistor used to sense the motor current
38	CBOOST	Pin for connection of capacitor to ground for the internal step up converter.
43	LBOOST	Pin for connection of inductor to V_{DD} for the internal step up converter.
51	PD_CAP	External capacitor to ground which stores energy for use during braking.
52	BRK	Active LOW logic input that turns off all drivers, and triggers the delayed brake.
53	BRK_DLY	Pin for connection of external RC network to configure delay of braking.
60	GAIN	Logic input to configure the gain in the current sense feedback loop (K). Low state produces gain of 4, high state produces a gain of 16.
61	CLOCK	Rising edge triggered input used to increment the commutation sequencer.
62	RESET	Logic input used in conjunction with CLOCK. For CLOCK = Low and RESET = high the sequencer is forced to state 1. For CLOCK = high and RESET = high an immediate BRAKE is initiated. An immediate BRAKE implies no delay.

ELECTRICAL CHARACTERISTICS (V_P = 5V; Tamb = 25°C; unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_P	Power Supply voltage		4.5	5	5.5	V
I_P	Supply Current	Drivers off brake = high brake = low			8 1	mA mA
I_{DSX}	Output leakage Current				1	mA
$R_{DS(ON)}$	Sink Output ON Resistance	T_j = 125°C			0.75	Ω
	Source Output ON Resistance				0.75	Ω
$V_{DS(SAT)}$	Source Saturation Voltage	I_{DS} = 1A T_j = 125°C			0.75	V
	Sink Saturation Voltage				0.75	V
V_F	Body Diode Forward Drop	I_{DS} = 1A			1.3	V
t_{PRK}	Maximum Brake Delay Time	BRK → 0V or V_P → 0V; C_{PDCAP} = 4.7µF; R_{DSON} ≤ 4Ω			0.3	s
t_{BRK}	Maximum Brake Time				4	s
I_{er}	Error Amplifier Input Bias Current				1	µA
V_{EAR}	Error Amp. Input Linear Range		0		4	V
K	Sense Amplifier Gain	Gain = Low Gain = High		4 16		V/V
	Sense Amp. Input Bias Current				1	µA
V_{SAR}	Sense Amp. Input Linear Range	Gain = Low Gain = High	0 0		1 0.25	V V
V_{CLO}	Current Loop Total Offset Voltage				TBD	mV
V_{INH}	Logic Input Voltage		2			V
V_{INL}					0.8	V
I_{INH}	Logic Input Current	V_{IN} = 5V			1	µA
I_{INL}		V_{IN} = 0V			1	µA
t_{don1}	Upper/Lower Turn-on Delay	Upper		TBD		µs
t_{don2}		Lower		TBD		µs
t_{doff1}	Upper/Lower Turn-off Delay	Upper		TBD		µs
t_{doff2}		Lower		TBD		µs
T_{sd}	Shutdown Temperature			160		°C
T_{sdr}	Recovery Temperature			120		°C
C_{BOOST}	Step-up Converter Storage Capacitor		1			µF
L_{BOOST}	Step-up Converter Charging Inductor			220		µH
dv/dt	DMOS Output Turn-off Slew rate	R_{SLEW} = 100K		150		mV/µs
I_{OMAX}	BEMF Output Source/Sink Current	V_{DROP} = 0.4V	±0.36			mA
T_{INC}	Min. Clock Pulse width to Increment Sequencer	V_{DD} = 5V	500			ns
F_{CLK}	Max. Sequencer Clock Frequency (50% D.C.)	V_{DD} = 5V			1	MHz
R_{CT}	Value of "Y" Connected Center Tap Resistors			20		KΩ
F_{REF}	Max. FREF Clock Frequency (50% D.C.)	V_{DD} = 5V			10	MHz

Figure 1: Sequencer Timing Diagram.



SEQUENCER STATES				SEQUENCER TRUTH TABLE				
	OUTA	OUTB	OUTC	CLK	RESET	MUX_SGL	OPERATING MODE	
STATE1	I+	I-	0	X	0	0	Single BEMF	Drivers Enabled
STATE2	I+	0	I-	X	0	1	MUX BEMF	
STATE3	0	I+	I-	0	1	0	Initialize Sequencer	
STATE4	I-	I+	0	X	1	1	Tri-State, MUX BEMF	
STATE5	I-	0	I+	1	1	0	Logic Brake, Initialize Seq.	
STATE6	0	I-	I+	X = DON'T CARE ↑ Indicates not level sensitive, increments sequencer on positive edge				
LOGIC BRK (SEQ->STATE1)	I-	I-	I-					

I+: Upper On, I-: Lower On, 0: Tri-State

SPINDLE DRIVE FUNCTIONAL DESCRIPTION

The commutation is accomplished via three logic inputs (CLOCK, RESET, MUX_SGL). A positive transition at the clock input will increment the internal sequencer producing commutation to the next phase (refer to logic truth table for explanation of sequencer operations).

The L6237 performs internal sensing of the Back Electromotive Force (BEMF), giving a CMOS compatible logic output signal that is high or low if the current BEMF voltage is respectively above or below the central tap voltage. For application in which the center tap is not connectable to the relative input pin, three resistors are internally available from outputs in a "Y" configuration to simulate the presence of the center tap. The BEMF comparator input is internally switched to the output phase that is in tristate condition, while the output is selectable via the MUX_SGL input. When MUX mode is selected the BEMF output will track the current floating phase, as determined by the sequencer state. When SGL mode is active, only the C output BEMF is provided.

The L6237 performs an adaptive digital mask to block unwanted zero crossing generated during phases commutation. This mask is activated when a positive CLOCK transition increments the sequencer, and remains active for a period that is one fourth of the period between two zero crossing. Considering that a full increment of the sequencer (one "electrical" revolution) gives 6 different output states, the period between two commutation can be considered of 60 electrical degrees, so that the masking time is 15 electrical degrees. An input clock signal FREF is requireed as a time base for the internal mask counters.

The BRK and BRK_DLY inputs offer flexibility to the system designer in the implementation of the braking function. The BRK input, when pulled low, turns off all upper and lower DMOS drivers. This

way the outputs are in tristate condition, and since no brake is applied to the motor, it will continue its rotation, giving a BEMF voltage proportional to its speed. The low transition at BRK input will also produce a delayed negative transition at the BRK_DLY input. This delay is configurable by connecting a capacitor and resistor from the BRK_DLY pin to ground. The negative transition at this pin will initiate the braking of the motor by turning on all lower DMOS, keeping all upper DMOS turned off. This feature provides a time interval where the motor acts as a generator, whose BEMF can be used to power the Read/Write Parking function. As soon as the head has been parked, the motor can be really braked, stopping its rotation in a very short time. The brake function utilizes the energy stored in an external capacitor to turn on or off the DMOS powers. This allows the braking procedure even if the Vp supply has been powered down. Additionally, while in brake mode, part of the analog circuitry is turned off and the quiescent current is minimized. This is useful in battery operated sistems when disk access is minimal. An immediate brake can be realized by simultaneously driving RESET and CLOCK high, and MUX_SGL low. This will turn off the upper drivers turning on the lower drivers. Braking occurs regardless of the condition of the BRK_DLY input.

Motor current is determined by a voltage imposed on the VIN input. The SENSE pins are intended for connection of a resistor in series with the source of all lower DMOS. The voltage at this pin provides the feedback signal which is utilized internally to regulate the motor current. This one can be determined by the expression Imotor = Vin/K*Rsense where K is the voltage gain of the sense amplifier. A value of 4 or 16 is selectable by the GAIN logic input. The current is regulated by a linear transconductance loop which drives the lower DMOS. The control is passed to each lower DMOS in succession during the commutation sequence.

To avoid recirculation of the current flowing in the coils of the motor when each phase is commutated, the turn off slew rate of the upper an lower drivers is externally configurable using a single resitor. This defines a current that is internally used to discharge a capacitor. The profile of the voltage across this capacitor will be reproduced at the output, performing the slew rate control. Because of this control the current flowing in the switched off coil will decrease to zero with a quadratic slope, while the total current in the motor is kept constant by the transconductance loop.

Thermal protection circuitry will shut off all drivers when the chip junction temperature exceeds the threshold temperature. A small amount of hysteresis is included to prevent rapid on/off cycling of the power stages.

CIRCUIT OPERATION AND FORMULAS

BRAKE DELAY

The amount of time that a signal transition takes to propagate from BRK to BRK_DLY pins can be determined by the espression

$$Td \cong 1.5 \cdot RC \quad [ms]$$

where R and C are the values of the resistor an capacitor connected to BRK_DLY pin. With the above expression the value of Td is expressed in milliseconds.

TRANSCONDUCTANCE LOOP GAIN

The transconductance is given by the expression:

$$Gm = 1/(K \cdot Rsense)$$

Where K can be 4 or 16 depending on the state of pin GAIN. If GAIN=0, K=4; if GAIN=1, K=16. As a result the total current flowing in the motor is:

$$Im = Gm \cdot Vin = Vin/(K \cdot Rsense)$$

where Vin is the voltage applied to pin V_{IN}.

SLEW RATE CONTROL

By means of an external resistor it is possible to configure the turn off slew rate following this expression:

$$SR = 15/Rslew(K\Omega) \quad [V/\mu s]$$

Rslew is the resistor connected to pin SLEW and its value is espressed in Kohms, while the SR value will be V/µs.

DIGITAL BEMF MASKING: THEORY OF OPERATION

A 9 bit up counter is used to measure the period between to successive zero crossings. This "period counter" counts a frequency that is FREF/2E6 = FREF/64. When a new zero crossing is detected, the period counter will transfer its contents to the 6 bit down counter that is the real "mask counter".

The up counter will then reset to zero and commence the counting of the following period. Since that the mask counter uses a frequency that is FREF/2E7 = FREF/128, that is half of the frequency used by the up counter, the final masking time will be one fourth of the period between to successive zero crossings or, in other terms, 15 electrical degrees.

During start up, when the period is quite large, the period counter will saturate when all bit are in "1" state, providing a maximum mask interval. As the motor speed increases, a fixed masking time will be applied until the period between two commutations is less than the maximum time of the period counter.

This means that the masking time will be proportional for commutations period that are less than

2E9/(FREF/64).
There are three parameters that are affected by the choice of FREF:

1)Maximum masking time, Tmax, that can be calculated as:

Tmax = 2E6/(FREF/128) = 2E13/FREF

2)Minimum time resolution of the mask counter, that is 1 bit or:

Tres = 128/FREF

3)Truncation error, Et, coming from the approssimation caused by the division by 4, that will typically generate non integer numbers, whose decimals will be skipped. This error is again one bit (with the period of the frequency used by the down counter) or:

Et = 128/FREF

As a result of the above the maximum error of the masking time can be up to:

Emax = Tres + Et = 256/FREF

Please note that the truncation error is not fixed, but depends from the period count and can also be null if the count between two zero crossings can be exactly divided by 4.

As an example, we can consider the case of an 8pole, three phases motor rotating at 5400 rpm. Let consider FREF = 8MHz.

8 poles → 4 electrical cycles for each mechanical revolution

and

3 phases → 6 commutations for each electrical cycle

therefore:

Commutation Frequency = 5400 rev/min * 1min/60seconds * 24comm/rev = 2160Hz.

This means that the commutation period is about 463 microseconds. Considering the above expression we will have:

Tmax = 2E13/8E6 = 1.024ms

This means that the masking time will be proportional starting from a commutation period lower than 4Tmax = 4.096ms that means a speed higher than 610 rpm. Additionally we will have:

Tres = 128/FREF = 16µs

Emax = 256/FREF = 32µs

With a commutation period of 463 microseconds, we should have a masking time of 463/4 = 116µs so that we obtain:

Accuracy = 32/116 = 27.6%

This is the maximum error. Considering the real situation and mainly the real truncation error we will have in this particular situation an Emax=20 microseconds so that the accuracy is about 17.3%

Figure 2: Typical Normalized $R_{DS\ (on)}$ vs. Junction Temperature.

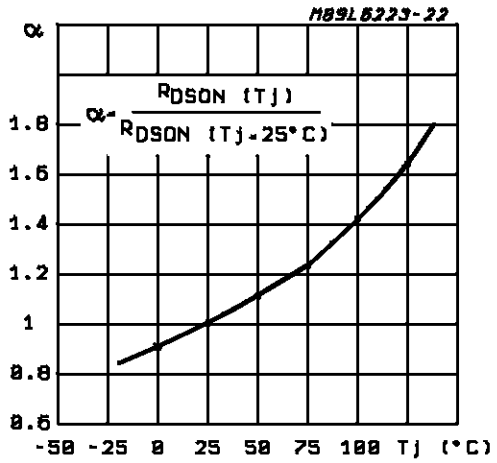
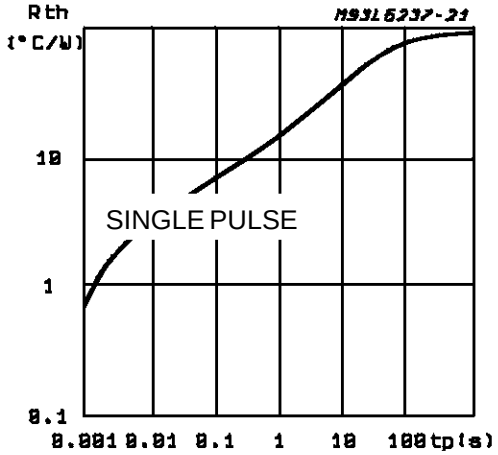


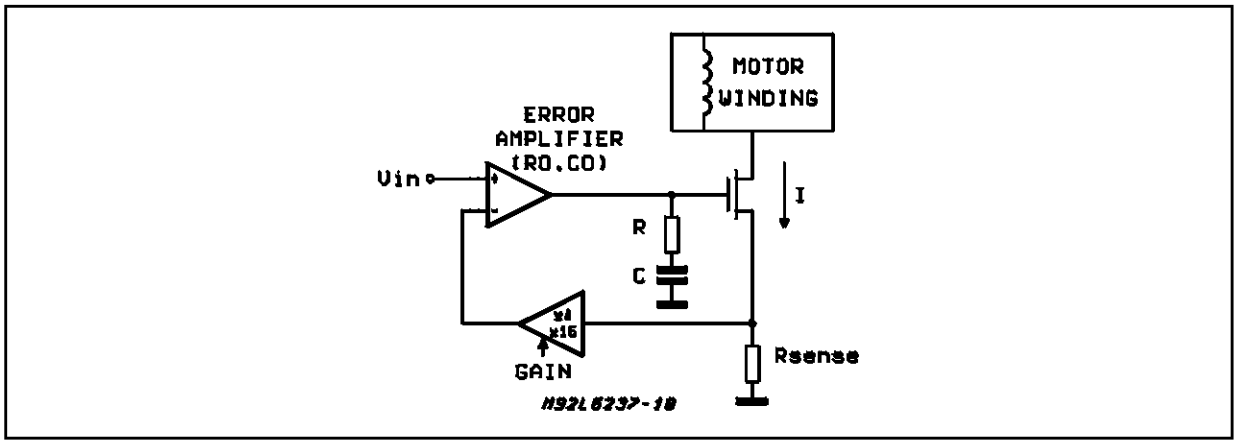
Figure 3: Typical Transient Thermal Impedance vs. Time or Pulse Width



APPLICATION INFORMATION

A typical application configuration of the L6237 driving a three phase brushless sensorless DC motor is shown in Fig.6.
The spindle motor typically is a 2.5" Rigid Disk Driver having 1.3Ω - 0.1mH per phase, star connected.
This kind of load requires a suitable compensation of the linear control loop that can be achieved by an RC network of 10K and 10nF, connected to the "COMP" pin.
Changing the motor characteristics, the RC network could be modified for the best performances of the system.
This is a suggestion about how to choose the value of the RC compensation network of the current loop: the following figure shows the entire control system of the current regulator. The error amplifier is a transconductance amplifier. It is used in open loop configuration inside the main control loop and its gain and frequency

Figure 4.



response are determined by a compensation network connected between its output and ground. This OTA has a large bandwidth (300KHz) and so its pole does not interfere with the pole and zero of the Motor + Power Mos system and of the compensation network. In the application the RC network gives an high system gain at low frequency to ensure good precision and a low gain at high frequency to ensure stability of the system. The figure 5 shows the Bode plot of the compensated error amplifier plus power stage and motor.

The RC value of the compensating network must be choosen to have for high frequencies a flat gain of about 20dB so that the double pole of the motor makes the Bode diagram change its slope and decrease with 40dB/decade stabilizing the whole system cutting the bandwidth. An empiric way to find good RC value for compensation network can be the follow:

1)set a great value of C in order to not interfere at high frequencies

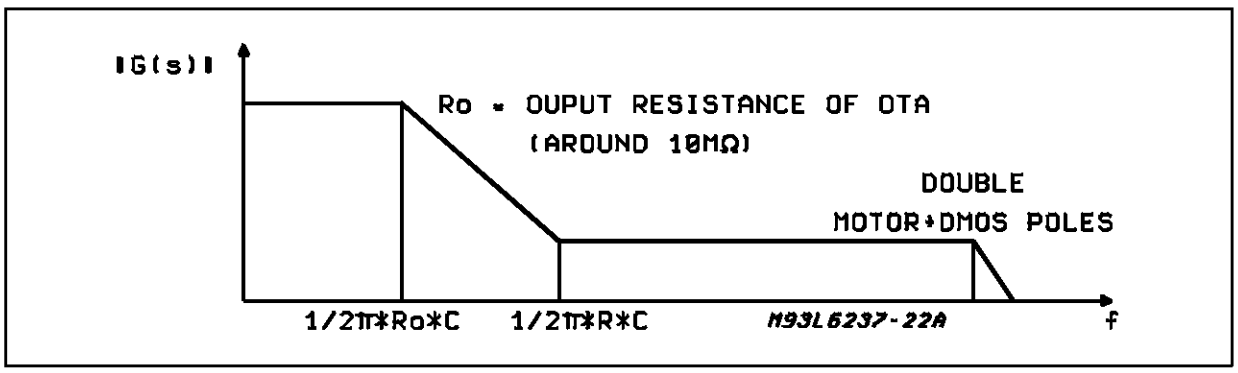
2)give, with motor completely stopped, an excitation as voltage step and act on R in order to get an acceptable current overshoot

3)decrease the value of C until to have a good gain at low frequencies.

To drive the upper DMOS a voltage higher than the power supply Vp is needed. The step-up integrated in the L6237 keeps the CBOOST storage capacitor at the correct voltage.
The switching of the internal step-up circuit can create some noise that could disturb the current control loop. In order to minimize the interference between the step-up circuit and the linear control loop of the output current is suggested to choose an LBOOST of 220µH with an equivalent series resistor minimum of 2Ω.
Another way to decoupling the noise effects of the step-up from the linear control loop is taking care in the PC BOARD design about the GROUND path.
The charging current of the inductor, for the internal step-up converter, flowing through the pin LBOOST (43) is coming out from the device at GND pin 42.
A good solution is to keep separate in the PC BOARD the GND track connection of this pin (42) from the other GND pins (6,7,8,40,41).

Pin 37 of the device is the input of the internal sense amplifier (see Fig. 4).
The voltage at this pin provides the feedback signal which is internally used to regulate the motorurrent.
In order to have no differences in regulated cur-

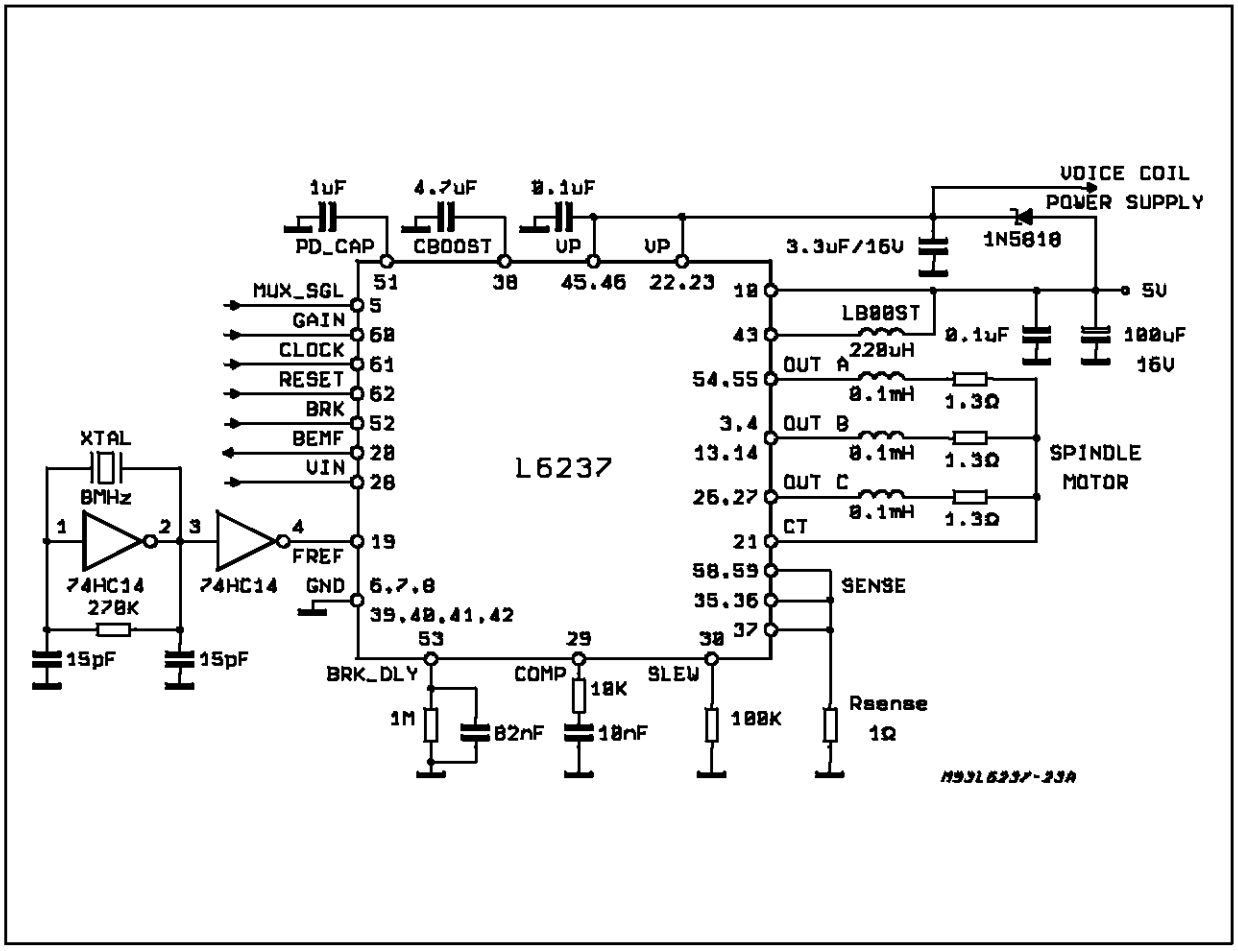
Figure 5.



rent level of the three phase currents, is suggested to connect the sense resistor using two differents tracks: one for the connection of the sources of the output DMOS (pins 35, 36, 58, 59) and another one for the sense amplifier input (pin 37).

The typical application of the L6237 is in HDD systems where there is the need to park the Read-Write Heads before the motor braking.
At power supply switch-off the BRK input is driven low (Active Low), so the power output stage is switched in a high impedance state. The schottky diode 1N5818 insulates the L6237 from the main power supply. The spindle motor now, acting as a three-phase alternator, supplies the Heads voice-coil motor through integrated diodes that rectifie the EMFvoltage. After a delay longer than the parking time, the lower output DMOS can be switched-on and the spindle motor is braked.

Figure 6: Application Circuits



TQFP64 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.85			0.073
A1			0.25			0.010
A2	1.30	1.40	1.50	0.051	0.055	0.059
B	0.18	0.23	0.28	0.007	0.009	0.011
C	0.12	0.16	0.20	0.0047	0.0063	0.0079
D			12.60			0.496
D1		10.00			0.394	
D3		7.50			0.295	
e		0.50			0.0197	
E			12.60			0.496
E1		10.00			0.394	
E3		7.50			0.295	
L	0.40	0.50	0.60	0.0157	0.0197	0.0236
L1			1.30			0.052
K	0°(min.), 5°(max.)