SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

HIGH EFFICIENCY DOUBLE DC-DC CONVERTER WITH L4985

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The growing use of portable equipments supplied by rechargeable batteries requests the implementation of power supplies able to operate with high efficiency at low voltages, as well as to perform the so-called "power management".
The L4985 IC is an integrated solution to meet these requirements and which, in addition, puts an auxiliary converter at the designer's disposal.
This note describes how the device operates, giving also useful information about its use in applications.

1) DEVICE DESCRIPTION

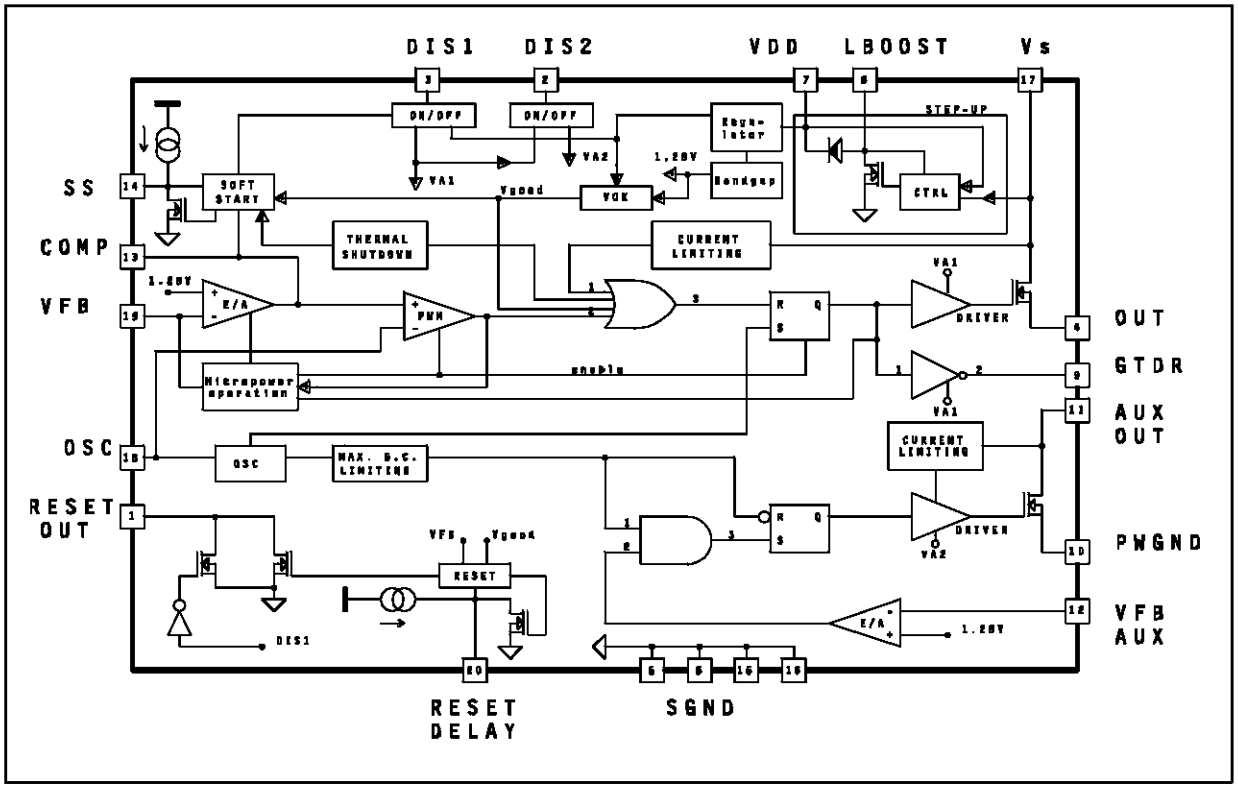
The L4985 is realized in BCD Multipower technology and, thanks to its low internal power dissipation, is delivered in plastic dual in line packages, Powerdip 20 with 60°C/W $R_{th\ j\text{-}amb}$ for standard assemblies and SO20L with 80°C/W $R_{th\ j\text{-}amb}$ for SMD assemblies.

As shown in fig. 1, where the internal block diagram is depicted, the IC includes power stages and control circuitries of two DC-DC converters. The first one (the "main" converter) is a step-down in buck topology. The second one (the "auxiliary" converter) can be a simple boost converter or use a topology with transformer.

The IC operates starting from 4.5V up to 22V and, to allow such low input voltages, is provided with a low power internal boost converter.

The "power management" is performed by means of two inputs which allow partial or total device disabling: either the auxiliary converter only or the whole chip ("sleep mode" operation) can be shut down.

Figure 1: Block Diagram



The L4985 IC characteristics are:

- MAIN CONVERTER
  Input voltage (IC supply voltage) from 4.5 to 22V.
  Output voltage from 1.28V up to a maximum of 18V.
  Maximum output DC current up to 3A (internally limited to 4.2A.)
  Micropower operation for high efficiency at low current.
  Synchronous rectifier driver.
  Usual facilities such as soft-start function, reset function and thermal shutdown.
  Fixed frequency/voltage mode PWM with duty cycle up to 100%.

- AUXILIARY SECTION
  50V / 1Ω NDMOS as a power switch.
  Switch peak current up to 1.5A.
  Hysteretic operation clocked by the same oscillator of the main converter.

The pin functions and descriptions are briefly summarized in the following table:

PIN FUNCTIONS

N.	Name	Description
1	RESET OUT	Open drain output: a low level indicates the drop of the main converter output voltage by a certain percentage or that the L4985 is disabled (see pin 3). A high level means all is working properly. Ref. Sec. 2.1.7
2	DIS2	TTL compatible input: a low level (below 0.9 V) disables the auxiliary converter only; a high level (above 3 V) enables it. Ref. Sec. 2.4
3	DIS1	TTL compatible input: a low level (below 0.9 V) disables the whole device ("sleep mode"); a high level (above 3 V) enables it. Ref. Sec. 2.4
4	OUT	Output: source of the DMOS of the main converter. This pin is connected to the cathode of the free-wheeling diode and to one end of the output filter inductor. If synchronous rectification is used, the drain of the external power NMOS must be tied to this pin. Ref. Sec. 2.1
5, 6 15, 16	SGND	Signal ground: these pins must be connected all together and to the negative lead of the output capacitor. These pins are dissipative, thus a copper area on the board can be effectively used as a heatsink.
7	VDD	Output: internal step-up regulated voltage, typically 10 V above supply voltage. A buffer capacitor must be connected to this pin. Ref. Sec. 2.3
8	LBOOST	Internal step-up switch drain: the step-up coil is connected between this pin and the supply. Ref. Sec. 2.3
9	GTDR	Output: gate driver for an external MOSFET performing synchronous rectification. If not used, this pin must be left floating. Ref. Sec. 2.1.5
10	PWGND	Power ground: this is the ground of the internal step-up and the auxiliary converter and should be connected to the output capacitor separately from SGND.
11	AUXOUT	Output: drain of the DMOS of the auxiliary converter. Using flyback topology, a lead of the primary winding of the coupling transformer is connected to this pin; using boost topology, the coil and the anode of the diode are connected. Ref. Sec. 2.2
12	VFBAUX	Input: feedback signal of the auxiliary converter. This pin is connected to the output divider that fixes the output voltage. Ref. Sec. 2.2
13	COMP	Output: E/A output, available for frequency compensation (connected between this pin and pin 19).Ref. Sec. 2.1.3
14	SS	Input: soft start timing. A capacitor connected between this pin and SGND fixes the soft start time. Ref. Sec 2.1.6
17	VS	Input: supply voltage. A buffer capacitor and a filter capacitor must be connected as close as possible to this pin.
18	OSC	Input: switching frequency setting. A capacitor connected between this pin and SGND fixes the operating frequency of the IC. Ref. Sec. 2.1.2
19	VFB	Input: feedback signal of the main converter. It is connected to the output directly if a 1.28V output voltage is requested or through a divider for greater values. The compensation network is connected between this pin and pin 13 (COMP). Ref. Sec 2.1.3
20	RESET DELAY	Input: reset timing. A capacitor connected to this pin and to SGND fixes the lasting of a low level on pin 1 after the disappearence of a fault condition for the main converter. Ref. Sec. 2.1.7

2) SYSTEM DESCRIPTION

2.1 MAIN CONVERTER

2.1.1 Buck Topology Review.

Buck topology is the most widely used in step-down converters.

As shown in fig. 2, a switch interrupts the line current and provides a pulsed voltage to the output LC filter. The dc voltage appearing at the ends of the capacitor depends on the width of the pulses applied to the filter, since the amplitude is fixed. For this topology, "continuous mode" operation (i.e. the inductor current is never zero) is recommended in order to reduce the stress of the output capacitor and of the free-wheeling diode.

The output voltage is usually controlled with PWM technique. The L4985 uses the so-called "voltage mode" control (also known as "direct duty cycle control"), in which a fixed frequency/fixed amplitude sawtooth is compared to an error signal, thus setting on and off times of the switch.

2.1.2 Oscillator

Referring to fig. 3, we will consider how the oscillator works. At start, the voltage across the external capacitor C_{osc} is zero, the comparator output is low and both MOSs M1 and M2 are off.
A 62µA current generator charges C_{osc}, increasing its voltage linearly till the comparator threshold is reached. Now, this is placed at 2V by the divider formed by the 50kΩ and the 100kΩ resistors. Once the threshold is crossed, the comparator output goes high turning on M2 and lowering the comparator threshold to 1V. After a short delay, introduced by the two inverters, also M1 is turned on and C_{osc} is quickly discharged through it.

When the C_{osc} voltage drops below the 1V threshold, the comparator switches again, turning M2 off and moving the threshold to 2V once more, M1 is turned off and another cycle begins.

Due to the internal delays, the peak and the valley values of the sawtooth thus generated exceed slightly the two threshold values. For example,

Figure 2: Basic Buck Topology

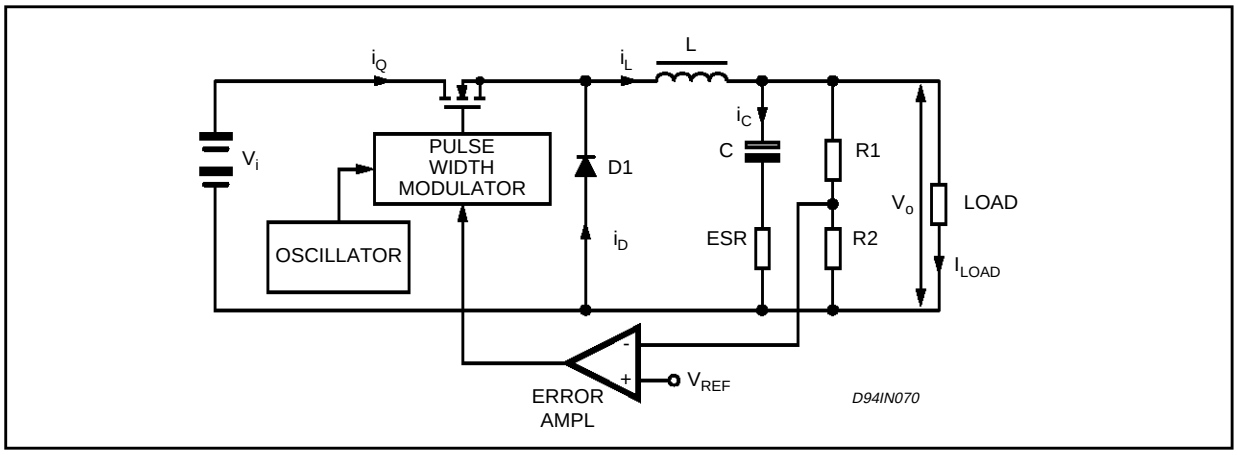
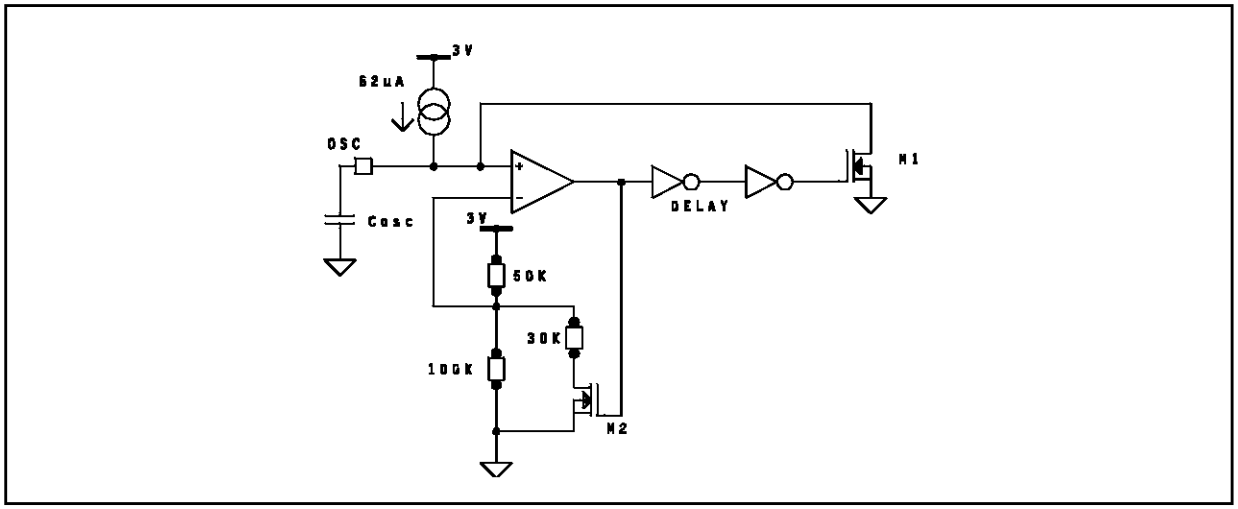


Figure 3: Oscillator Internal Schematic



the waveform swings between 0.7 and 2V at 100kHz.

The oscillator frequency (f_{sw}) is set by the external capacitor C_{osc} according to the approximate formula, valid in the range from 25 kHz to 350 kHz:

$$f_{sw} = 31 - 8 \cdot C_{osc} + \frac{32}{C_{osc}}$$

($[f_{sw}]$=kHz, $[C_{osc}]$= nF)

2.1.3 Error amplifier and compensation network

The error amplifier (E/A) supplies the signal to be compared with the oscillator sawtooth to perform PWM. Its non-inverting input is internally connected to a 1.28 V reference voltage, while its inverting input and the output are externally available for feedback and frequency compensation.

In continuous mode buck converters, controlled in voltage mode PWM, the power section gain has two poles due to the output LC filter, plus a zero due to the ESR of the output capacitor. That requires an E/A compensation network with two poles and two zeroes, like the one shown in fig. 4. The zeroes compensate the double pole of the filter, while one pole compensates the zero of the ESR. The second pole is nominally in the origin, which would arise the gain towards infinity at f=0. Actually, the gain cannot exceed the DC value of the E/A and the pole occurs where the gain intersects this limit, at a very low frequency (see fig. 5).

2.1.4 Current Limiting

Buck topology allows effective handling of overload conditions because of the position of the switch. The schematic of the current limiting block (fig. 6) shows the output NDMOS split in two paralleled transistors (5.35:1 ratio). The drop across

Figure 4: E/A Compensation Network

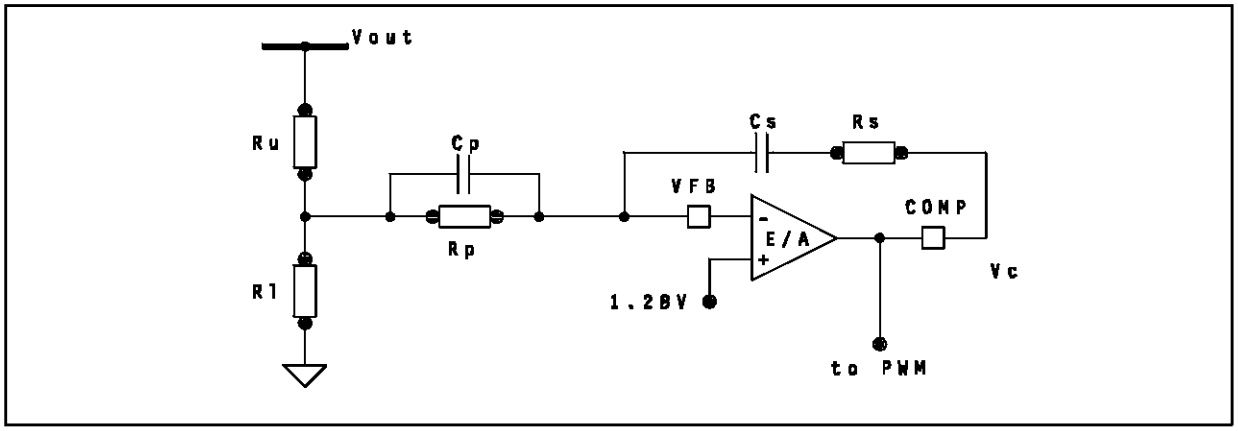


Figure 5: E/A Compensation Network Gain

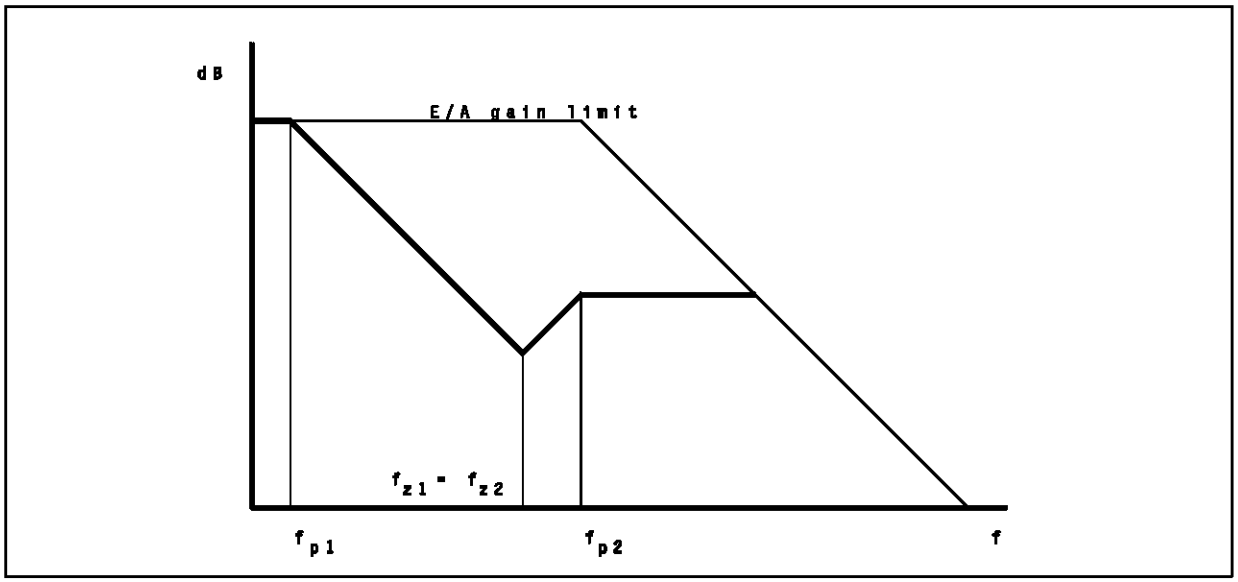


Figure 6: Current Limiting Circuit

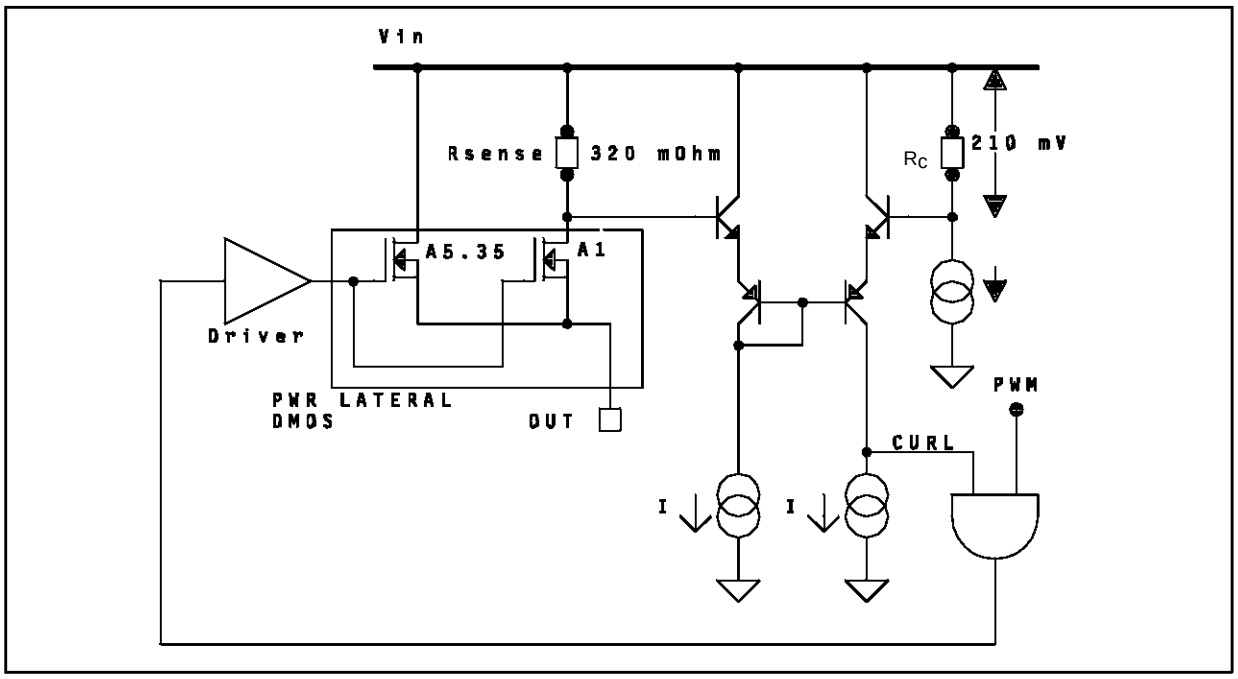
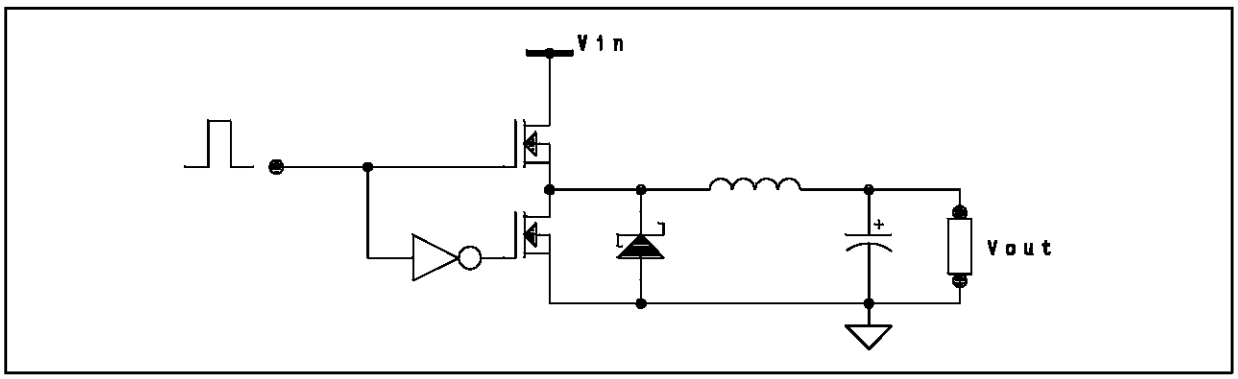


Figure 7: Synchronous Rectification



the 320mΩ R_{sense} is compared to the one on R_c, set at 210mV by a current source.

If the current exceeds the limit value, the drop across R_{sense} will be greater than 210mV, the mirror will be unbalanced so that the CURL point will go low. The AND gate will mask the PWM signal and the output NDMOS will be turned off.

The static limit value is:

$$I_{max} = 6.35\ (210\ mV/320m\Omega) \approx 4.2\ A$$

Owing to internal delays of the circuit (typ. 800 ns), the dynamic value will be slightly higher.

2.1.5 Synchronous Rectifier Driver

To achieve the maximum efficiency at high load current it is possible to resort to synchronous rectification.

This requires an external MOSFET which must be driven in phase opposition to the IC output. The principle schematic and the related waveforms are shown in fig. 7 and 8. Pin 9 is the gate driver for the synchronous rectifier; it can deliver up to 30 nC per cycle with a 10 V voltage, and takes into account the dead-times needed to avoid cross conduction between the two MOSFETs.

The Schottky diode in fig. 7 (smaller than the one we should use if synchronous rectification was not employed) prevents the body diode of the external NMOS from turning on during the dead-times, which would impair efficiency.

2.1.6 Soft-start

Soft-start is essential to assure a correct and safe start-up of step-down converters. It is particularly useful for controllers like L4985 which do not have any limitation on duty cycle.

It avoids inrush current surge to overload the out-

Figure 8: Synchronous Rectifier waveforms

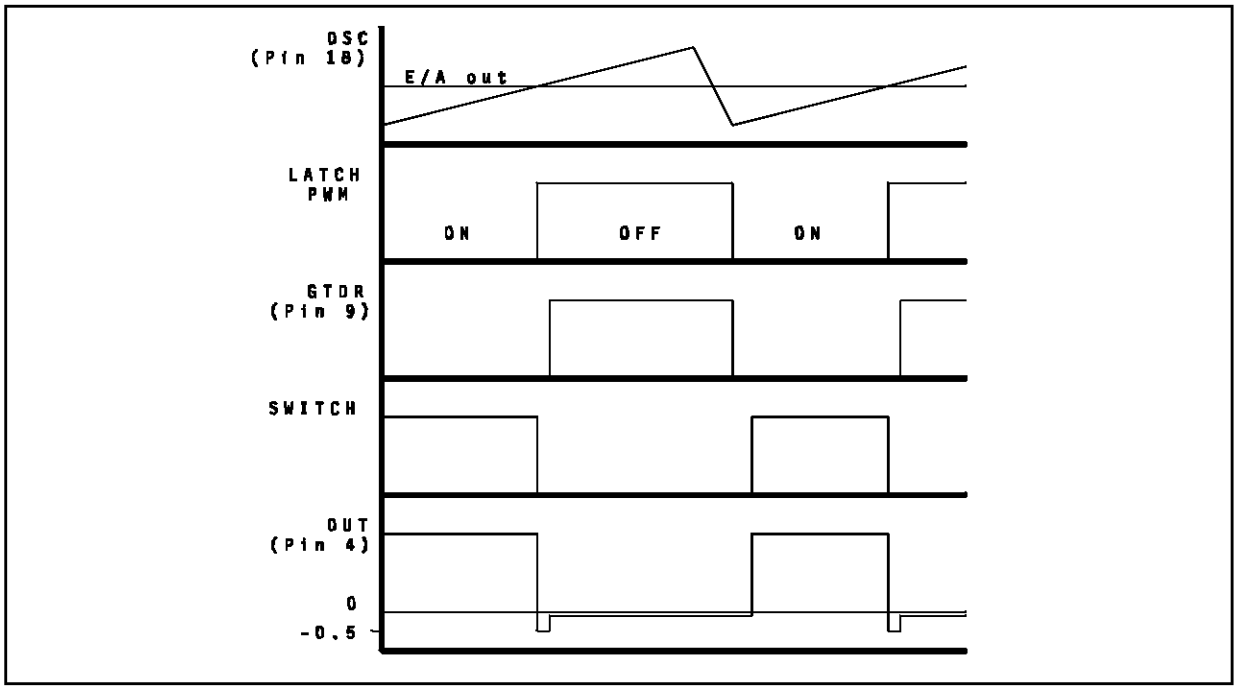
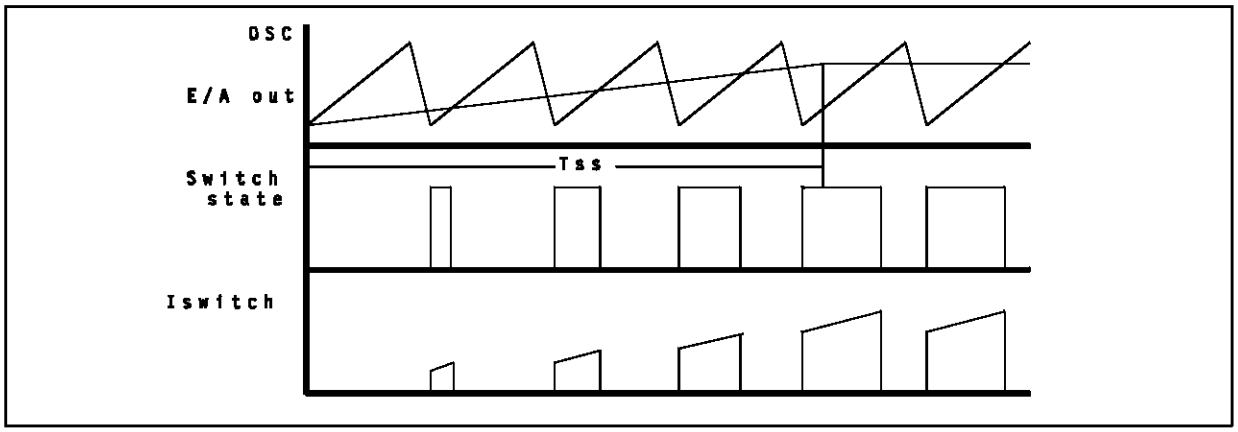


Figure 9: Soft start Waveforms



put power stage and makes the output voltage increase monotonically.

Soft-start is performed by means of an external capacitor, C_{ss}, charged by an internal current generator, which does not allow the E/A output to rise abruptly, thus making duty-cycle increase starting from zero to the correct value (see fig. 9).

Soft-start intervenes at start-up (e.g. after a DIS1 enabling), and after a thermal shutdown.

In case of thermal shutdown, the C_{ss} capacitor will be discharged through MOS M1 (see fig. 10) and a new soft-start cycle will begin as soon as normal operating conditions (see Sec. 2.5) are resumed.

The soft-start time is related to the value of the C_{ss} capacitor according to the rate:

$$T_{ss} \approx 25 \frac{V_{out}}{V_{in}} \text{ ms/}\mu\text{F}$$

2.1.7 Reset & Reset Delay

The Reset function is useful for diagnostic purposes. The signal, delivered at pin 1 with an open drain output (requiring an external pull-up resistor), is normally high but becomes low if the chip is disabled or the feedback voltage falls 160mV below the reference voltage (1.28V) - for more than 2µs, to prevent uncorrect activation by disturbances - so recognizing a drop of the output voltage. To avoid uncertain behaviours in case of output voltage drops, the sensing system is provided with hysteresis.
The high level appears, after a programmable delay, as the chip is enabled or when the feedback

Figure 10: Soft Start Circuit

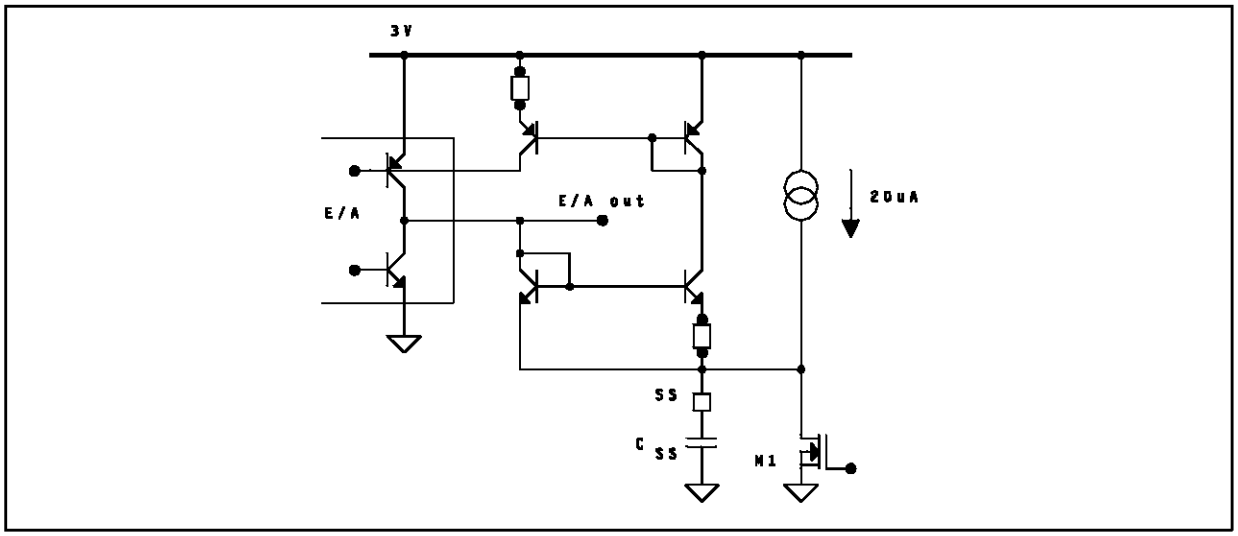
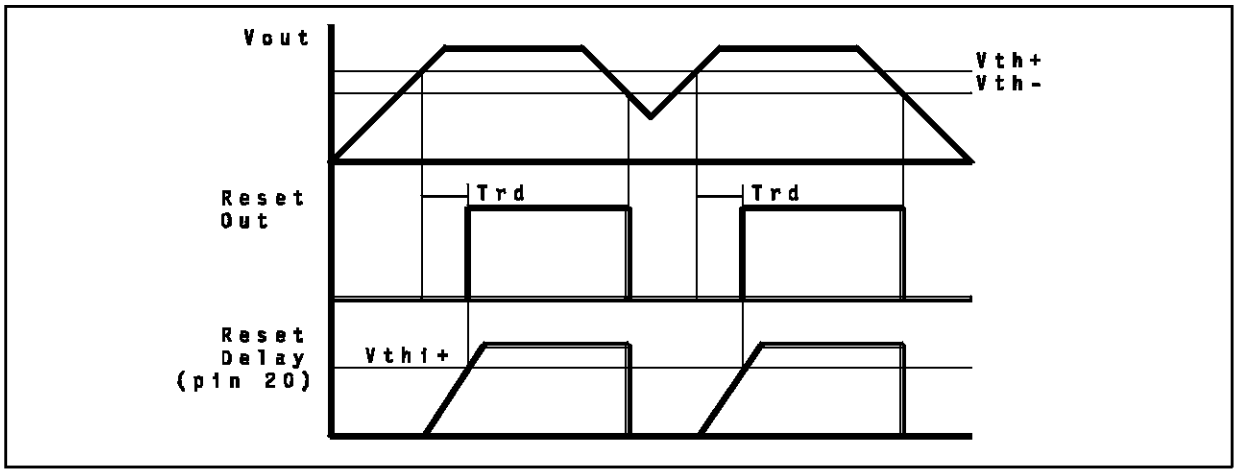


Figure 11: Reset & Reset Delay Waveforms



signal reaches 60 mV below the reference (see fig. 11). The delay is programmed by an external capacitor connected between pin 20 and SGND and the relationship between the capacitance value and the Reset Delay time is:

$$T_{rd} = 250\ ms/\mu F$$

The Reset function could untimely intervene because of undershoots resulting of load transients, without a real fault condition. This should be checked especially if V_{out} is close to V_{in}. For details, look them up in Sec. 3.1.

2.1.8 "Micropower" Operation

At low output power, converters efficiency drops significantly, being the current absorbed by the circuit comparable to the one delivered to the load. To improve efficiency in such a condition, the device has been provided with the "Micropower" operation (µPWR) which reduces the switching consumption, responsible for most of the power losses.

If this operating feature is required in the application, the synchrounous rectification cannot be employed.

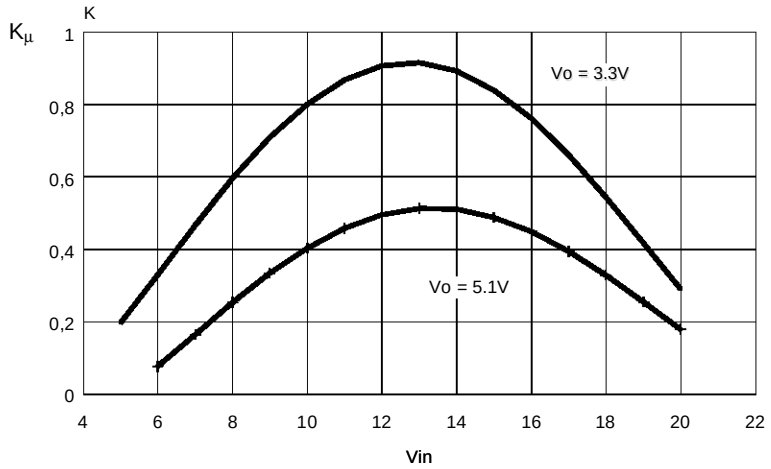
The "light load" condition is detected by comparison of the on time of the power switch, T_{on}, to an internal time reference, T_{ref}, depending (likewise T_{on}) on V_{in}.

Actually, in such a situation, the converter operates in discontinuous mode and, therefore, T_{on} decreases with the load current, even if V_{in} is fixed. If T_{on} stays below T_{ref} for more than 20ms (to assure it is not a transient situation), the µPWR will replace PWM and the switching frequency will be considerably reduced.

When in µPWR, the converter operates in "free-running" mode: the feedback voltage, fed into a capacitor with hysteresis, drives the turn-on and turn-off of the output switch.

Increasing the load current, the off time of the power switch decreases and, as it falls below

Figure 12: K_μ vs. V_{in} @ V_{out}



180μs, the μPWR is left and PWM resumed.
The μPWR activation current, $I_{\mu on}$, can be estimated by the following formula:

$$I_{\mu on} = \frac{K_\mu}{L\, f_{sw}}$$

Where K_μ is a function of the input and the output voltages, as shown in fig. 12. The PWM resumption current, $I_{\mu off}$ can be found with the approximate formula:

$$I_{\mu off} = 80\ C\ V_{in}$$

2.2 AUXILIARY CONVERTER

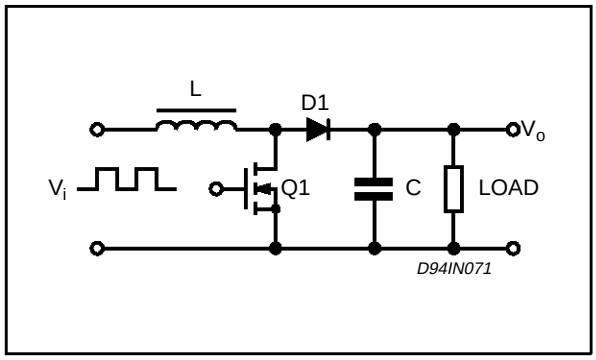
2.2.1 Possible Topologies Overview

The auxiliary section includes, as a power switch, an NDMOS with grounded source and open drain. Therefore, the magnetic load of the switch is to be connected to the supply. This load can be either a coil - this leading to a boost topology - or the primary winding of a transformer, for insulated or multiple outputs topologies.

Boost topology (see fig. 13) is the simplest and suitable for making step-up converters only.

The topologies with transformer coupling (see fig. 14) are more flexible and allow both step-up and step-down converters but, of course, are more complex.

Figure 13: Basic Boost Topology



2.2.2 Circuit operation

The duty cycle control is performed by means of comparators (hysteretic control) and therefore does not need any E/A or frequency compensation. Referring to figg. 15 and 16, we see that the

Figure 14: Basic Topology with Transformer

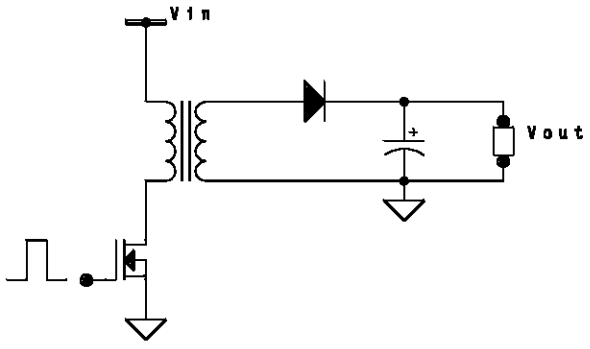


Figure 15: Auxiliary Converter Internal Schematic

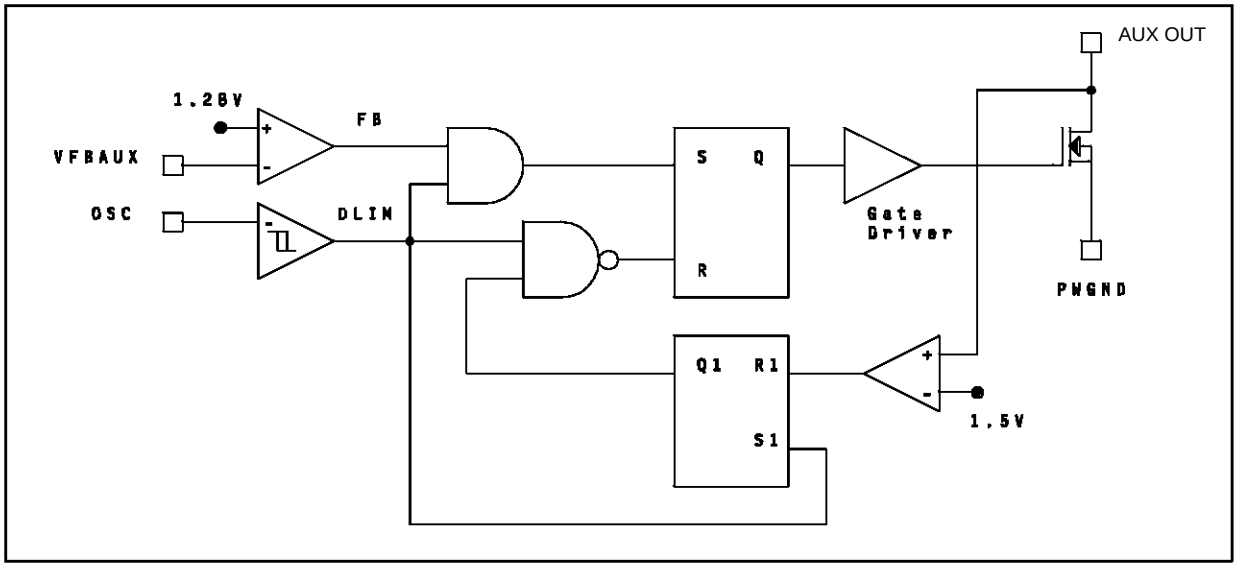
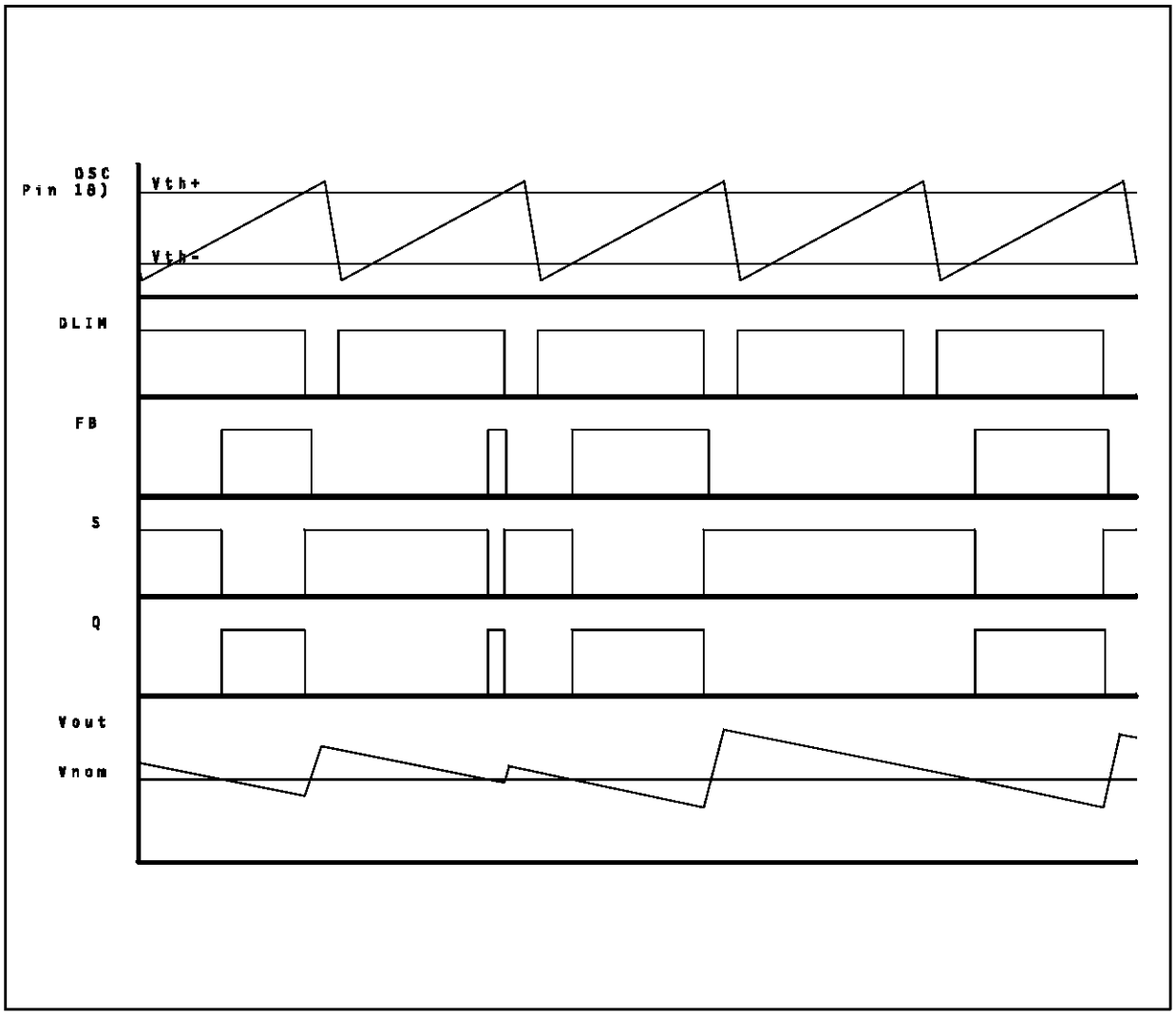


Figure 16: Auxiliary Converter: Principal Waveforms



turn-on of the power switch is imposed by the VFBAUX signal (if it falls below the 1.28V reference), provided that the DLIM signal is high (during the ramp-up of the oscillator). The switch is turned off by DLIM itself, when it goes low at oscillator ramp-down.
During the ON state of the switch the current limiting block senses its voltage drop. If the current rises above the maximum limit (typ. 1.5A), this block will intervene turning off the switch before DLIM does it.
As a consequence of this operation, neither frequency nor duty cycle of the output are constant, there is only a limit on their maximum values.

2.3 INTERNAL STEP-UP AND POWER SUPPLY

The L4985 has been designed to operate at input voltages starting from 4.5 V and, in order to drive effectively the internal switches, an internal voltage as high as 10 V is needed. Besides, to drive the output NDMOS of the main converter, a voltage 10V above the input voltage is required.
An internal low power step-up (boost) converter, requiring only a coil and a capacitor as external components, is used to meet both these requirements.
The converter works at a variable frequency in discontinuous mode and can deliver few mA for external use.

The architecture of the internal buses is shown in fig. 17. The line V3 supplies the low voltage logic circuits and the reference generator (bandgap). V11power supplies the drivers of both converters and of the synchronous rectifier, while V11logic is mainly used to supply the level shifters which interface logic and power circuits. The VOK block monitors V3, V11logic and the bandgap voltage, enabling the converters operation if their values are above the respective thresholds (2.5V, 8.5V and 1.19 V).

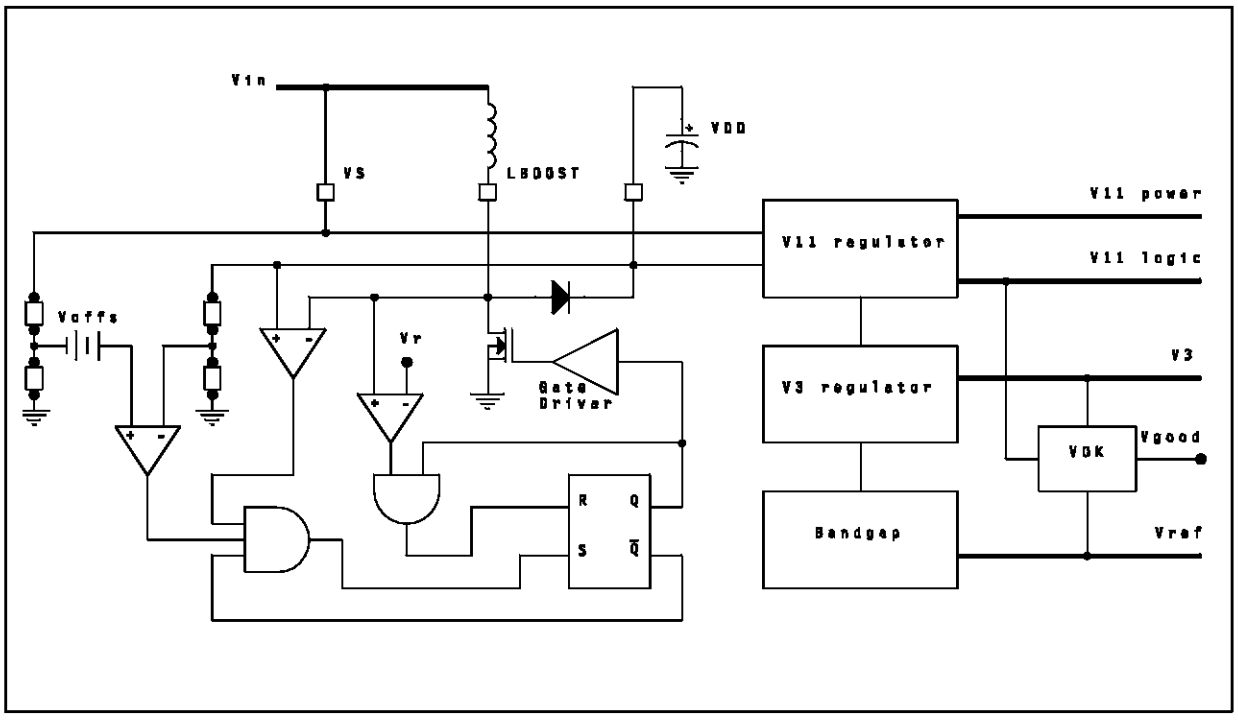
2.4 "SLEEP MODE" OPERATION

The control of the "power management" is performed with pins 2 and 3 which accept TTL-compatible signals.
Pin 3, called DIS1, controls the enabling/disabling of the whole chip. A low level (below 0.9V) disables the chip, putting it in "sleep mode": the internal supply is turned off and the current absorbed from the supply is reduced to few µA.
To enable the chip operation, it is necessary to apply a voltage above 3V.
Pin 2, called DIS2, works like DIS1 but controls the auxiliary converter only. Of course, DIS2 works only if DIS1 is high: if the latter is low, the former has no effect.

2.5 THERMAL SHUTDOWN

To protect the device in case of anomalous operation, the IC is provided with a sensing system which monitors continuously the temperature.
If it exceeds T_h°C, the NDMOS of the main converter will be turned off and the soft-start capacitor discharged. The auxiliary section, as well as the internal step-up, will carry on working.
Normal operation will be resumed as soon as the

Figure 17: Internal Step-up and Supply Architecture



chip temperature drops below T_l°C. The two thresholds T_h and T_l, assure a thermal hysteresis of 30°C. The typical value for T_h is 145°C.

3) APPLICATION INFORMATION.

In the following we will deal with three evaluation boards we have developed, giving also the design criteria for applications.

The target specifications are:

- Application 1: step-down only.
  - Input Voltage Range :4.5 to 22V
  - Output Voltage: 3.3V
  - Max Output Current: 3A
  - Operating Frequency: 85kHz
  - Maximum p-p Ripple: 30mV

- Application 2: step-down only.
  - Input Voltage Range: 6 to 22V
  - Output Voltage: 5.1V
  - Max Output Current: 3A
  - Operating Frequency: 85kHz
  - Maximum p-p Ripple: 50mV

- Application 3: double converter.
  - Step-down section as Appl. 2
  - Step-up section
    - Output Voltage: 24V
    - Output Current: 200mA
    - Maximum p-p Ripple: 240mV

3.1 STEP-DOWN DESIGN

The procedure starts dimensioning the devices involved in power handling: the Output Filter, the Free-wheeling Diode and the Input Capacitor. Then it proceeds with the small signal part.

Inductor selection

The first step is to select a minimum inductance value so that the inductor current ripple never exceeds a maximum value ΔI_{lmax}, in order to assure continuous mode operation. If the minimum load current Ioutmin is stated, then:

$$\Delta I_{lmax} = 2I_{outmin}$$

if not, a good criterium is to choice ΔI_{lmax} = 25 to 30% of the maximum output current I_{outmax}.

The maximum ripple occurs when the off time of the switch is maximum, that is at minimum duty cycle:

$$D_{min} = \frac{V_{out} + V_f}{V_{inmax} + V_f - V_{dson}}$$

$$T_{offmax} = \frac{1 - D_{min}}{f_{sw}}$$

where: V_f, voltage drop on the recirculation element (free-wheeling diode or synchronous rectifier);

V_{dson}, drop across the output NDMOS;

f_{sw}, switching frequency;

The minimum inductance value will be:

$$L_{min} = \frac{(V_{out} + V_f)T_{offmax}}{\Delta I_{lmax}}$$

In the above applications, since a synchronous rectifier is used, we assumed V_f = 0.2V. V_{dson} was neglected.

Appl. 1: Lmin = 39µH;
selected value: L = 45µH

Appl. 2+3: Lmin = 47.5µH;
selected value: L = 50µH

Once a value for L has been chosen (L > L_{min}), the next step is how to make the inductor.
As for the material, the requirement of high efficiency will orient the selection towards ferrite, Molypermalloy or Kool Mµ.

Concerning the geometry, toroids, E cores, pot cores and many others are at designer's disposal. The specific application, with its requirements concerning cost, performances, encumbrance, etc., will orient the designer towards one solution instead of another. For the inductor sizing procedure (core size selection, winding design, etc.), make reference to handbooks.
In the applications, Molypermalloy toroids were used for simplicity reasons. The characteristics of the coils are:

Appl. 1: Core Magnetics 55120/58120;
Winding: 24 turns ϕ 0.9 mm

Appl. 2+3 : Core Magnetics 55120/58120;
Winding: 27 turns ϕ 0.8 mm

Output Capacitor selection

The capacitor selection criterium is based on output voltage ripple requirements.

The current flowing through the capacitor has a triangular waveform (with zero average value) which makes a voltage ripple appear at its ends. This voltage ripple has a capacitive component, usually negligible, and a resistive one due to ESR.
With the previously selected inductance value (L) the current ripple will be:

$$\Delta I_l = \frac{(V_{out} + V_f)T_{offmax}}{L}$$

if V_r is the maximum voltage ripple, the maximum ESR allowed for the output capacitor is then:

$$ESR_x = \frac{V_r}{\Delta I_l}.$$

A capacitor with an ESR ≤ ESR_x will be chosen.
Usually, once the ESR requirement has been met, the capacitance value C far exceeds the minimum amount imposed by the capacitive ripple. In fact, this is given by:

$$V_c = \frac{\Delta I_l}{8\ C\ f_{sw}}$$

and, even if not being much smaller than the ESR component, it does not affect the total ripple very much (e.g, even if V_c is 40% of ESR • ΔI_l, the total ripple will increase less than 8%).
More often, the minimum amount of capacitance is imposed by other considerations. For instance, in case of large load variations, too a small capacitance produces a poor dynamic behaviour of the output voltage.
Moreover, the L4985 implements the Reset Function and therefore, if this is used, output voltage undershoots resulting of a load increase could trigger it. To avoid this problem, a minimum capacitance value is required:

$$C_{min} = \frac{K_c\ L\ \Delta I_{out}^2}{V_{out}\,(V_{inmin} - V_{out})}$$

where: ΔI_{out} is the maximum load variation;
K_c is a coefficient, depending also on the compensation network (assume K_c = 2).

It goes without saying that there is the possibility to parallele multiple capacitors in order to meet the requirements.

In all applications here described the OS-CON series by SANYO was employed because these capacitors have the minimum ESR for their size.

Appl. 1: ESR_x = 35mΩ;
selected: 2x220 µF/10V OS-CON

Appl. 2+3: ESR_x = 53mΩ;
selected: 220µF/10V OS-CON

The ESR of the 220µF / 10V OS-CON capacitor is 35mΩ.

Free-Wheeling Diode

Owing to their lower forward drop (0.5V), Schottky diodes are preferred to p-n diodes in low voltage applications.

In buck converters the diode must withstand an average current:

$$I_{dmax} = I_{outmax}\ (1 - D_{min})$$

However, if overload conditions must be taken into account, the IC maximum current I4 should be considered in the above formula, instead of I_{outmax}.

The reverse blocking voltage must be greater than the maximum input voltage (add 25% of safe margin), thus standard values from 20 to 40V can be suitable. With synchronous rectification, the Schottky diode is still used but its rated current may be significantly reduced. In such a case, the selection criterium is to have a forward drop less than 0.7V at I = I_{outmax} in order to avoid the body diode of the external NMOS turns on.

Synchronous rectifier

In our applications synchronous rectification was employed to have maximum efficiency at high currents.
A NMOS with a gate charge Q_g not exceeding 30 nC at V_{gs}=10V must be selected.

To make profitable the use of a synchronous rectifier, its R_{dson} should be as low as possible, with respect to the above constraint.
Referring to the power lost in a Schottky diode:

$$P_{sd(max)} = V_f \bullet I_{dmax} \cong 0.5\ I_{dmax},$$

the power dissipated by the NMOS:

$$P_{nmos(max)} = R_{dson}\ I_{outmax}2\ (1 - D_{min})$$

should be quite less than $P_{sd(max)}$ (say, half or even less).

Of course, R_{dson} is computed at the operating silicon temperature, considering a factor K_{th} which, with a good approximation, is:

$$K_{th} = 1 + 0.005\ (T_j - 25).$$

T_j can be estimated taking into consideration $P_{nmos(max)}$ and the thermal resistance of the package that will be possibly used. In the total balance of losses, also the energy required to drive the NMOS should be taken into account. Each switching cycle, a charge Q_g moves from the input source to ground, resulting in a power request which, at maximum, is:

$$P_{gc} = V_{inmax}\ Q_g\ f_{sw}$$

(assume Q_g = 30 nC for calculations). Thus, it should be:

$$R_{dson} \le \frac{P_{nmos(max)} - P_{gc}}{(1 - D_{min})\ I_{outmax}^2\ K_{th}}$$

From this relationship:

Appl. 1: $P_{nmos(max)}$ = 400mW; $R_{dson} \leq 36m\Omega$
Appl. 2+3:$P_{nmos(max)}$ = 400mW;
$R_{dson} \leq 40m\Omega$

As for voltage and current ratings, what said about the free-wheeling diode is still valid.

These requirements are met by a Si9410DY (R_{dson} = 30mΩ; Q_g = 30nC). As additional Schottky diode we have used a ST BYV 10-40.

Input Capacitor selection

The input capacitor is subject to a pulsed current, the RMS value of which dissipates power in its ESR.

It can be shown that the worst condition occurs at 50% duty cycle and that, in this situation, this RMS value is half of the DC output current.

Therefore the input capacitor, besides having a low ESR to reduce power losses, should be sized for a RMS current as high as half of the maximum output DC current, not to shorten its life significantly.

In this class of applications, due to efficiency and encumbrance reasons, a power loss P_x of about 1 to1.5% of the output power can be considered an acceptable value. Thus:

$$ESR \leq \frac{4\,P_x}{I_{outmax}^2}$$

A good solution was found in Chemicon capacitors (LXF series, 470µF/25V, 62mΩ ESR or 560µF/25V, 52mΩ ESR).

Frequency compensation

The goal of the E/A compensation is to close the control loop (see fig.18) assuring stability and good dynamic performances.

The basic idea is that the overall loop gain should resemble the Bode plot of a simple RC low-pass filter: this is stable and has 90° phase margin.

We will refer to fig. 19 where the equivalent circuit of the compensation network is shown.

The first step is to evaluate the gain of the power stage (PWM modulator + power switch + output filter):

$$G_{pw} = G_{pwo}\,\frac{1+\frac{s}{2\pi f_z}}{1+\frac{s}{2\pi f_o\,Q}+\left(\frac{s}{2\pi f_o}\right)^2}$$

where:

$$G_{pwo}=\frac{V_{in}}{V_s},\quad f_o=\frac{1}{2\pi\sqrt{LC}},\ f_z=\frac{1}{2\pi\ ESR\ C}$$

(Q is trivial for our aim).

V_s is the swing of the PWM sawtooth (assume V_s = 1.3V).
The worst condition is at high input voltages, thus G_{pwo} must be computed at $V_{in} = V_{inmax}$.

The crossover frequency f_c of the overall loop gain should be as high as possible to have optimum dynamic performances. However, there is an upper limit imposed by stability considerations:

$$f_c < \frac{f_{sw}}{2\,\pi\,D_{max}}$$

$$D_{max}=\frac{V_{out}+V_f}{V_{inmin}+V_f-V_{dson}}$$

Figure 18: Control Loop Block Diagram

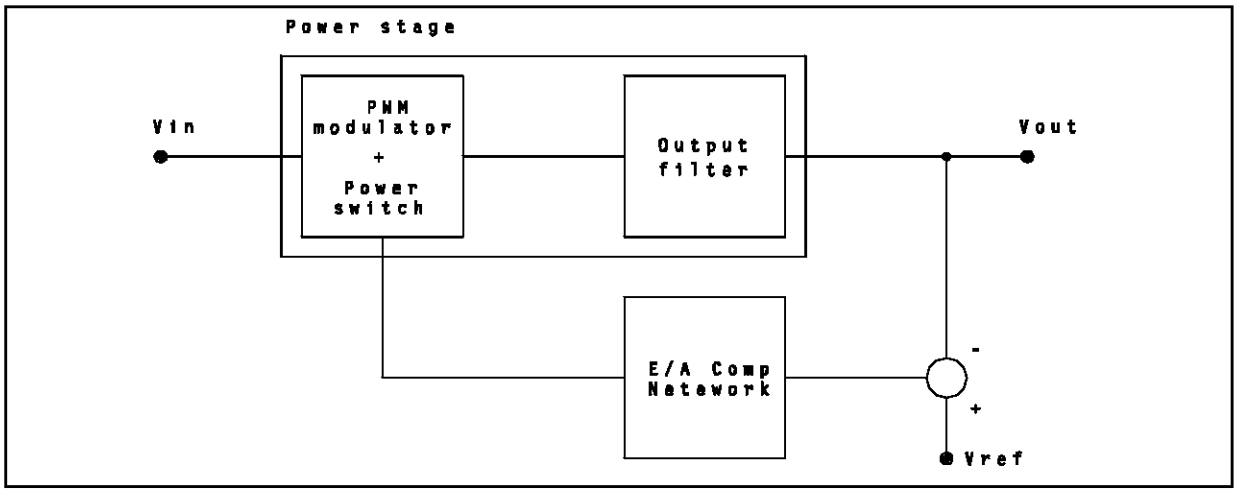
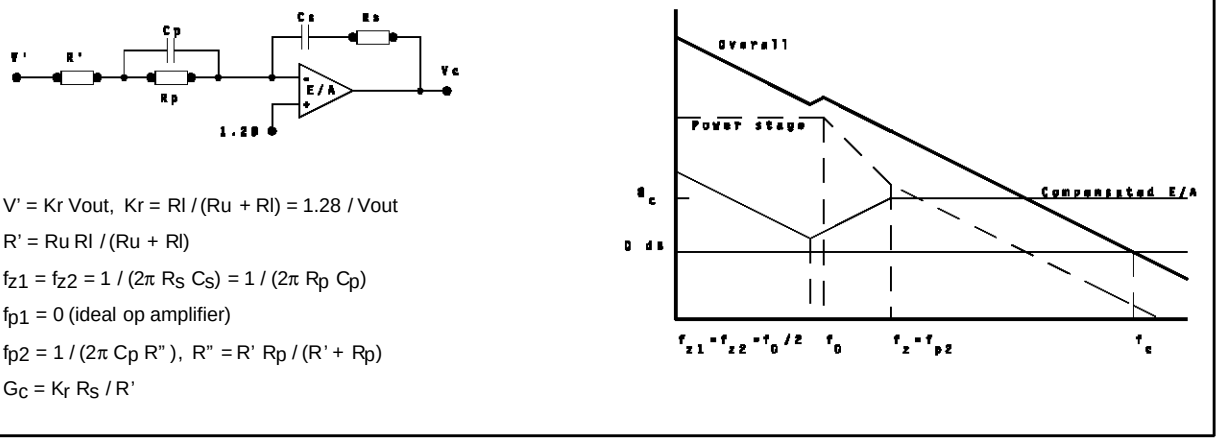


Figure 19: Compensation Network equivalent circuit/design



V' = Kr Vout, Kr = Rl / (Ru + Rl) = 1.28 / Vout

R' = Ru Rl / (Ru + Rl)

$f_{z1} = f_{z2} = 1 / (2\pi R_S C_S) = 1 / (2\pi R_p C_p)$

f_{p1} = 0 (ideal op amplifier)

$f_{p2} = 1 / (2\pi C_p R'')$, $R'' = R' R_p / (R' + R_p)$

$G_C = K_r R_S / R'$

Usually, f_c is chosen 1/10 of f_{sw}, to have a safe margin and reduce the effect of disturbances.

To impose that the crossover frequency is f_c, it is necessary to lift up the Bode plot (around f_c) so that it crosses 0dB axes just at $f = f_c$. With this aim, the high frequency gain of the E/A compensation network should be:

$$G_C = \frac{f_z f_c}{G_{pwo} f_o^2}$$

Now it is possible to select network components, starting with the resistor R_p. Usually it is of some tens of kΩ. This choice does not lead to too high values for C_p, which would slow down the response of the regulation loop during large load transients.

The capacitor C_p is selected so that the first zero of the network is placed at $f = \frac{f_o}{2}$, in order to compensate the abrupt phase change due to the resonance of the output filter:

$$C_p = \frac{1}{\pi f_o R_p}$$

The value R' (Thevenin equivalent of the output divider) is calculated so that the pole of the network is placed at $f = f_z$:

$$R' = \frac{R_p}{\frac{2 f_z}{f_o} - 1}$$

Naming K_r the ratio between reference and output voltages (equal to the output divider ratio):

$$K_r = \frac{1.28}{V_{out}}$$

the resistor R_S, chosen so that the high frequency gain is equal to G_C, will be:

$$R_S = \frac{R' G_C}{K_r}$$

R_S is usually of tens of kΩ. Values below 5kΩ could make the E/A current capability exceeded, thus they must not be accepted.

Now C_S can be calculated in order to place also the second zero at $f = \frac{f_o}{2}$:

$$C_S = \frac{C_p R_p}{R_S}$$

Finally, the upper (R_u) and the lower (R_l) resistor of the output divider can be calculated:

$$R_u = \frac{R'}{K_r}; \quad R_l = \frac{R_u}{\frac{1}{K_r} - 1}$$

In the above procedure, the L4985 E/A is considered as an ideal op-amp. Really, it should be verified that such an assumption is correct. This is practically unnecessary because the op-amp of the L4985 has a low frequency gain and a gain-bandwidth product sufficient to fulfil all practical cases.

Appl. 1: R_p = 56kΩ; C_p = 4.7nF; R_S = 33kΩ; C_S = 8.2 nF; R_u = 3.9kΩ; R_l = 2.4kΩ;

Appl. 2+3: R_p = 56kΩ; C_p = 3.9nF; R_S = 39kΩ; C_S = 5.6 nF; R_u = 8.2kΩ; R_l = 2.7kΩ;

Oscillator capacitor (C_{osc})

As for its value, we remind the relationship between C_{osc} and the oscillator frequency:

$$f_{sw} = 31 - 8 \cdot C_{osc} + \frac{32}{C_{osc}}$$

$$[\,([\,f_{sw}\,] = kHz,\ [\,C_{osc}\,] = nF\,)\,]$$

It is well known that it is desirable to work at fre-

quencies as high as possible, to reduce cost and size of the external output filter, but losses increase with frequency. To optimize that, a value between 80 and 100kHz is suggested. Higher frequencies can be used but at the cost of an efficiency worsening: the designer has to choose a compromise.

The use of a high quality capacitor is advised to predict exactly the frequency value and avoid its drift due to temperature.

In our applications we used a multilayer capacitor. The capacitance value is the suggested one, C_{osc} = 560pF, which leads to a frequency next to 85kHz.

3.2 AUXILIARY CONVERTER DESIGN.

In this section the design of a simple boost converter will be taken into consideration.

Very few external components are needed: the inductor, the output capacitor, the diode and the output divider.

Inductor selection

Referring to Appendix for explanation, a minimum inductance value is needed in order to allow energy transfer from input to the load:

$$L_{min} = (V_{out} - V_{inmin}) \frac{I_{outmax}}{f_{sw}}$$

To make the inductor, the previous considerations about the coil of the main converter are still valid.

Appl. 3: L_{min} = 43µH;
selected value: L = 50µH
Core: Magnetics 55050/58050
Winding: 25 turns, ϕ 0.6mm

Capacitor selection

The capacitor is selected looking at its ESR, in order to limit the ripple of the output voltage. Another parameter to be taken into account is the RMS current ripple rating.

The first step is to calculate the inductor peak current:

$$I_{lp} = 1.5 \sqrt{(V_{out} - V_{inmin}) \frac{I_{outmax}}{L \cdot f_{sw}}}$$

Thus, if V_r is the maximum ripple admitted on the output voltage, it will be:

$$ESR_x = \frac{V_r}{I_{lp}}$$

and a capacitance value C with an ESR lower than ESR_x will be selected. Its RMS current rating should be:

$$I_{rms} = \sqrt{I_{outmax} \frac{2\, I_{lp} - 3\, I_{outmax}}{3}}$$

Finally, you can verify (this is unnecessary in most cases) that the capacitive ripple V_c, which does not exceed:

$$\frac{I_{out}}{C\, f_{sw}}$$

is less than V_r (say, 40% of V_r at maximum). If not, C should be increased.

Appl. 3: ESR_x = 174mΩ;
selected: NCC-LXF 220µF/35V, 84mΩ ESR or 330µF/35V, 62mΩ ESR.

Free-Wheeling diode

The Free-Wheeling diode should be selected for withstanding I_{outmax} as average current and a peak forward current as high as I_{lp}.

The reverse blocking voltage must be greater than the output one (a 25% of safe margin should be added).

The use of a Schottky diode is not mandatory but, with the aim of an optimization of losses, can be taken into consideration. In the application here described, a ST BYV 10-40 was used.

Output divider selection

This divider fixes the output voltage. For its dimensioning, it is possible to choose first a current value I_d, negligible with respect to the load current. Thus, the lower resistor R_l is:

$$R_l = \frac{1.28}{I_d}$$

and the upper resistor is:

$$R_u = \frac{R_l}{\frac{V_{out}}{1.28} - 1}$$

Appl. 3: ($I_d \cong$ 0.5 mA) R_l = 2.7kΩ,
R_u = 47kΩ.

3.3 OTHER COMPONENTS SELECTION.

Internal step-up coil and capacitor

Being part of a low power converter, the coil can be a small size one. Its inductance can lie in the range 100 to 200µH. Few ohms of intrinsic resistance are not harmful, so a small axial or a chip inductor can be used. In all three application an axial inductor of 180µH was used.

As for the capacitor, there is not any particular requirement; a 10µF electrolytic capacitor towards PWGND is just what is needed.

Soft-start and Reset Delay capacitors

For these components, general selection criteria

cannot be given: only the specific situation will guide the designer.

In the application here described small electrolytic capacitors of few µF were used.

Noise filtering and disturbances reduction

It is possible that some points require filtering for high frequency noise reduction, to assure a good operation.

In our applications were used:

1) A film capacitor (0.33µF) placed as close as possible to the supply pin of the IC and connected to SGND;
2) A small film capacitor (22nF) placed between VFBAUX pin and PWGND (for Appl. 3 only).

A RC snubber network across the free-wheeling element of the main converter can be useful to reduce the amplitude of the RF noise. This practical method can be employed to dimension C and R:

a) with the scope, measure the frequency of the ringing (f_r);

b) place a small capacitor directly across the diode, increasing its value until the frequency has been roughly halved;

c) if C is the capacitance value, the damping resistor is:

$$R \approx \frac{1}{2 f_r C}$$

3.4 BOARD LAYOUT CONSIDERATIONS.

To prevent degraded performances or, worse, instabilities and oscillations, a careful board layout is mandatory. With this aim, the following points should be kept in mind.

1) Separate ground paths of signals and load currents for the main converter. The two paths should have their common point in the (-) plate of the output capacitor.
2) Separate the ground path of the auxiliary converter from that of the main converter. The former runs from the (-) plate of its output capacitor to PWGND. The (-) plates of the two output capacitors should be connected.
3) Make separate supply paths for the IC (pin 18), the internal step-up and the auxiliary converter, all leading to the (+) plate of the input capacitor.

Figure 20: PC Board (Component Side) and Components Layout of Appl. 1 and 2 (scale 1:1)

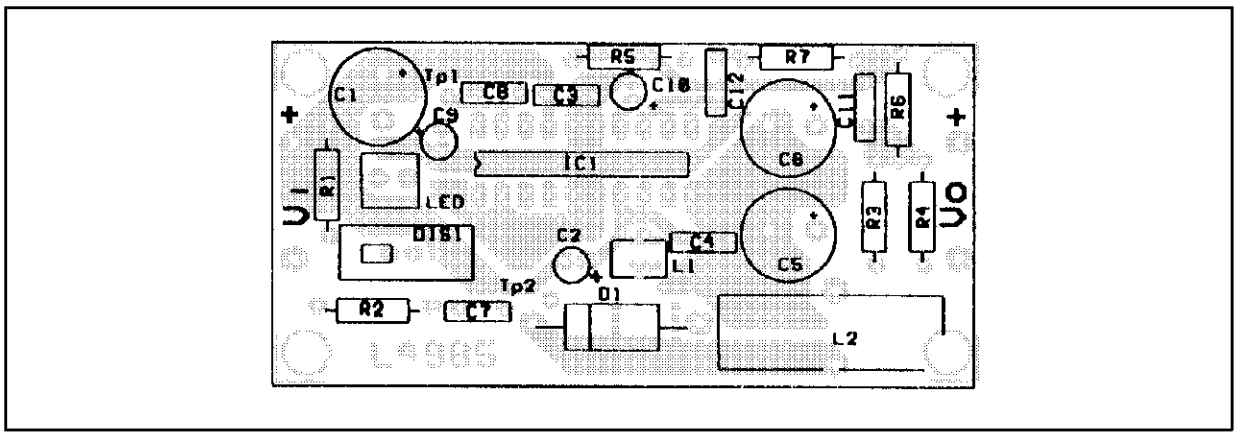


Figure 21: PC Board (Back Side) and Components Layout of Appl. 1 and 2 (scale 1:1)

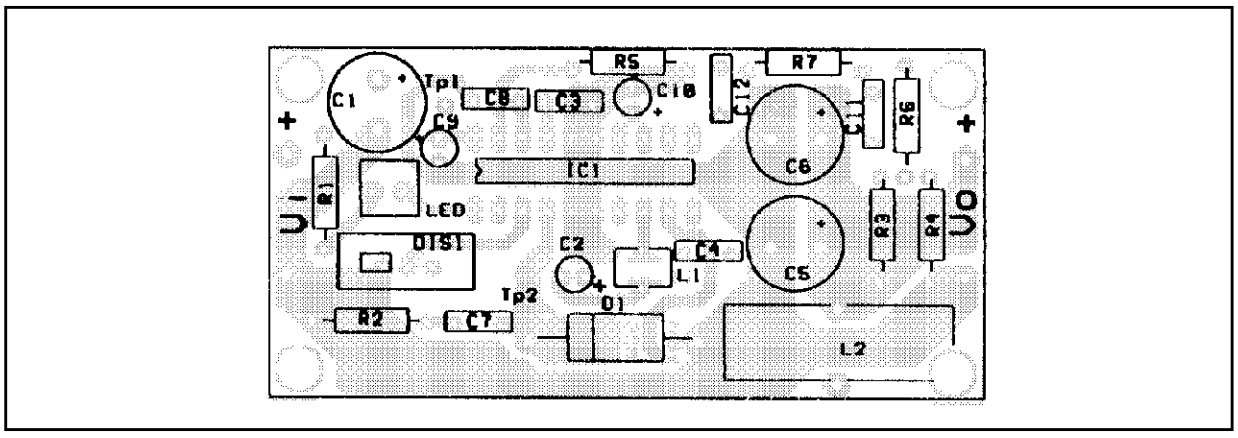


Figure 22: PC Board (Component Side) and Components Layout of Appl. 3 (scale 1:1)

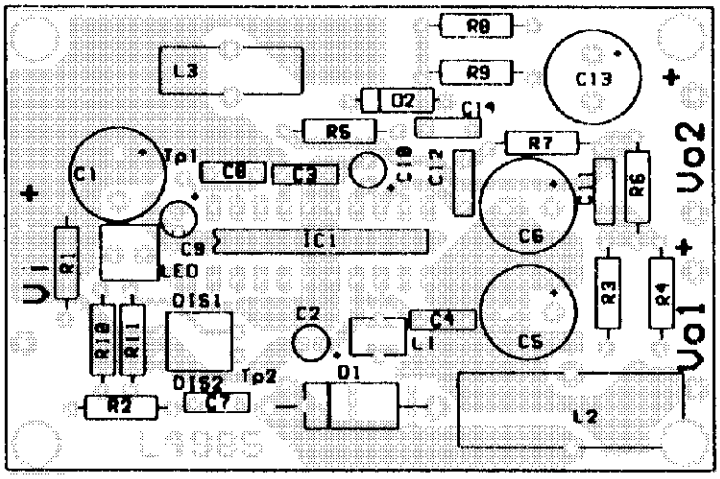
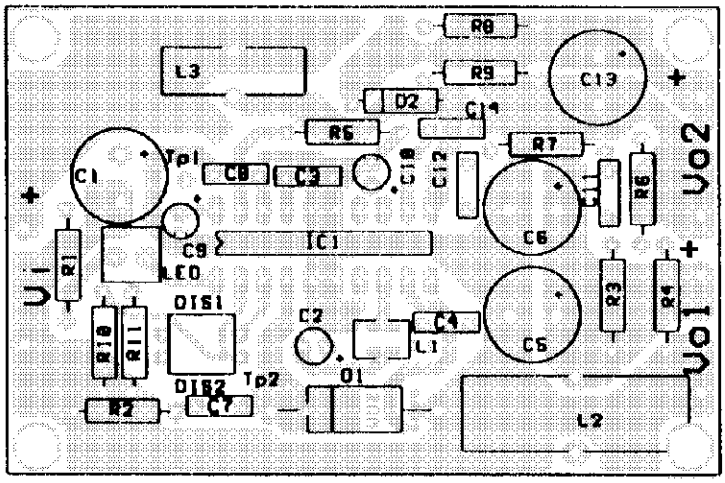


Figure 23: PC Board (Back Side) and Components Layout of Appl. 3 (scale 1:1)



4)The anode of the Schottky diode (the drain of the synchronous rectifier, when used) should be placed as close as possible to pin 4 in order to reduce stray inductance which causes ringing spikes at MOS turn-off.

5)Place the input capacitor as close as possible to the IC so that the input source "draws near".

6)Make copper tracks carrying high currents (either pulsed or DC) as large as possible, in order not to impair efficiency and load regulation. Concerning this, it is important to use copper layers as thick as possible. Some of these tracks could be doubled on the other side of the board.

7)Make copper tracks carrying small signals running far from points with quickly swinging voltages.

8)Widen as much as possible the copper area to which the four central ground pins are connected, in order to make easier heat dissipation. Also ground paths could be widened to form ground planes.

3.5 DEMO-BOARDS

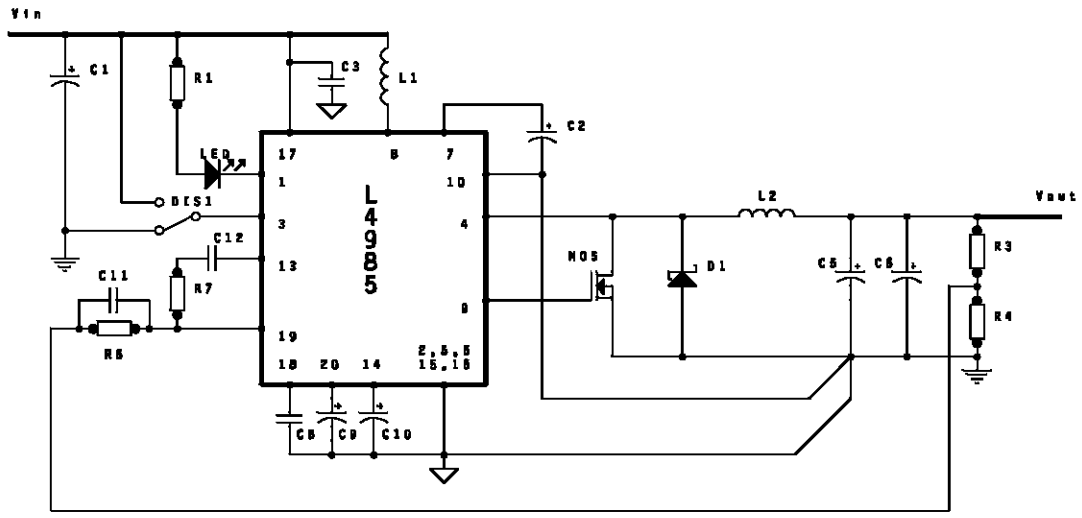
To implement the above depicted applications, two PCBs have been realized. The first one, shown in figg. 20 and 21, allows to use the main

converter only and is employed in applications 1 and 2. The second PCB (see figg. 22 and 23) allows the implementation of both converters and is used in application 3.

To evaluate how the device behaves, the board circuits (with the related parts lists) and some data concerning the evaluation results are presented.

APPLICATION 1: Circuit & part list: see fig. 24

Figure 24: Step Down Converter V_{in} = 4.5 to 22V; V_{out} = 3.3V; I_{out} = 3A



C1 = 470µF / 25V NCC LXF
C2 = 10µF / 50V
C3 = 330nF film
C5 = C6 = 220µF / 10V SANYO OS-CON
C8 = 560pF multilayer
C9 = C10 = 2.2µF / 10V
C11 = 4.7nF
C12 = 8.2nF

R1 = 3.3kΩ
R3 = 3.9kΩ
R4 = 2.4kΩ
R6 = 56kΩ
R7 = 33kΩ

L1 = 180µH axial
L2 = 45µH (Core Magnetics 58120, 24 turns, 0.9mm)

D1 = ST BYV 10 - 40

MOS = DY9410 SILICONIX

Evaluation results:

Symbol	Parameter	Test Condition	Value	Unit
η	Efficiency	V_{in} = 5V; I_{out} = 1A	94.0	%
		V_{in} = 5V; I_{out} = 3A	89.1	%
ΔV_{out}	Line Regulation	V_{in} = 4.5 to 22V; I_{out} = 0.5A	2.0	mV
ΔV_{out}	Load Regulation	V_{in} = 4.5 to 22V; I_{out} = 0.5 to 3A	5.0	mV

Figure 25: Efficiency Diagram

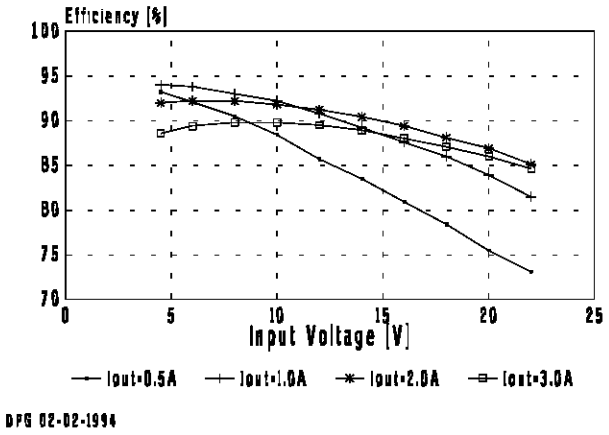
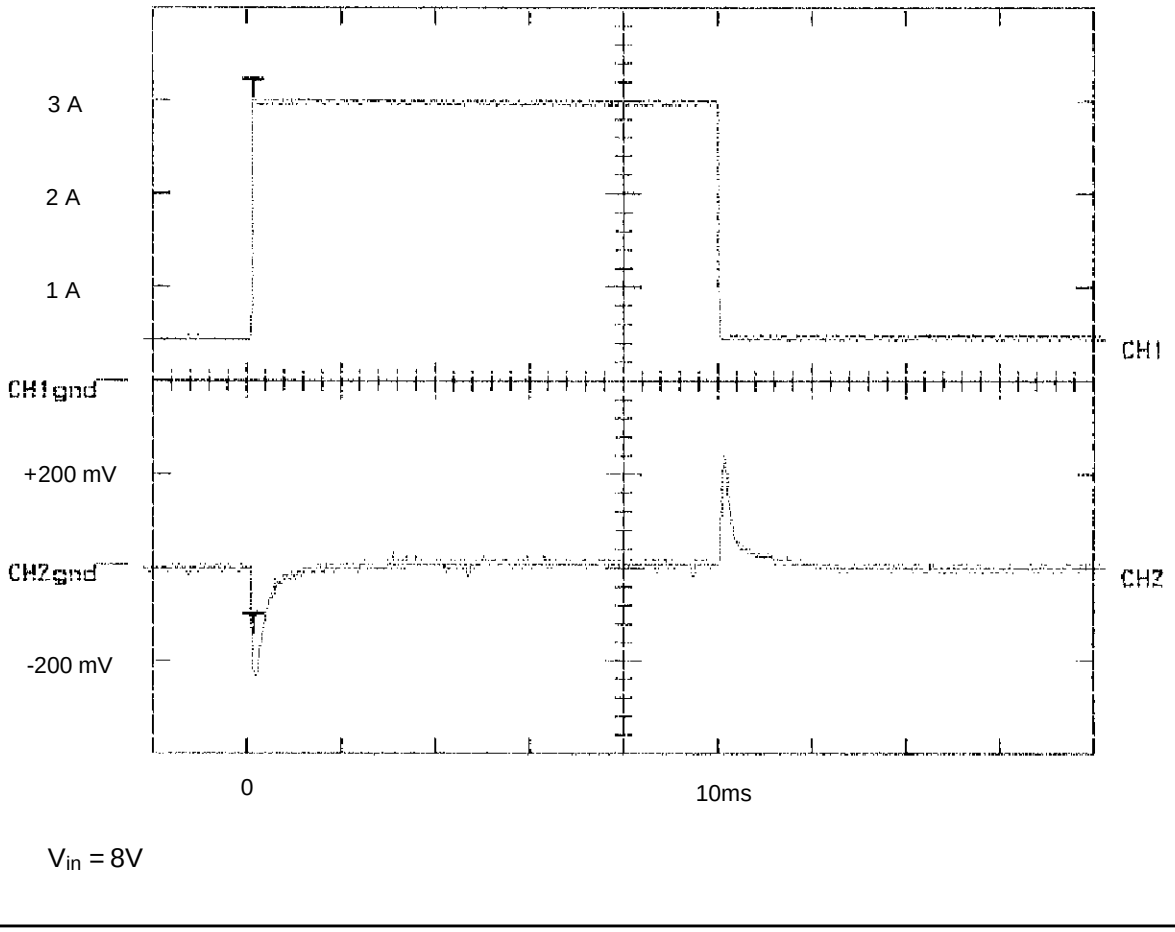
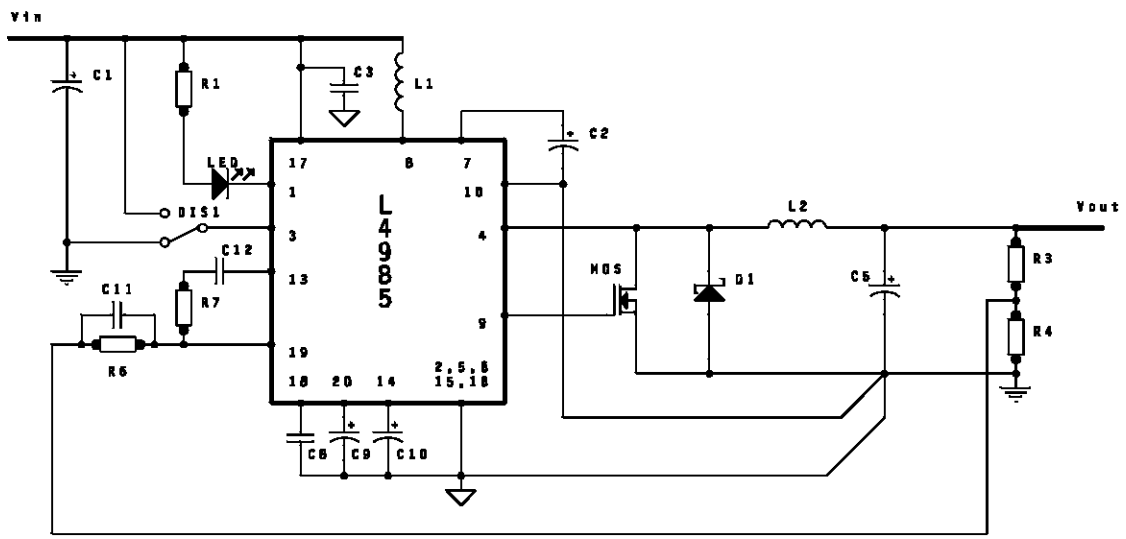


Figure 26: Load Transient Diagram



Application 2: Circuit & part list: see fig. 27

Figure 27: Step Down Converter V_{in} = 6 to 22V; V_{out} = 5.1V; I_{out} = 3A



C1 = 470µF / 25V NCC LXF
C2 = 10µF / 50V
C3 = 330nF film
C5 = 220µF / 10V SANYO OS-CON
C8 = 560pF multilayer
C9 = C10 = 2.2µF / 10V
C11 = 3.9nF
C12 = 5.6nF

R1 = 3.3kΩ
R3 = 8.2kΩ
R4 = 2.7kΩ
R6 = 56kΩ
R7 = 39kΩ

L1 = 180µH axial
L2 = 50µH (Core Magnetics 58120, 27 turns, 0.8mm)

D1 = ST BYV 10 - 40

MOS = DY9410 SILICONIX

Evaluation results:

Symbol	Parameter	Test Condition	Value	Unit
η	Efficiency	V_{in} = 8V; I_{out} = 1A	95.5	%
		V_{in} = 8V; I_{out} = 3A	92.4	%
ΔV_{out}	Line Regulation	V_{in} = 4.5 to 22V; I_{out} = 0.5A	4.0	mV
ΔV_{out}	Load Regulation	V_{in} = 4.5 to 22V; I_{out} = 0.5 to 3A	6.0	mV

Figure 28: Efficiency Diagram

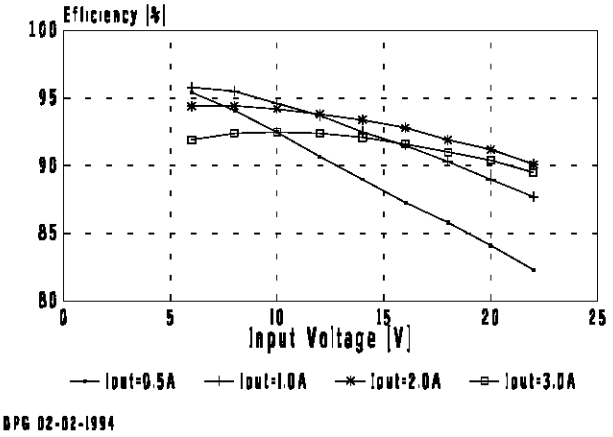
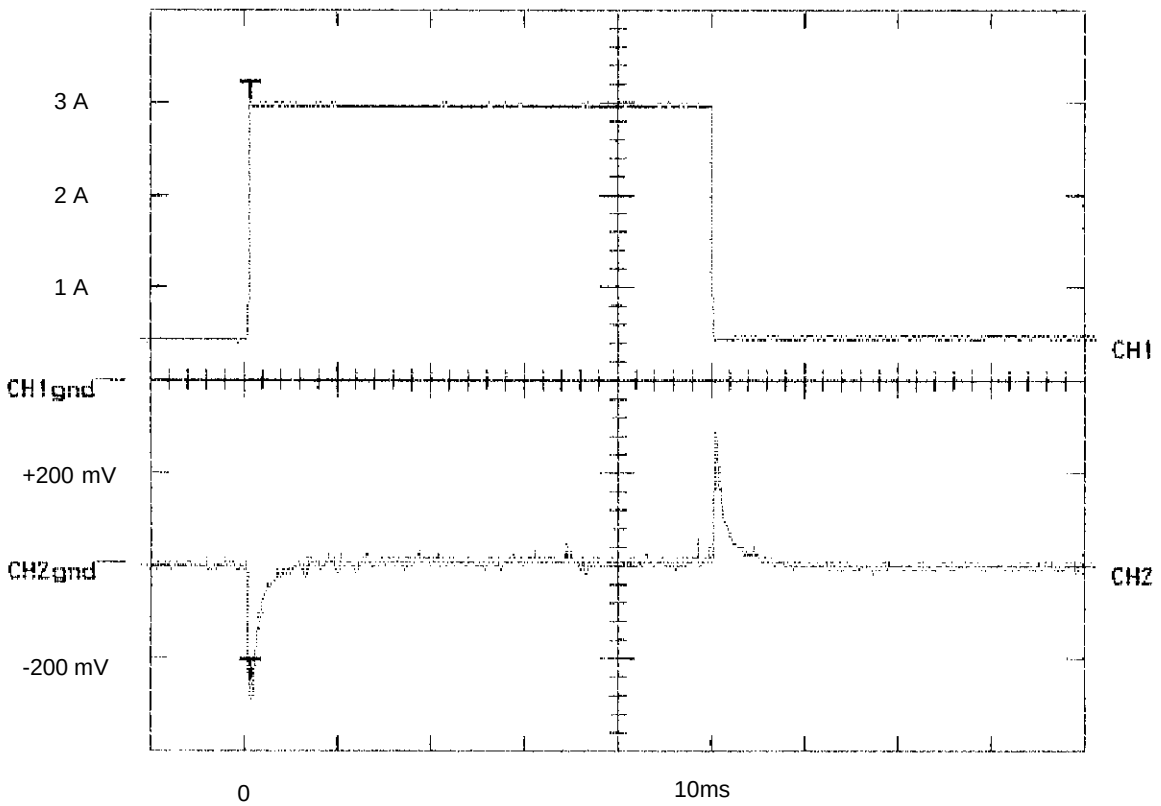


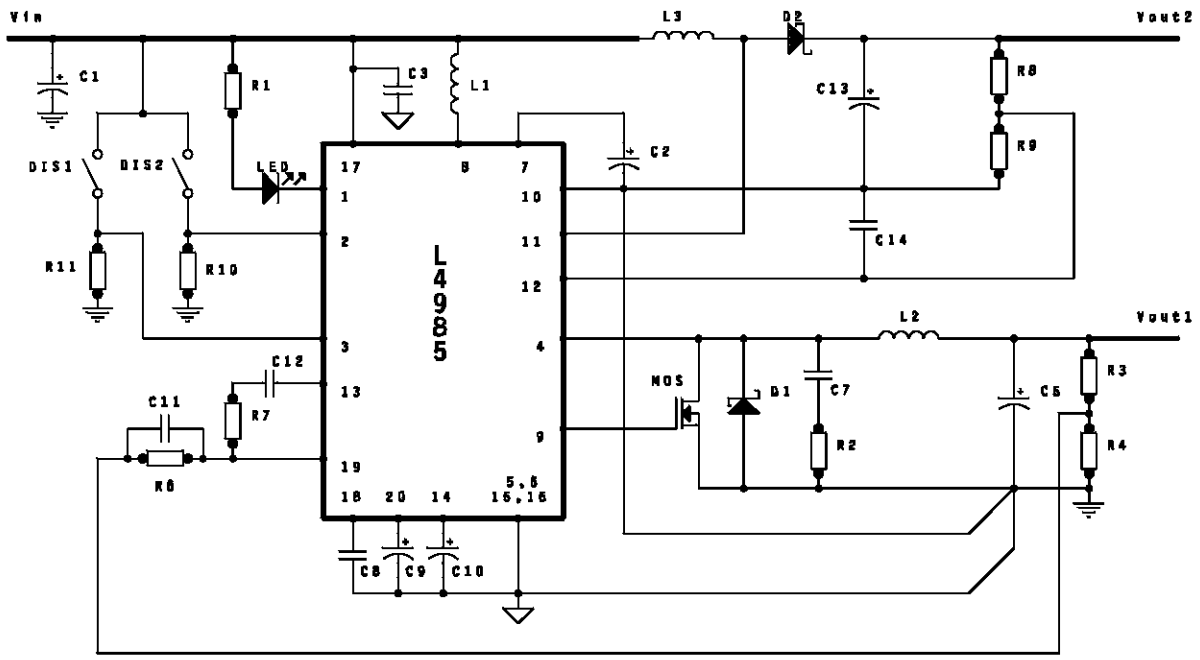
Figure 29: Load Transient Diagram



V_{in} = 12V

Application 3: Circuit & part list: see fig. 30

Figure 30: Dual Converter (main: see applic. 2) ; Auxiliary: V_{out2} = 24V; I_{out2} = 200mA



C1 = 560µF / 25V NCC LXF
C2 = 10µF / 50V
C3 = 330nF film
C5 = 220µF / 10V SANYO OS CON
C7 = 2.2nF film
C8 = 560pF multilayer
C9 = C10 = 2.2µF / 10V
C11 = 3.9nF
C12 = 5.6nF
C13 = 330µF / 35V NCC LXF
C14 = 22nF

R1 = 3.3kΩ
R2 = 4.7Ω
R3 = 8.2kΩ
R4 = 2.7kΩ
R6 = 56kΩ
R7 = 39kΩ
R8 = 47kΩ
R9 = 2.kΩ
R10 = 10kΩ
R11 = 10kΩ

L1 = 180µH axial
L2 = 50µH (Core Magnetics 58120, 27 turns, 0.8mm)
L3 = 50µH (Core Magnetics 58050, 27 turns, 0.6mm)

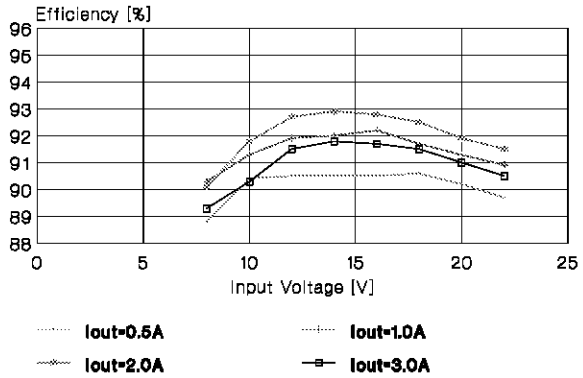
D1 = D2 = ST BYV 10 - 40

MOS = DY9410 SILICONIX

Evaluation results:

Symbol	Parameter	Test Condition	Value	Unit
η	Efficiency	V_{in} = 14V; DIS 2 = HIGH; I_{out1} = 1A; I_{out2} = 0.2A;	92.0	%
		V_{in} = 14V; DIS 2 = HIGH; I_{out1} = 3A; I_{out2} = 0.2A;	91.8	%
ΔV_{out1}	Line Regulation	V_{in} = 8 to 22V; DIS 2 = HIGH I_{out1} = 0.5A; I_{out2} = 20mA;	4	mV
ΔV_{out1}	Load Regulation	V_{in} = 8 to 22V; DIS 2 = HIGH I_{out1} = 0.5 to 3A ; I_{out2} = 0.2A	10	mV
ΔV_{out2}	Line Regulation	V_{in} = 8 to 22V; DIS 2 = HIGH I_{out1} = 0.5A; I_{out2} = 20mA;	50	mV
ΔV_{out2}	Load Regulation	V_{in} = 8 to 22V; DIS 2 = HIGH I_{out1} = 0.5 to 3A ; I_{out2} = 0.2A	300	mV

Figure 31: Efficiency Diagram



APPENDIX

INDUCTANCE VALUE SELECTION IN THE AUXILIARY BOOST

With the aid of fig. 32, we see that, during one switching cycle, the energy sunk from the input is:

$$(1) \qquad E_i = \frac{1}{2} V_{in} (T_{on} + T_{dch}) I_{lp}$$

The peak value of the coil current, is given by:

$$(2) \qquad I_{lp} = \frac{1}{L} V_{in} T_{on}$$

neglecting the voltage drop across the switch. The T_{dch} time is involved in the relationship:

$$(3) \qquad I_{lp} = \frac{1}{L} (V_{out} - V_{in}) T_{dch}$$

where the forward drop across the diode has been neglected.

Solving (2) for T_{on}, (3) for T_{dch} and replacing in (1), we get:

$$(4) \qquad E_i = \frac{1}{2} L I_{lp}^2 \frac{V_{in}}{V_{out} - V_{in}}$$

The energy Ei, reduced by losses, is delivered to the output:

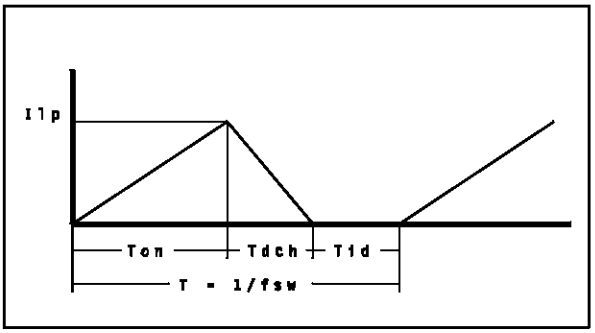
$$(5) \qquad \eta E_i = \frac{V_{out} \ I_{out}}{f_{sw}}$$

where η is the converter efficiency and I_{out} the load current.

We can relate I_{lp} to I_{out} by combining equations (4) and (5):

$$I_{lp}^2 = \frac{2 (V_{out} - V_{in}) I_{out}}{\eta L f_{sw}}$$

Figure 32: Discontinuous Boost Inductor Current



Due to current limiting, I_{lp} cannot exceed I_x. Thus from:

$$I_{lp}^2 < I_x^2$$

we can find the minimum inductance value needed to transfer the energy requested by the load from input to output:

$$L_{min} = \frac{2 (V_{out} - V_{in}) I_{out}}{\eta I_x^2 f_{sw}}$$

Since I_x = 1.5 A and η is close to 90%, it is possible to assume that $2 / (\eta I_x^2) \approx 1$ and, therefore:

$$L_{min} = \frac{(V_{out} - V_{in}) I_{out}}{f_{sw}}$$

Of course, L_{min} should be sized so to guarantee the energy transfer even in the worst conditions, that is for $V_{in} = V_{inmin}$ and $I_{out} = I_{outmax}$. Thus, finally:

$$L_{min} = \frac{(V_{out} - V_{inmin}) I_{outmax}}{f_{sw}}$$