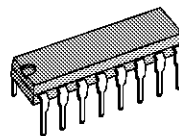


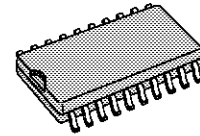
## ADVANCED VOLTAGE REGULATOR

PRODUCT PREVIEW

- ENABLE AND SENSE INPUTS (EN, SI) PROTECTED AGAINST NEGATIVE TRANSIENTS DOWN TO -5V
- RESET THRESHOLD ADJUSTABLE FROM 3.8 TO 4.7V
- EXTREMELY LOW QUIESCENT CURRENT, 65 $\mu$ A (LESS THAN 90 $\mu$ A) IN STANDBY MODE
- OPERATING DC SUPPLY VOLTAGE RANGE 5V - 28V
- OPERATING TRANSIENT SUPPLY VOLTAGE UP TO 40V
- HIGH PRECISION STANDBY OUTPUT VOLTAGE 5V  $\pm$  1% WITH 100mA CURRENT CAPABILITY
- OUTPUT 2 VOLTAGE 5V  $\pm$  2% WITH 400mA CURRENT CAPABILITY (ADJ WIRED TO V<sub>OUT2</sub>)
- OUTPUT 2 VOLTAGE ADJUSTABLE BY EXTERNAL VOLTAGE DIVIDER
- OUTPUT 2 DISABLE FUNCTION FOR STANDBY MODE



DIP16 (12+2+2)



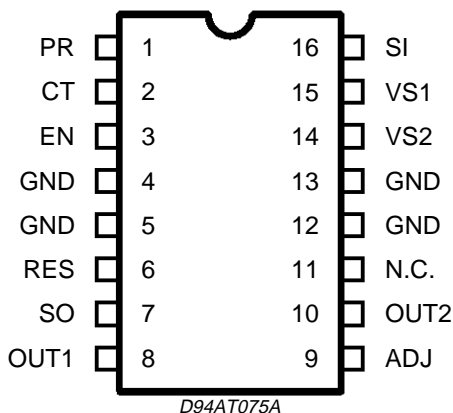
SO20 (12+4+4)

**ORDERING NUMBERS:** L4938E (DIP)  
L4938ED (SO)

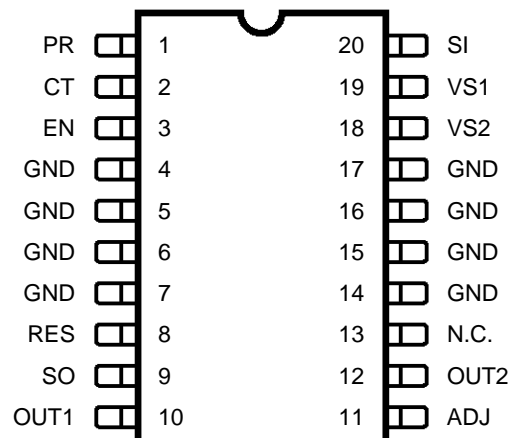
### DESCRIPTION

The L4938E is a monolithic integrated dual voltage regulator with two very low dropout outputs and additional functions as power-on reset and input voltage sense. It is designed for supplying the microcomputer controlled systems especially in automotive applications.

### PIN CONNECTIONS



DIP 12+2+2



SO 12+4+4

## ABSOLUTE MAXIMUM RATINGS

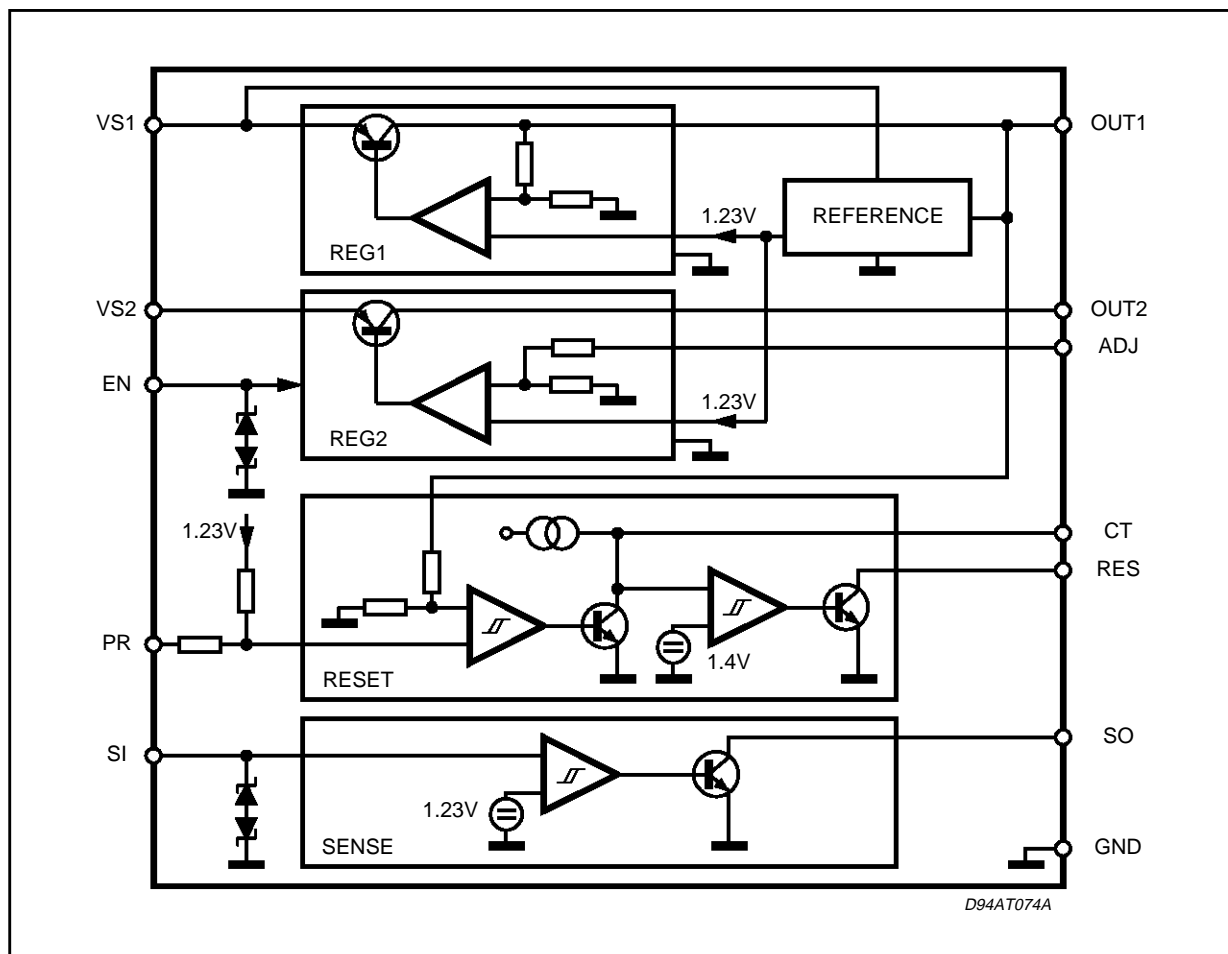
Symbol	Parameter	Value	Unit
$V_{INDC}$	DC Operating Supply Voltage	28	V
$V_{INTR}$	Transient Operating Supply Voltage ( $T < 400\text{ms}$ )	-14 to 40	V
$I_O$	Output Current	internally limited	
$V_{SI}$	Sense Input Voltage (Voltage Forced) (note 2)	-20 to 20	V
$I_{SI}$	Sense Input Current (Current Forced) (note 2)	$\pm 1$	mA
$V_{EN}$	Enable Input Voltage (Voltage Forced) (note 2)	-20 to 20	V
$I_{EN}$	Sense Input Current (Current Forced) (note 2)	$\pm 1$	mA
$V_{RES}, V_{SO}$	Output Voltages	-0.3 to 20	V
$I_{RES}, I_{SO}$	Output Currents (Output Low)	5	mA
$P_O$	Power Dissipation at $T_{amb} = 80^\circ\text{C}$ (note 3) Powerdip 12+2+2	875	mW
$T_{stg}$	Storage Temperature	-65 to 150	$^\circ\text{C}$
$T_j$	Operating Junction Temperature	-40 to 150	$^\circ\text{C}$
$T_{JSD}$	Thermal shutdown junction temperature Output 2 will shut-down typically at $T_j$ 10K lower than output 1	165	$^\circ\text{C}$

Note: The circuit is ESD protected according to MIL-STD-883C

Note 2: Current forced means voltage unlimited but current limited to the specified value  
Voltage forced means voltage limited to the specified values while the current is not limited

Note 3: Typical value soldered on a PC board with 8cm<sup>2</sup> copper ground plane (35mm thick).

## BLOCK DIAGRAM



## THERMAL DATA

Symbol	Parameter	DIP 12+2+2	SO 12+4+4	Unit
$R_{th\ j-amb}$	Thermal Resistance Junction-ambient	40	50	°C/W

Note 3: Typical value soldered on a PC board with 8cm<sup>2</sup> copper ground plane (35mm thick).

## PIN FUNCTIONS

PIN (DIP 12+2+2)	PIN (SO 12+4+4)	Name	Function
14	18	VS2	Supply Voltage (400mA Regulator)
15	19	VS1	Supply Voltage (100mA Regulator, Reset, Sense)
16	20	S1	Sense Input
1	1	PR	Reset Theresold Programming
2	2	CT	Reset Delay Capacitor
3	3	EN	Enable (low will activate the 400mA regulator)
4, 5, 12, 13	4, 5, 6, 7, 14, 15, 16, 17	GND	Ground
6	8	RES	Reset Output
7	9	SO	Sense Output
8	10	OUT 1	100mA Regulator Output
9	11	ADJ	Feedback of 400mA Regulator
10	12	OUT 2	400mA Regulator Output
11	13	NC	Not Connected

ELECTRICAL CHARACTERISTICS ( $V_S = 14V$ ;  $T_j = -40$  to  $150^\circ C$  unless otherwise specified.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>OUT 1</b>						
$V_{O1}$	Supply Output Voltage	$V_S = 6$ to $28V$ ; $I_{O1} = 400\mu A$ to $100mA$	4.9	5	5.1	V
		$T_j \leq 125^\circ C$ ; $I_{O1} = 50$ to $400\mu A$	4.8	5	5.2	V
$V_{DP1}$	Dropoutput Voltage 1	$I_{OUT1} = 10mA$		0.1	0.2	V
		$I_{OUT1} = 100mA$ ; $V_S = 4.8V$		0.2	0.4	V
$V_{OL01}$	Load Regulation 1	$I_{OUT1} = 1$ to $100mA$ (after regulation setting)			25	mV
$V_{LIM1}$	Current Limit 1	$V_{OUT1} = 0.8$ to $4.5V$	100	200	400	mA
$I_{QSB}$	Quiescent Current in Standby Mode	$I_{EN} \geq 2.4V$ (output 2 disabled) $I_{O1} = 0.1mA$ ; $V_{SI} > 1.3V$		65	90	$\mu A$
		$T_j < 85^\circ C$ ; $R_{PR} = 0$		75		$\mu A$
<b>OUT 2</b>						
$V_{O2}$	Output Voltage 2 ADJ connected to OUT 2	Enable = LOW; $V_S = 6$ to $28V$ ; $I_{O2} = 5$ to $400mA$	4.9		5.1	V
$V_{DP2}$	Dropoutput Voltage 2	$I_{OUT2} = 100mA$ ; $V_S = 4.8V$		0.2	0.3	V
		$I_{OUT2} = 400mA$ ; $V_S = 4.8V$		0.3	0.6	V
$V_{OL02}$	Load Regulation 2	$I_{OUT1} = 5$ to $400mA$ (after regulation setting)			50	mV
$R_{ADJ}$	Adjust Input Resistance		60	100	150	K $\Omega$
$I_{LIM2}$	Current Limit 2	$V_{O2} = 0.8$ to $4.5V$	450	650	1300	mA
$I_Q$	Quiescent Current	$I_{OUT1} = 100mA$ ; $I_{OUT2} = 400mA$			20	mA
<b>OUT1, OUT 2</b>						
$V_{OL1,2}$	Line Regulation	$V_S = 6$ to $28V$ ; $I_{O1} = 1mA$ , $I_{O2} = 5mA$ , (after regulation setting)			20	mV

## ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ENABLE INPUT						
V <sub>ENL</sub>	Enable Input Low Voltage (Output 2 Active)		-20		1	V
V <sub>ENH</sub>	Enable Input High Voltage		1.4		20	V
V <sub>ENhyst</sub>	Enable Hysteresis		20	30	60	mV
I <sub>EN LOW</sub>	Enable Input Current Low	V <sub>EN</sub> = 0	-20	-8	-3	μA
I <sub>EN HIGH</sub>	Enable Input Current High	V <sub>EN</sub> = 1.1 to 7V; T <sub>J</sub> < 130°C;	-1	0	1	μA
		V <sub>EN</sub> = 1.1 to 7V; T <sub>J</sub> = 130 to 150°C;	-10	0	10	μA
RESET CIRCUIT						
V <sub>RT</sub>	Reset Theresold Voltage (note4)	R <sub>PR</sub> = ∞	4.5	V <sub>O1-0.3</sub>	V <sub>O1-0.2</sub>	V
		R <sub>PR</sub> = 0	3.65	3.8	3.95	V
V <sub>RTH</sub>	Reset Theresold Hysteresis	R <sub>PR</sub> = ∞	15	40	100	mV
t <sub>RD min</sub>	Reset Pulse Delay	C <sub>RES</sub> = 47nF; t <sub>r</sub> ≤ 30μs; (note 5)	40	60	100	ms
t <sub>RD nom</sub>	Reset Pulse Delay	C <sub>RES</sub> = 47nF; (note 6)	60	100	140	ms
t <sub>RR</sub>	Reset Reaction Time	C <sub>RES</sub> = 47nF	10	50	150	μs
I <sub>CT</sub>	Pull Down Capability of the Discharge circuit	V <sub>OUT1</sub> < V <sub>RT</sub>	3	6	15	mA
I <sub>CT</sub>	Charge Current	V <sub>OUT1</sub> > V <sub>RT</sub>	-1.3	-1	0.7	μA
V <sub>RESL</sub>	Reset Output Low Voltage	R <sub>RES</sub> = 10KΩ to V <sub>OUT1</sub> V <sub>OUT1</sub> ≥ 1.5V			0.4	V
V <sub>RESH</sub>	Reset Output High Leakage current	V <sub>RES</sub> = 5V			1	μA
SENSE COMPARATOR						
V <sub>SI</sub>	Functional Range		-20		20	V
V <sub>SIT</sub>	Sense Threshold Voltage	Falling Edge; T <sub>J</sub> <130°C	1.08	1.16	1.24	V
		Falling Edge; T <sub>J</sub> 130 to 150°C	1.05	1.16	1.29	V
V <sub>SITH</sub>	Sense Threshold Hysteresis		10	30	60	mV
V <sub>SOL</sub>	Sense Output Low Voltage	V <sub>SI</sub> ≤ 1.05V; R <sub>SO</sub> =10KΩ connected to 5V; V <sub>S</sub> ≥ 5V			0.4	V
I <sub>SOH</sub>	Sense Output Leakage	V <sub>SO</sub> = 5V; V <sub>SI</sub> ≥ 1.5V			1	μA
I <sub>SI HIGH</sub>	Sense Input Current High	V <sub>SI</sub> = 1.1 to 7V; T <sub>J</sub> <130°C	-1	0	1	μA
		V <sub>SI</sub> = 1.1 to 7V; T <sub>J</sub> 130 to 150°C	-10	0	10	μA
I <sub>SI LOW</sub>	Sense Input Current Low	V <sub>SI</sub> = 0V	-20	-8	-3	μA

Note :

4) The reset threshold can be programmed continuously from typ 3.8V to 4.7V by changing a value of an external resistor from pin PR to GN

5) This is a minimum reset time according to the hysteresis of the comparator. Delay time starts with  $V_{OUT1}$  exceeding  $V_{RT}$ 6) This is the nominal reset time depending on the discharging limit of  $C_T$  (saturation voltage) and the upper threshold of the timer comparator. Delay time starts with  $V_{OUT1}$  exceeding  $V_{RT}$ 7) The leakage of  $C_T$  must be less than 0.5mA (2V). If an external resistor between  $C_T$  and  $V_{OUT1}$  is applied, the leakage current may be increased. The external resistor should have more than 30K $\Omega$ .  
for stability:  $C_S \geq 1\mu F$ ,  $C_{O1} \geq 10\mu F$ ,  $C_{O2} \geq 10\mu F$ ,  $ESR \leq 5\Omega$  (designed target for resistive load) For details see application note.8) For transients exceeding 20V or -20V external protection is required at the Pins SI and EN as shown at Pin EN. The protection proposed will provide proper function for transients in the range of  $\pm 200V$ . If the zener diode is omitted the external resistor should be raised to 200K $\Omega$  to limit the current to 1mA. Without the zener diode, the function 20V or -20V can not be guaranteed.



## Standby Regulator

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled. A second regulation path will keep the output voltage without load below 5.5V even at high temperatures.

### Output 2 Voltage

The output 2 regulator can be switches OFF via the enable input.



Connecting a resistor divider  $R_{1E}$ ,  $R_{2E}$  to the ADJ, OUT2 pin the output voltage 2 can be programmed to the value of

$$V_{OUT2} = V_{OUT1} \left( 1 + \frac{R_{1E}(R_{2E} + R_{ADJ})}{R_{2E} \cdot R_{ADJ}} \right)$$

with  $R_{ADJ} = 60K$  to  $150K$  and  $V_{OUT1} = 4.95$  to  $5.05V$ .

For an exact calculation the temperature coefficient ( $T_c$  -2000ppm) of the internal resistor ( $R_{ADJ}$ ) must be taken into account. Pin ADJ in this mode should not have a capacitive burden because this would reduce the phase margin of the regulator loop.

### Reset circuit

The reset circuit supervises the standby output voltage. The reset output (RES) is defined from  $V_{OUT} \geq 1V$ .

Even if  $V_S$  is lacking, the reset generator is supplied by the output voltage  $V_{OUT1}$ .

The reset threshold of 4.7V is defined with the internal reference voltage (note 9) and standby output divider, when pin PR is left open. The reset threshold voltage can be programmed in the range from 3.8V to 4.7V by connecting an external resistor from pin PR to GND.

The value of the programming resistor  $R_{PR}$  can be calculated with:

$$R_{PR} = \frac{22K}{\frac{4.7V}{V_{RT}} - 1} - 92.9K, 3.8V \leq V_{RT} \leq 4.7V$$

The reset pulse delay time  $t_{RD}$ , is defined with the charge time of an external capacitor  $C_T$ :

$$t_{RDmin} = \frac{C_T \cdot 0.6V}{1\mu A} \text{ (note 5)}$$

$$t_{RDnom} = \frac{C_T \cdot 1.4V}{1\mu A} \text{ (note 6)}$$

The reaction time of the reset circuit originates from the noise immunity. Standby output voltage drops below the reset threshold only a bit longer

than the reaction time results in a shorter reset delay time. The nominal reset delay time will be generated for standby output voltage drops longer than approximately  $50\mu s$ .

The minimum reset time is generated if reset condition only occurs for a short time triggering a reset pulse but not completely discharging  $C_T$ . The reset can be related to output2 on request. If higher charge currents for the reset capacitor are required a resistors from Pin  $C_T$  to OUT1, may be used to increase the current. We recommended the use of  $10K\Omega$  to 5V as an output pull up.

### Sense Comparator

The sense comparator compares an input signal with an internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application. It can be used to supervise the input voltage either before or after the protection diode and to give additional information to the microprocessor like low voltage warnings. We recommended the use of  $10K\Omega$  to 5V as an output pull up.

Note 9:

The reference is alternatively supplied from  $V_S$  or  $V_{OUT1}$ . If one supply is present, the reference is operating.

### Thermal Protection

Both outputs are provided with an overtemperature shut down regulation power dissipation down to uncritical values.

Output 2 will shut down approximately 10K before output 1.

Under normal conditions shut down of output 2 will allow the chip to cool down again. Thus output 1 will be unaffected.

The thermal shut down reduces the output voltages until power dissipation and the flow of thermal energy out of the chip balance.

### Transient Sensitivity

In proper operation ( $V_{OUT} > 4.5V$ ) the reference is supplied by  $V_{OUT1}$  thus reducing sensitivity to input transients.

Precise Data will be issued as soon as samples are available.

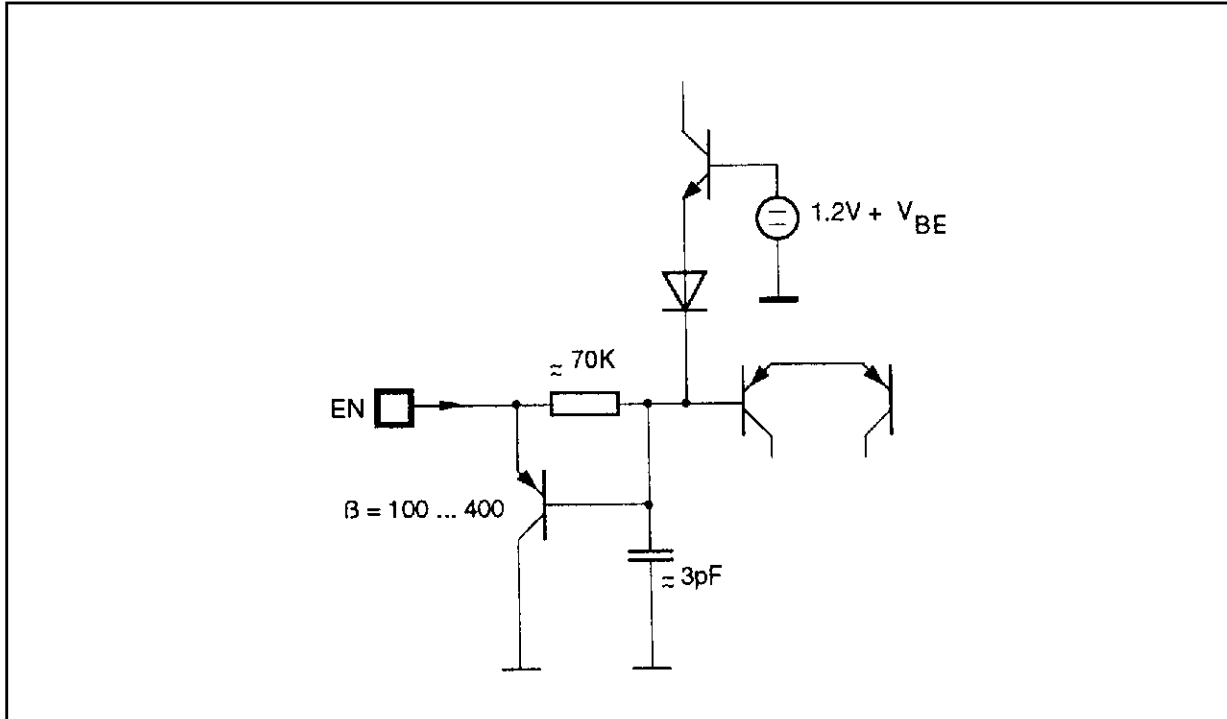
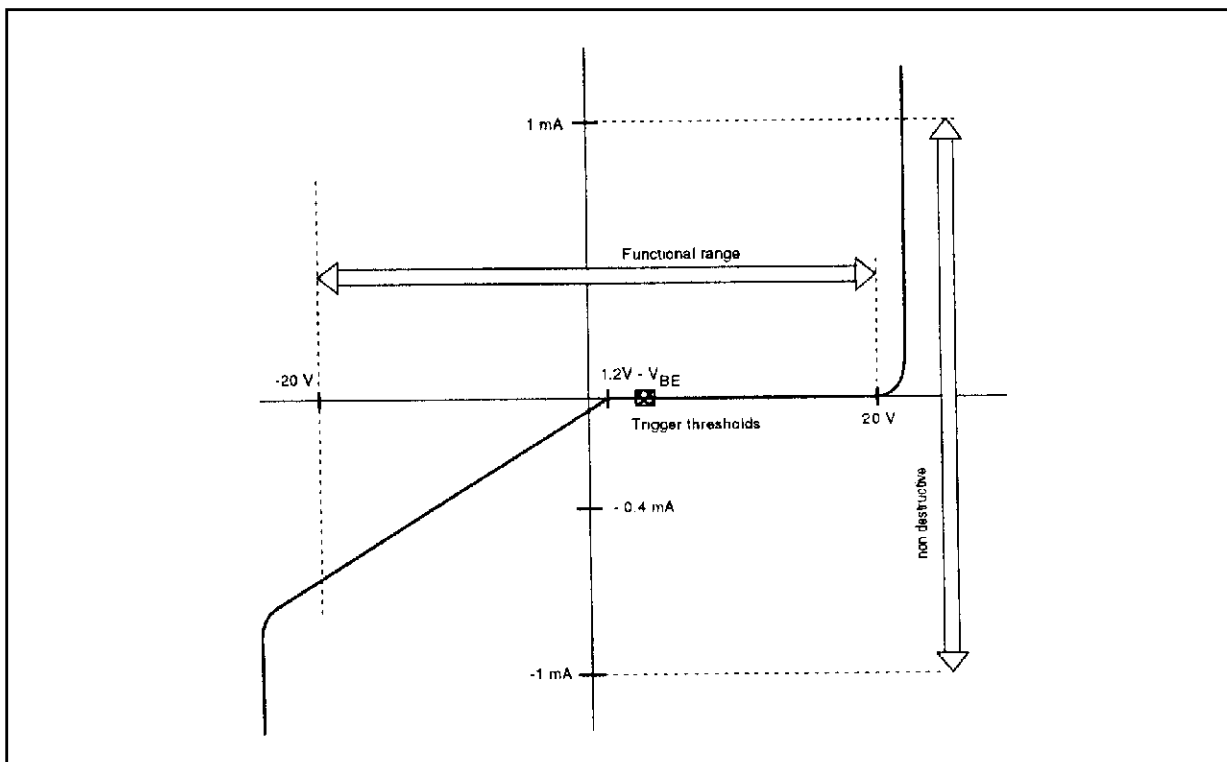


**INPUT PROTECTION**

The Inputs Enable (EN) and sense in(SI) are pro-

ected against negative transients. Figure 5 is showing the simplified schematic.

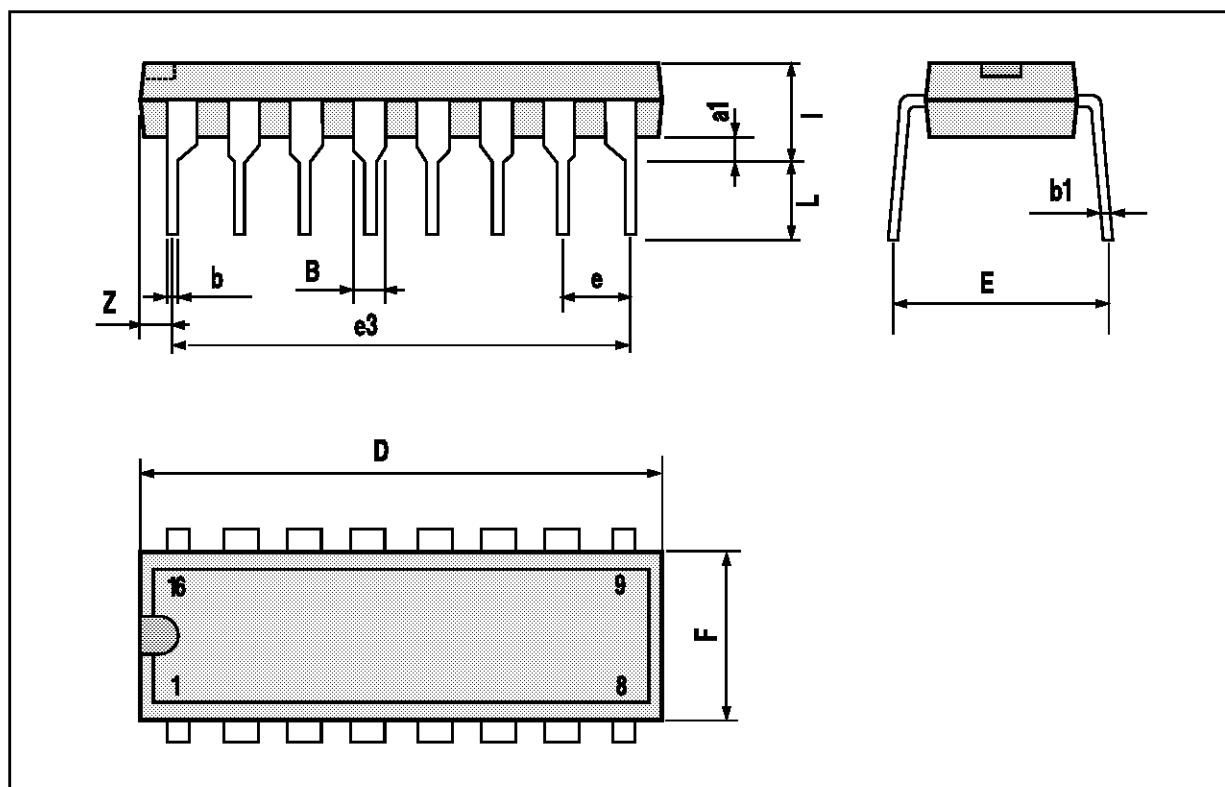
**Figure 5:**

**Input Characteristics of SI, EN:**



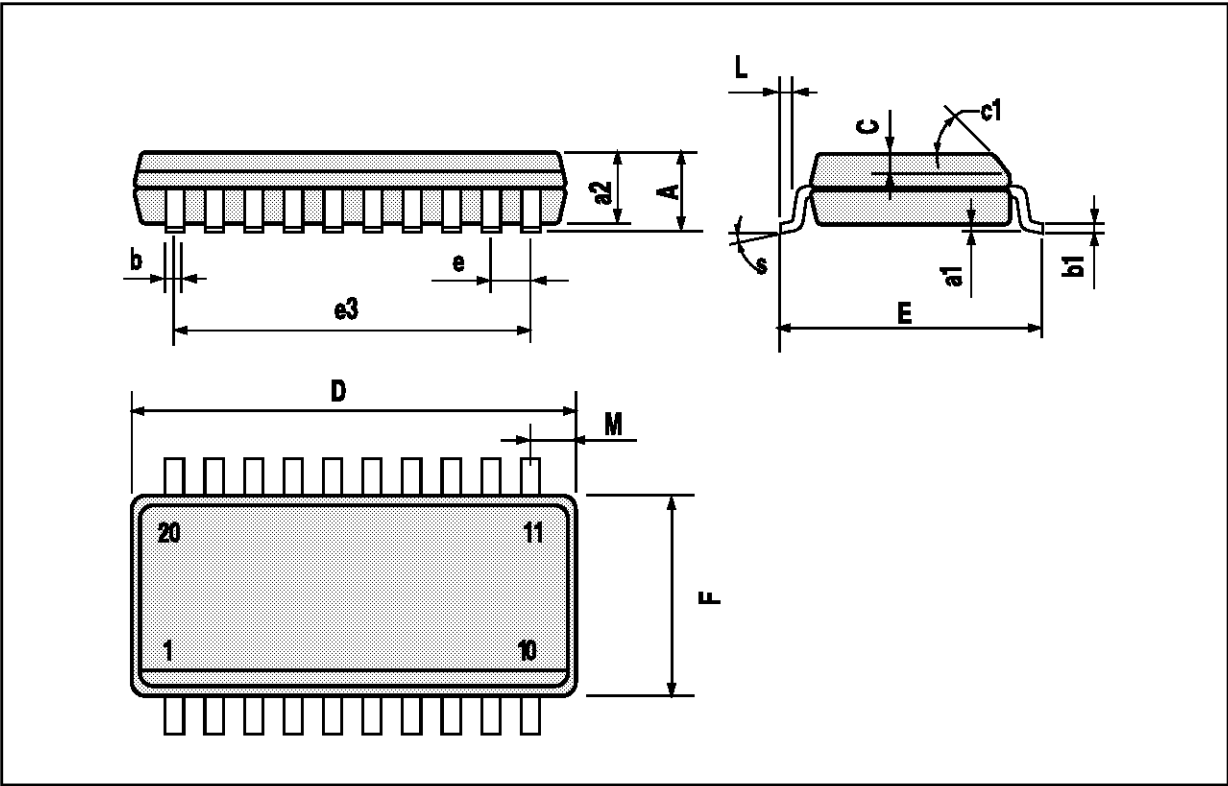
## DIP16 (12+2+2) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050



SO20 (12+4+4) PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					



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