SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

SGS-THOMSON SLIC KIT AC MODELS

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INDEX

1. INTRODUCTION

In this note you can find the basic structure of all SGS-THOMSON Microelectronics SLICs concerning AC performances.

In all these SLICs are present two capacitors one for AC/DC path splitting and the other for loop stability. The effect of these capacitors is neglectible in speech band (300 - 3400Hz) therefore for each KIT are evaluated the typical AC performances not considering their influence.

If performances on a wider band or very high accuracy are requested the effect of these capacitors must be included.

Another possibility to study the effect of these capacitors is to enter the SLIC structure in a circuit simulator like SPICE, as shown at the end of this note with the L3000N/L3092 SLIC KIT and L303X monochip SLIC.

2. L3000N/L3010 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000N/L3010 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3010. The components names are the same used in the data sheet.

Figure 1: L3000N/3010 SLIC Basic Structure.

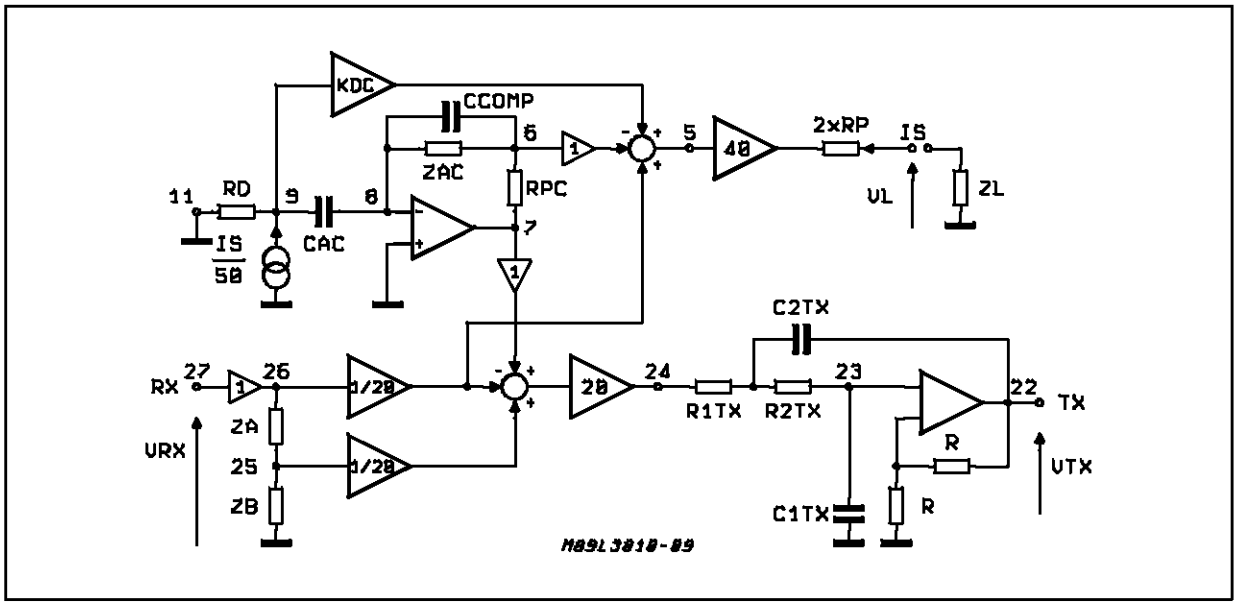
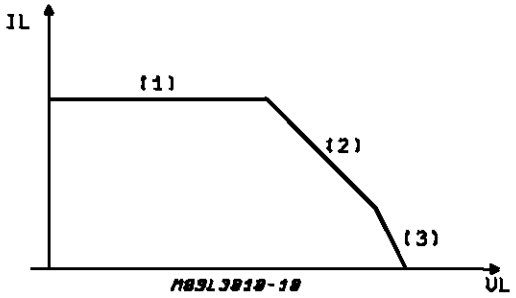


Figure 2: L3000N/3010 DC Characteristic.



The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 2 for region 1

RD = RDC ; KDC = 2 for region 2

RD = RDC ; KDC = 2/3 for region 3

CAC is a large capacitor (typ. 22µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 8.2nF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 2.1. Also the TTX filter influence in speech band is neglected.

2.1. SLIC IMPEDANCE AT LINE TERMINATIONS:

$$ZML = \left.\frac{V_L}{I_S}\right|_{VRX = 0} = (4/5) \times ZAC + 2 \times RP$$

2.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

2.3. SENDING GAIN

$$G_S = \left.\frac{V_{TX}}{V_L}\right|_{VRX = 0} = -\frac{ZAC + RPC}{ZAC + (5/2) \cdot RP}$$

therefore if RPC = (5/2) x RP

$$G_S = -1$$

2.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \cdot \left(\frac{ZB}{ZA + ZB} - \frac{ZL + 2 \cdot RP - (4/5) \cdot RPC}{ZL + ZML}\right)$$

therefore if RPC = (5/2) · RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

3. L3000N/L3030 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000N/L3030 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3030 in PLCC package. The components names are the same used in the data sheet.

As you can see on the L3000N/L3030 data sheet the large AC/DC splitting capacitor (typ. 22µF) can be avoided using the on chip capacitor multiplier. In the following you can see the basic structure in both cases.

Figure 3: L3000N/L3030 SLIC Configured without Capacitor Multiplier Basic Structure.

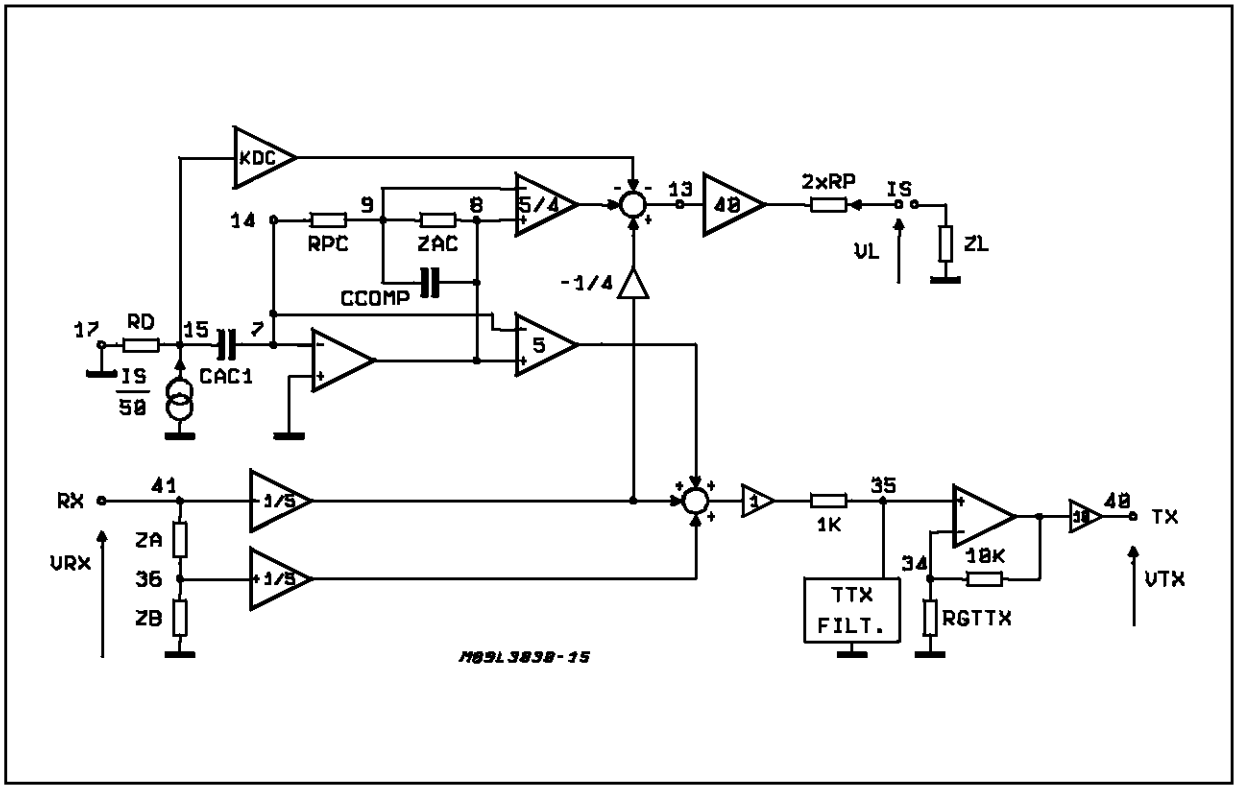


Figure 4: L3000N/L3030 SLIC Configured with Capacitor Multiplier Basic Structure.

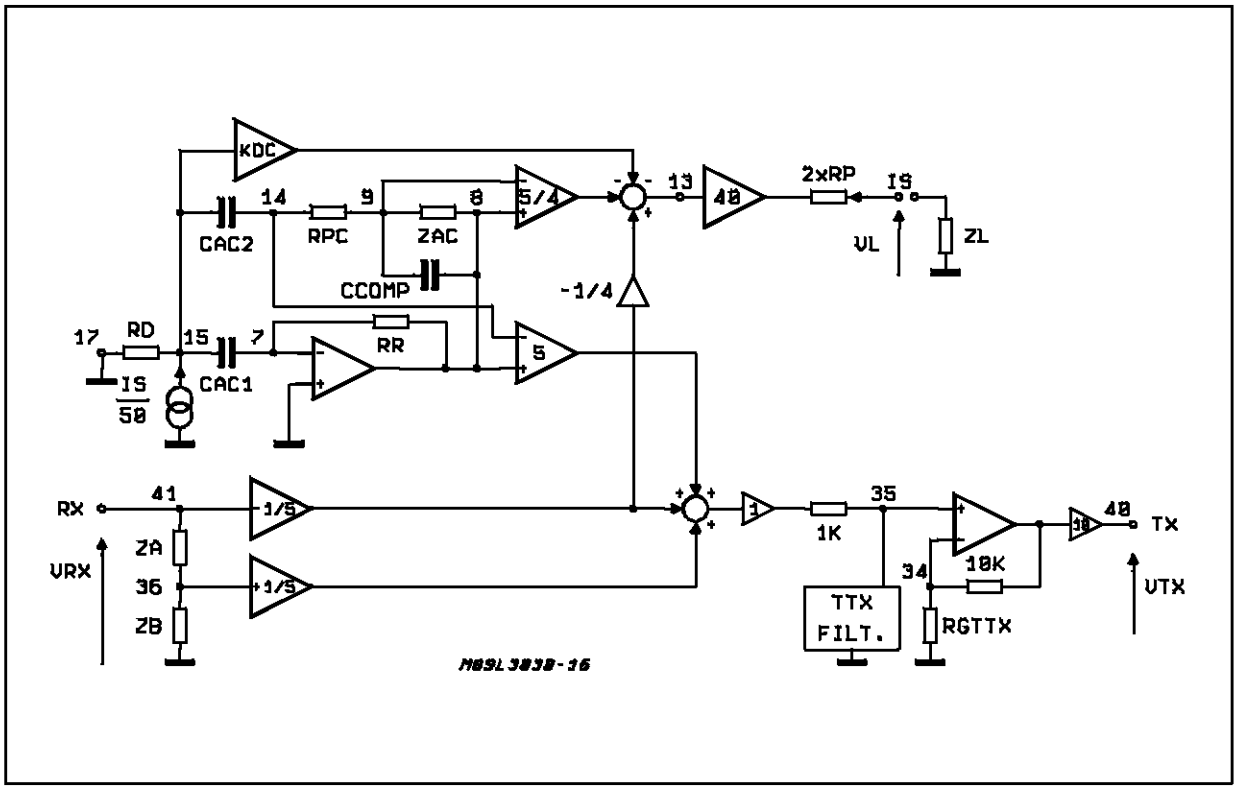
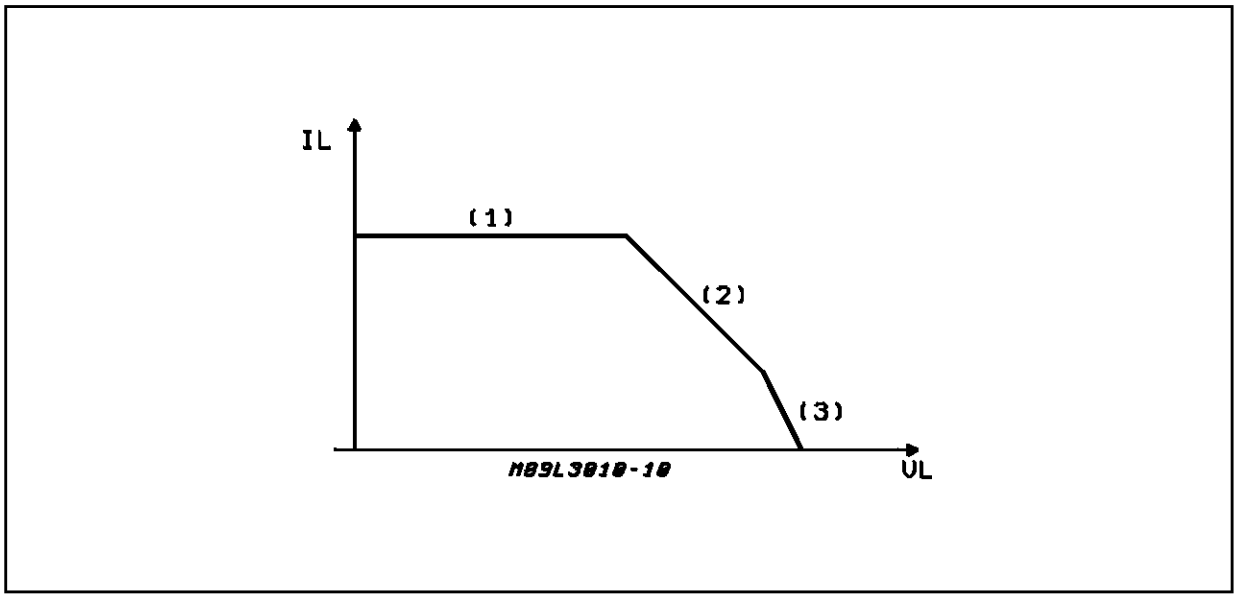


Figure 5: L3000N/3030 DC Characteristic.



The RD and KDC values depends on the working point on DC characteristic, in particular :

RD = infinite ; KDC = 5/4 for region 1

RD = RDC ; KDC = 5/4 for region 2

RD = RDC ; KDC = 5/12 for region 3

CAC1 or the sinthesized capacitor obtained with the capacitor multiplier is relatively large (typ. 22µF) and it is used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 10nF) used to guarantee loop stability.

CAC1, CAC2 and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC1 or the sinthetized capacitor obtained with the capacitor multiplier equivalent to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 3. Also the TTX filter influence in speech band is neglected. The TTX filter impedance is supposed to be equal to RGTTX/10 in speech band and zero at the TTX frequency

3.1. SLIC IMPEDANCE AT LINE TERMINATIONS:

$$ZML = \frac{V_L}{I_S}\Bigg|_{VRX = 0} = ZAC + 2 \times RP$$

3.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$$G_R = 1$$

3.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\Bigg|_{VRX = 0} = -\frac{ZAC + RPC}{ZAC + 2 \cdot RP}$$

therefore if RPC = 2 x RP

$$G_S = -1$$

3.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = 2 \cdot \left(\frac{ZB}{ZA + ZB} - \frac{ZL + 2 \cdot RP - (4/5) \cdot RPC}{ZL + ZML}\right)$$

therefore if RPC = 2 · RP and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP, CAC and TTX filter in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

4. L3000N/L3092 SLIC KIT BASIC STRUCTURE

Here below you can see the basic structure of the L3000N/L3092 SLIC KIT concerning AC performances.

For an easier representation the high voltage part is drawn as a single ended amplifier with a gain of 40. Close to each node is written the corresponding pin number of L3092. The components names are the same used in the data sheet.

Figure 6: L3000N/3092 SLIC Basic Structure.

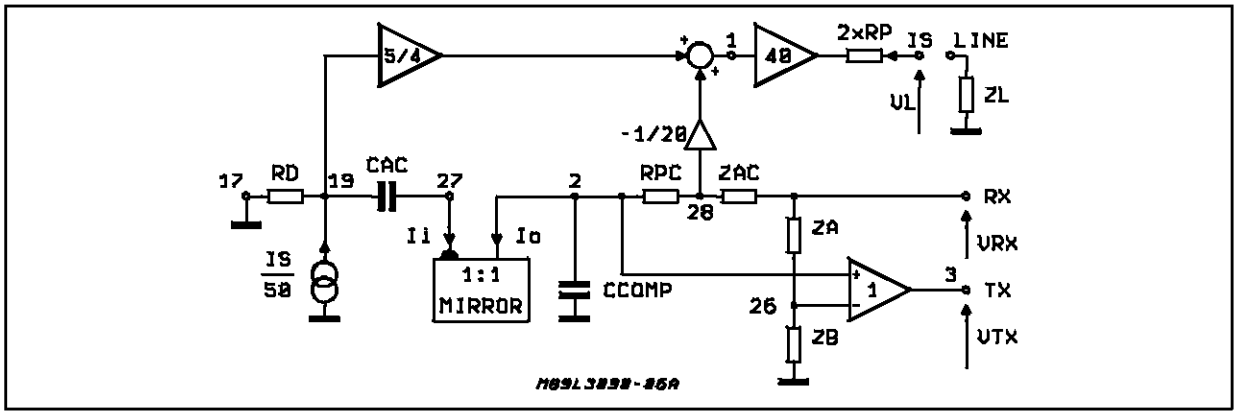
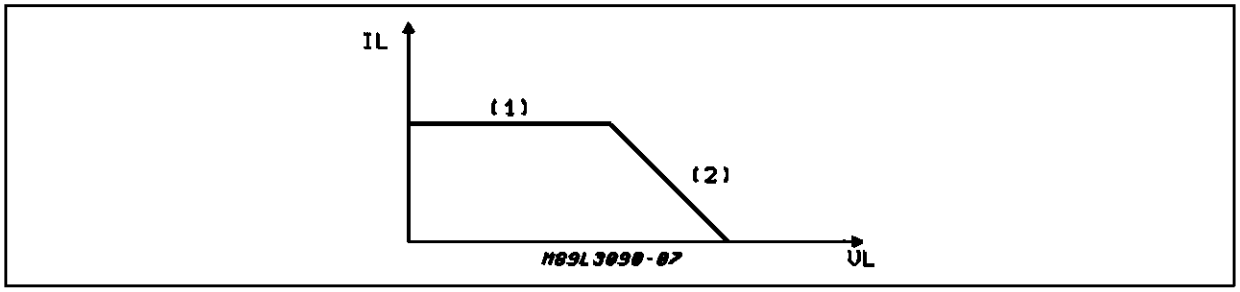


Figure 7: L3000N/3092 DC Characteristic.



The RD value depends on the working point on DC characteristic, in particular :

RD = infinite for region 1

RD = RDC for region 2

CAC is a large capacitor (typ. 47µF) used to split AC and DC components of line current.

CCOMP is a small capacitor (typ. 390pF) used to guarantee loop stability.

CAC and CCOMP values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relationships can be easily obtained from the circuit diagram of fig. 4.1.

4.1. SLIC IMPEDANCE AT LINE TERMINATION

$$ZML = \left.\frac{V_L}{I_S}\right|_{VRX = 0} = (ZAC/25) + 2 \times RP$$

4.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZML}$$

therefore if ZL = ZML

$G_R = -1$

4.3. SENDING GAIN

$$G_S = \left.\frac{V_{TX}}{V_L}\right|_{VRX = 0} = -0.5 \cdot \left(\frac{ZAC + RPC}{ZAC + 25 \cdot (2 \cdot RP)}\right)$$

therefore if RPC = 25 x (2 x RP)

$G_S = -1$

4.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = \frac{ZL + 2 \cdot RP - (RPC/25)}{ZL + ZML} - \frac{ZB}{ZA + ZB}$$

therefore if RPC = 25 (2 · RP) and ZA/ZB = ZML/ZL

THL = 0

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP and CAC in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 6).

5. L303X MONOCHIP SLIC BASIC STRUCTURE

Here below you can see the basic structure of the L303X MONOCHIP SLIC family (L3035, L3036, L3037) concerning AC performances.

Close to each node is written the corresponding pin number. The components names are the same used in the data sheet.

Figure 8: L303X Monochip SLIC Basic Structure.

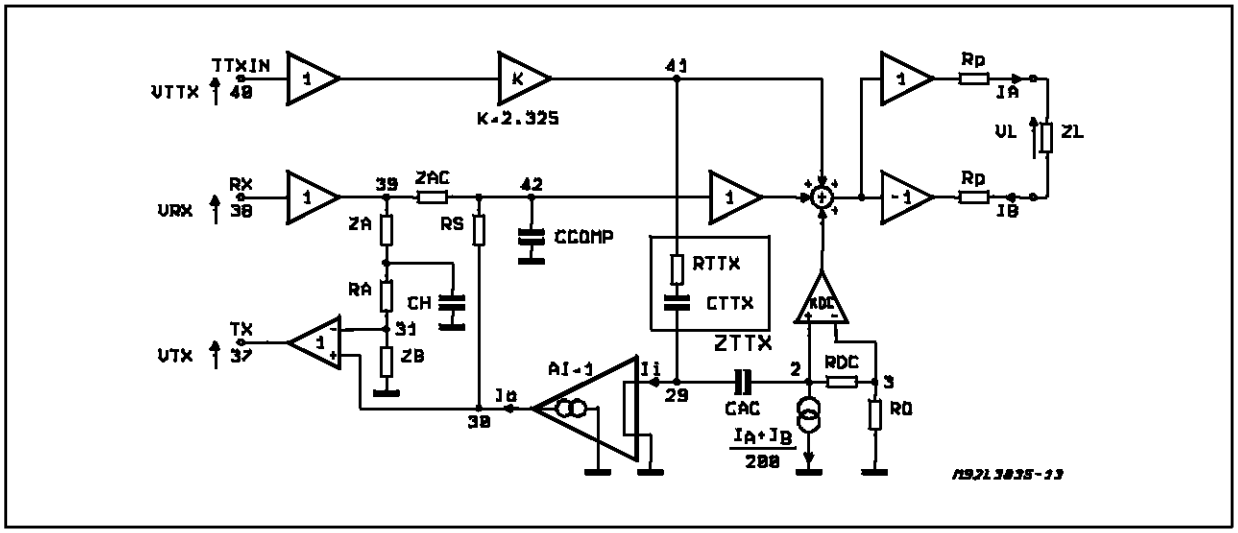
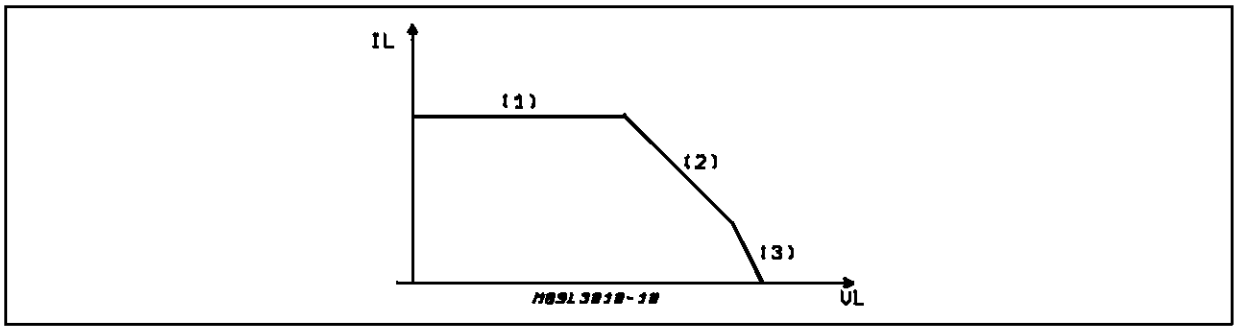


Figure 9: L303X DC Characteristic.



The R0 and KDC values depends on the working point on DC characteristic, in particular:

R0 = infinite ; KDC = 5 for region 1

R0 = 0 ; KDC = 5 for region 2

R0 = 0 ; KDC = 0 for region 3

CAC is a large capacitor (typ. 4.7µF) used to split AC and DC components of line current.

CCOMP and CH are small capacitors (typ.220pF) used to guarantee loop stability and good THL performances.

CAC, CCOMP and CH values are chosen in order to have a neglectible effect on speech band signals, therefore supposing CCOMP equivalent to an open circuit and CAC to a short circuit the following relation ships can be easily obtained from the circuit diagram of fig. 5.1.

5.1. SLIC IMPEDANCE AT LINE TERMINATIONS:

$$ZS = \frac{V_L}{I_S}\Bigg|_{VRX=0} = (ZAC/50) + 2 \times RP$$

5.2. RECEIVING GAIN :

$$G_R = \frac{V_L}{V_{RX}} = 2 \cdot \frac{ZL}{ZL + ZS}$$

therefore if ZL = ZS

$G_R = 1$

5.3. SENDING GAIN

$$G_S = \frac{V_{TX}}{V_L}\Bigg|_{VRX=0} = 0.5 \cdot \left(\frac{ZAC + RS}{ZAC + (50 \cdot 2RP)}\right)$$

therefore if RS = 50 · 2RP

$G_S = 1$

5.4. TRANS-HYBRID LOSS

$$THL = \frac{V_{TX}}{V_{RX}} = \frac{ZL + 2 \cdot RP - (RS/50)}{ZL + ZS} - \frac{ZB}{ZA + RA + ZB}$$

therefore if RS = 50 · 2RP and (ZA+RA)/ZB = ZS/ZL

THL = 0

5.5. TTX GAIN

Let's define ZL_{TTX} = line impedance at TTX frequency

$Z_{TTX} = R_{TTX} + \frac{1}{j\,\omega\,C_{TTX}}$: impedance of the TTX filter (R_{TTX} in series with C_{TTX}) at TTX frequency.

K = 2.325 TTX buffer gain.

From the block diagram of fig. 8 the TTX gain become:

$$G_{TTX} = \frac{V_L}{V_{TTX}} = 2K \cdot G \cdot \left(\frac{ZL_{TTX}}{ZL_{TTX} + 2Rp}\right) \cdot V_{TTX} \quad (1)$$

The residual at TX output is:

$$V_{TXres} = K \cdot (1 - G) \left(\frac{ZAC + RS}{ZAC}\right) \cdot V_{TTX} \qquad (2)$$

Where

$$G = \frac{\left[\frac{1 + ZAC}{(K \cdot Z_{TTX})}\right]}{1 + \frac{ZAC}{[(ZL_{TTX} + 2Rp) \cdot 50]}}$$

The optimum TTX filter is obtained for G = 1 that means

$$Z_{TTX} = 50(ZL_{TTX} + 2Rp) / K$$

In this case the (1) and (2) become:

$$G_{TTX} = 2K \cdot \left[\frac{ZL_{TTX}}{ZL_{TTX} + ZRp}\right]$$

$V_{TXres} = 0$

If you need a more careful evaluation of AC performances you can include also the effect of CCOMP and CAC in the above relations or you can simulate the system behavior with SPICE or other circuit simulators (see example at par. 7).

6. ONE EXAMPLE OF SPICE SIMULATION WITH L3000N/L3092 SLIC KIT

Figure 10: Circuit Diagram for L3000N/L3092 SLIC KIT ASpice Simulation.

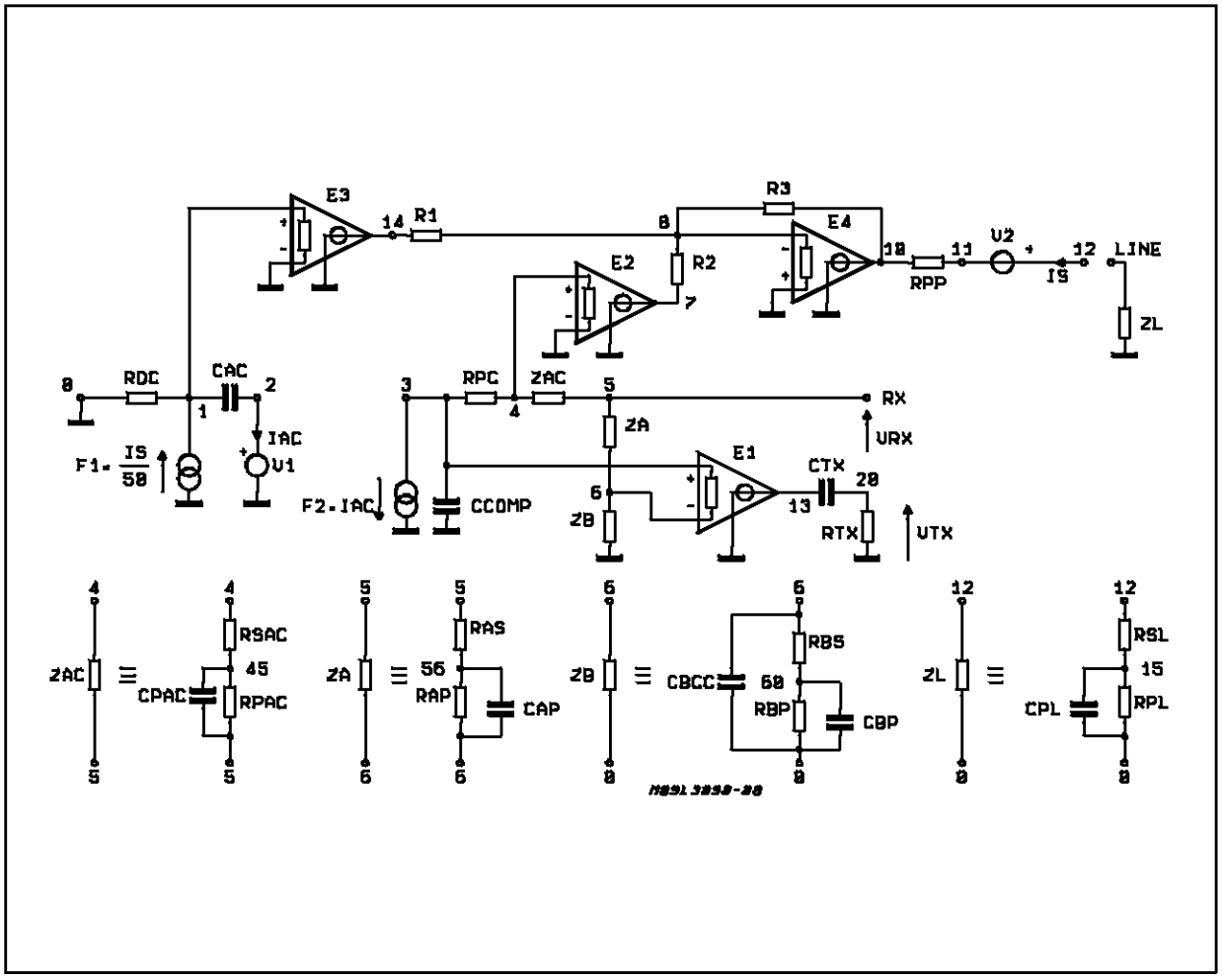
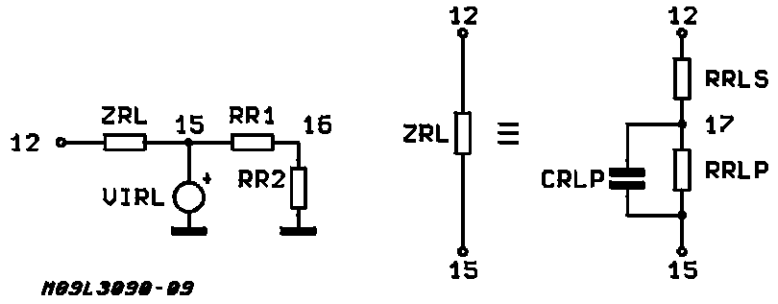
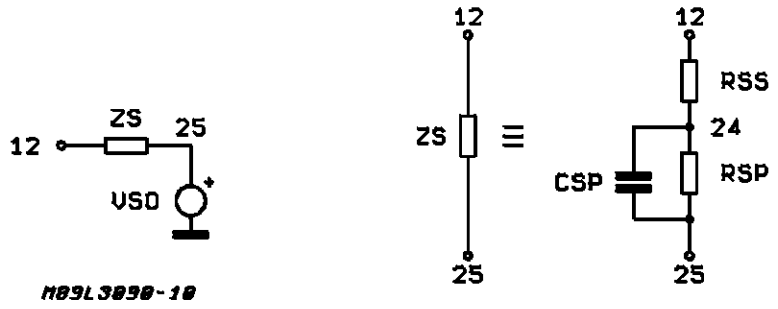


Figure 11: Network for RL Evaluation; ZRL = Return Loss Test Impedance.



$$RL = 20\log_{10}\left|\frac{ZRL - ZML}{ZRL + ZML}\right| = 20\log_{10}\left|\frac{2 \times V(12,16)}{VIRL}\right|$$

Figure 12: Network for TX Gain Evaluation with Sending Generator Series Impedance Equal to ZS.



$$G_S = 2 \times VTX/VSO$$

SPICE INPUT FILE FOR L3000N/L3092 SLIC KIT SIMULATION

```
L3092 AC ANALYSIS

********** CIRCUIT CONFIGURATION USED **********
*  PROT. RES. 2x50 OHM -- RPP = 100 OHM; RPC=2.5KOHM      *
*  FEEDING RES. 2x200 OHM -- RDC = 300 OHM                *
*  AC LINE IMPEDANCE 600 OHM -- RZAC = 12.5KOHM           *
*  (SAME CONFIGURATION AS L3000N/L3092 TEST CIRCUIT)      *
*********************************************************************

********** EXTERNAL COMPONENTS ********************************

RPC 3 4 2.5K
RSAC 4 45 .5K
RPAC 45 5 12K
*CPAC 45 5 1P
RAS 5 56 6K
RAP 56 6 6K
*CAP 56 6 1P
RBS 6 60 6K
RBP 60 0 6K
*CBP 60 0 1P
CBCC 6 0 470P
RPP 10 11 100
RTX 20 0 1MEG

CAC 1 2 47U
CCOMP 3 0 390P
CTX 13 20 10U

********** END EXT. COMPONENTS ******************************

********** MODEL COMPONENTS ***********************************
R1 14 8 1K
R2 7 8 1K
R3 8 10 40K
R4 8 0 10MEG

E1 13 0 3 6 1
E2 7 0 4 0 +.05
E3 14 0 1 0 -1.25
E4 10 0 8 0 -1MEG

V1 2 0
V2 12 11
```

```
F1 0 1 V2 .02
F2 3 0 V1 1

.AC LIN 40 100 4K
*.AC DEC 10 10 20K
.WIDTH IN=80 OUT=80

****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING *******
****** ON THE DC CHARACTERISTIC REGION                  *******
*** LIM CURRENT REGION ***********
* RDC 1 0 10MEG
*** END LIM REGION ***************

*** RES. FEED REGION *************
* RDC 1 0 300
*** END RES. REGION **************

****** INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING *******
****** ON WHICH ANALYSIS YOU WANT                       *******

*** TX GAIN EVALUATION VTX/VL WITH VRX = 0 ***
*VRX 5 0 DC 0
*VL 12 0 AC
*.PRINT AC VDB(20) VP(20)
*.PLOT AC VDB(20) VP(20)
* .STORE AC VDB(20) VP(20)
*** END TX GAIN ***********************************

*** TX GAIN EVALUATION 2VTX/VSO WITH VRX=0 ***
*** (SERIES IMP. OF SENDING GENERATOR = ZS)***
* VRX 5 0 DC 0
* VSO 25 0 AC 2
* RSS 24 12 300
* RSP 24 25 300
** CSP 24 25 1P
* .PRINT AC VDB(20) VP(20)
* .PLOT AC VDB(20) VP(20)
* .STORE AC VDB(20) VP(20)
*** END TX GAIN ***********************************

*** RX GAIN EVALUATION VL/VRX ****************
* RSL 12 15 300
* RPL 15 0 300
** CPL 15 0 1P
* VRX 5 0 AC
* .PRINT AC VDB(12) VP(12)
```

```
* .PLOT AC VDB(12) VP(12)
* .STORE AC VDB(12) VP(12)
*** END RX GAIN ******************************

*** THL EVALUATION VTX/VRX ******************
* RSL 12 15 300
* RPL 15 0 300
** CPL 15 0 1P
* VRX 5 0 AC
* .PRINT AC VDB(20) VP(20)
* .PLOT AC VDB(20) VP(20)
* .STORE AC VDB(20) VP(20)
*** END THL EVALUATION ***********************

*** RETURN LOSS EVALUATION *******************
* VRX 5 0 DC 0
* VIRL 15 0 AC 2
* RCS 12 17 300
* RCP 17 15 300
** CCP 17 15 1P
* RR1 15 16 1K
* RR2 16 0 1K
* .PRINT AC VDB(12,16)
* .PLOT AC VDB(12,16)
* .STORE AC VDB(12,16)
*** END RETURN LOSS EVALUATION ***************

*** INPUT IMPEDANCE EVAL. AT LINE TERMINALS **
* VRX 5 0 DC 0
* IL 0 12 AC
* .PRINT AC VM(12) VP(12)
* .PLOT AC VM(12) VP(12)
* .STORE AC VM(12) VP(12)
*** END INPUT IMPED. EVALUATION **************

.END
```

7. ONE EXAMPLE OF SPICE SIMULATION WITH L303X MONOCHIP SLIC.

Figure 13: Circuit Diagram for L303X Monochip SLIC SPICE Simulation.

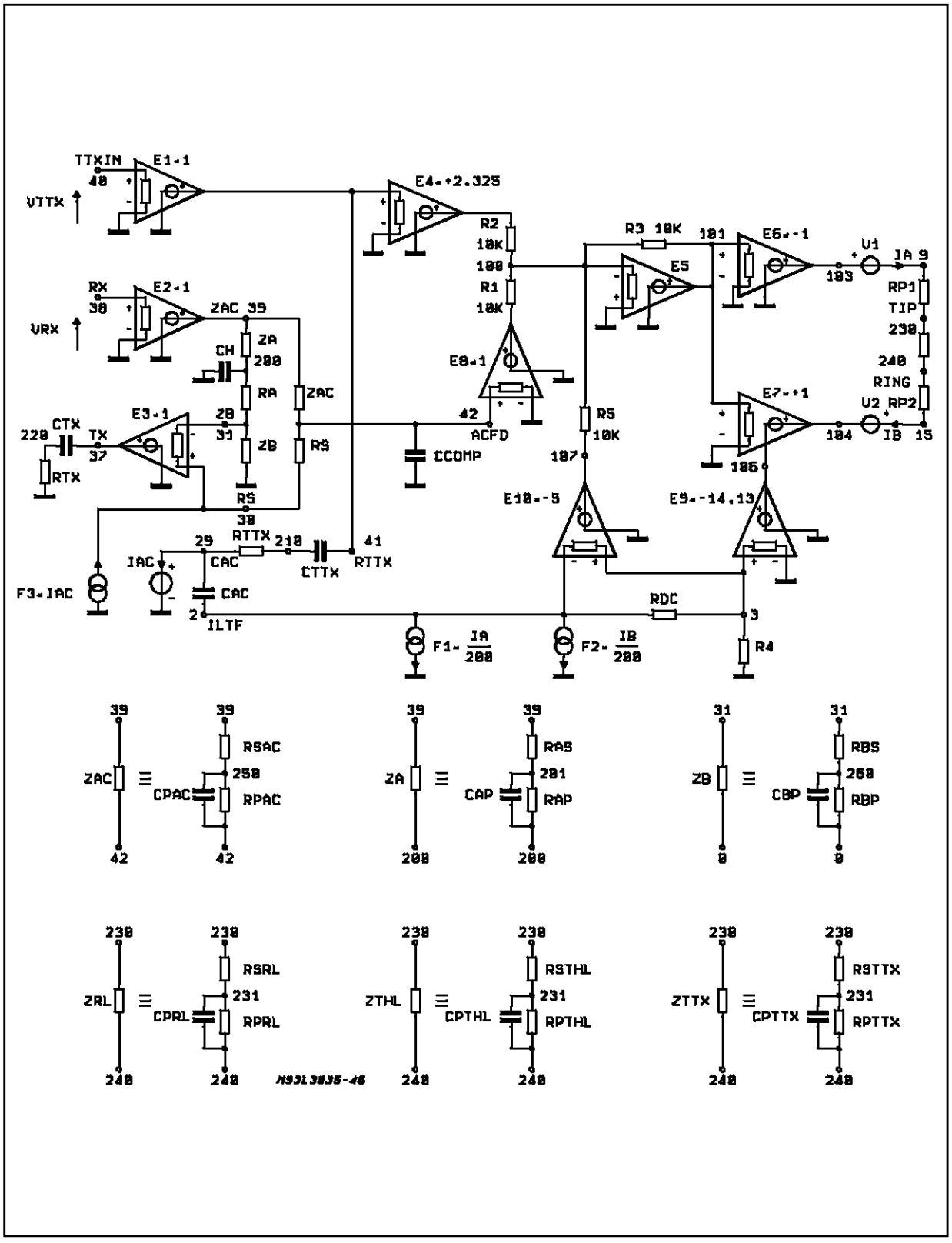
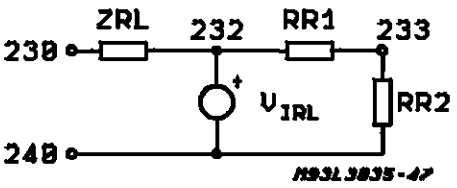
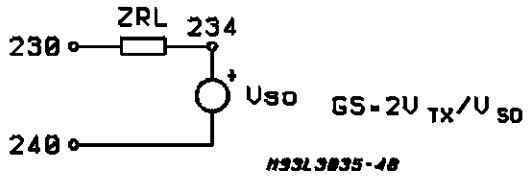


Figure 14: Network for RL Evaluation; ZRL = Return Loss Test Impedance.



$$RL = 20LOG_{10}\left|\frac{Z_{RL}-Z_S}{Z_{RL}+Z_S}\right| = 20LOG_{10}\left|\frac{2 \times V(230,233)}{V_{IRL}}\right|$$

Figure 15: Network for TX Gain Evaluationwith Sending Generator Series Impedance Equal to ZRL.



SPICE INPUT FILE FOR L303X SLIC SIMULATION

```
L303X MONOCHIP SLIC AC ANALYSIS

************************************DEFAULT CIRCUIT CONFIGURATION ************************************
*  PROT RESISTOR 2x40ohm -- RP1=RP2=40ohm -- RS=4Kohm                                                *
*  FEEDING RESISTANCE 400ohm -- RDC=3.2Kohm                                                          *
*  RETURN LOSS IMPEDANCE 600ohm -- ZAC=26Kohm                                                        *
*  TRANS HYBRID LOSS IMPEDANCE 600ohm -- RA=4Kohm, ZA=26Kohm, ZB=30Kohm                              *
*  (SAME CONFIGURATION AS L3036 TEST CIRCUIT)                                                        *
*****************************************************************************************************************

********** SLIC EXTERNAL COMPONENTS (SHOULD MATCH WITH THE APPLICATION )**********

RP1 9 230 40
RP2 15 240 40
RS 42 30 4K
RA 200 31 4K
RDC 2 3 3.2K
RTTX 29 210 6.34K
RTX 220 0 1MEG
RITTX 40 0 10MEG
RIRX 38 0 10MEG
RIZB 31 30 10MEG

CAC 2 29 4.7U
CCOMP 42 0 220P
CH 200 0 220P
CTTX 41 210 5.6N
CTX 37 220 100N

******** ZAC ********
RSAC 39 250 13K
RPAC 250 42 13K
*CPAC 250 42 4.4N
**********************

********* ZA *********
RAS 39 201 13K
RAP 201 200 13K
*CAP 201 200 4.4N
**********************

********* ZB *********
RBS 31 260 15K
RBP 260 0 15K
```

```
*CBP 260 0 4.4N
**********************************************

**** RETURN LOSS IMPEDANCE ******
.SUBCKT ZRL 1 2
RSRL 1 3 300
RPRL 3 2 300
*CPRL 3 2 220N
.ENDS
**********************************************

********** THL IMPEDANCE **************
.SUBCKT ZTHL 1 2
RSTHL 1 3 300
RPTHL 3 2 300
*CPTHL 3 2 220N
.ENDS
**********************************************

********** TTX LINE IMPEDANCE *******
.SUBCKT ZTTX 1 2
RSTTX 1 3 216
*RPTTX 3 2 200
CPTTX 3 2 120N
.ENDS
**********************************************


**********END SLIC EXTERNAL COMPONENTS ************************************


************************** MODEL COMPONENTS (SHOULD NOT BE MODIFIED) ************************

R1 100 105 10K
R2 100 102 10K
R3 100 101 10K

E1 41 0 40 0 1
E2 39 0 38 0 1
E3 37 0 30 31 1
E4 102 0 41 0 2.325
E5 101 0 100 0 -10MEG
E6 103 0 101 0 -1
E7 104 106 101 0 1
E8 105 0 42 0 1
E9 106 0 3 0 -14.13
```

```
V1 103 9
V2 15 104
V3 29 0

F1 2 0 V1 .005
F2 2 0 V2 .005
F3 0 30 V3 1

*.AC LIN 40 100 4K
.WIDTH IN=80 OUT=80

****************************************END MODEL COMPONENTS ***************************************


******* INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ON THE ***********
******* DC CHARACTERISTIC REGION                                  ***********

******** LIMITING CURRENT REGION ******************
*R4 3 0 1MEG
******** END LIMITING REGION ********     ***************

************* CONST VOLTAGE REGION *****************
*R4 3 0 1M
************* END CONST VOLTAGE REGION *************

**** RESISTIVE FEED REGION (NOT ALWAYS PRESENT) ****
*R4 3 0 1M
*R5 107 100 10K
*E10 107 0 3 2 -5
*********** END RESISTIVE FEED REGION **************

******* INSERT ONLY ONE OF THE FOLLOWING BLOCKS DEPENDING ON ***************
******* WHICH ANALYSIS YOU WANT                               ***************

******* TX GAIN EVALUATION VTX/VL WITH VRX=0 ********************
* VRX 38 0 DC 0
* VTTX 40 0 DC 0
* VL 230 240 AC
* .AC LIN 40 100 4K
* .PRINT AC VDB(220) VP(220)
* .PLOT AC VDB(220) VP(220)
* .PROBE AC V(220)
******* END TX GAIN *********************************************

******* TX GAIN EVALUATION 2VTX/VSOL WITH VRX=0 *****************
*VRX 38 0 DC 0
```

```
*VTTX 40 0 DC 0
*VSO 234 240 AC 2
*XZRL 230 234 ZRL
*.AC LIN 40 100 4K
*.PRINT AC VDB(220) VP(220)
*.PLOT AC VDB(220) VP(220)
*.PROBE AC V(220)
******** END TX GAIN ***************************************************

******** RX GAIN EVALUATION VL/VRX ********************************
*VTTX 40 0 DC 0
*XZRL 230 240 ZRL
*VRX 38 0 AC
*.AC LIN 40 100 4K
*.PRINT AC VDB(230,240) VP(230,240)
*.PLOT AC VDB(230,240) VP(230,240)
*.PROBE AC V(230,240)
******** END RX GAIN ****************************************************

******** THL EVALUATION VTX/VRX ***********************************
*VTTX 40 0 DC 0
*XZTHL 230 240 ZTHL
*VRX 38 0 AC
*.AC LIN 40 100 4K
*.PRINT AC VDB(220) VP(220)
*.PLOT AC VDB(220) VP(220)
*.PROBE AC V(220)
******** END THL EVALUATION ***************************************

******** RETURN LOSS EVALUATION ***********************************
*VTTX 40 0 DC 0
*VRX 38 0 DC 0
*XZRL 230 232 ZRL
*RR1 232 233 1K
*RR2 233 240 1K
*VIRL 232 240 AC 2
*.AC LIN 40 100 4K
*.PRINT AC VDB(230,233)
*.PLOT AC VDB(230,233)
*.PROBE AC V(230,233)
******** END RETURN LOSS EVALUATION ************************************

******** INPUT IMPEDANCE EVALUATION AT LINE TERMINALS ***********
*VTTX 40 0 DC 0
*VRX 38 0 DC 0
*IL 240 230 AC
```

```
*.AC LIN 40 100 4K
*.PRINT AC VM(230,240) VP(230,240)
*.PLOT AC VM(230,240) VP(230,240)
*.PROBE AC V(230,240)
******** END INPUT IMPEDANCE EVALUATION **************************

******** TTX GAIN EVALUATION VL/VTTXIN *******************************
*VRX 38 0 DC 0
*XZTTX 230 240 ZTTX
*VTTXIN 40 0 AC 1
*.AC LIN 2 12K 16K
*.PRINT AC VM(230,240) VP(230,240)
*.PLOT AC VM(230,240) VP(230,240)
*.PROBE AC V(230,240)
******** END TTX GAIN ************************************************

******** TTX CANCELLATION VTX/VTTXIN *****************************
*VRX 38 0 DC 0
*XZTTX 230 240 ZTTX
*VTTXIN 40 0 AC 1
*.AC LIN 2 12K 16K
*.PRINT AC VM(220) VP(220)
*.PLOT AC VM(220) VP(220)
*.PROBE AC V(220)
******** END TTX CANCELLATION ***************************************

.END
```