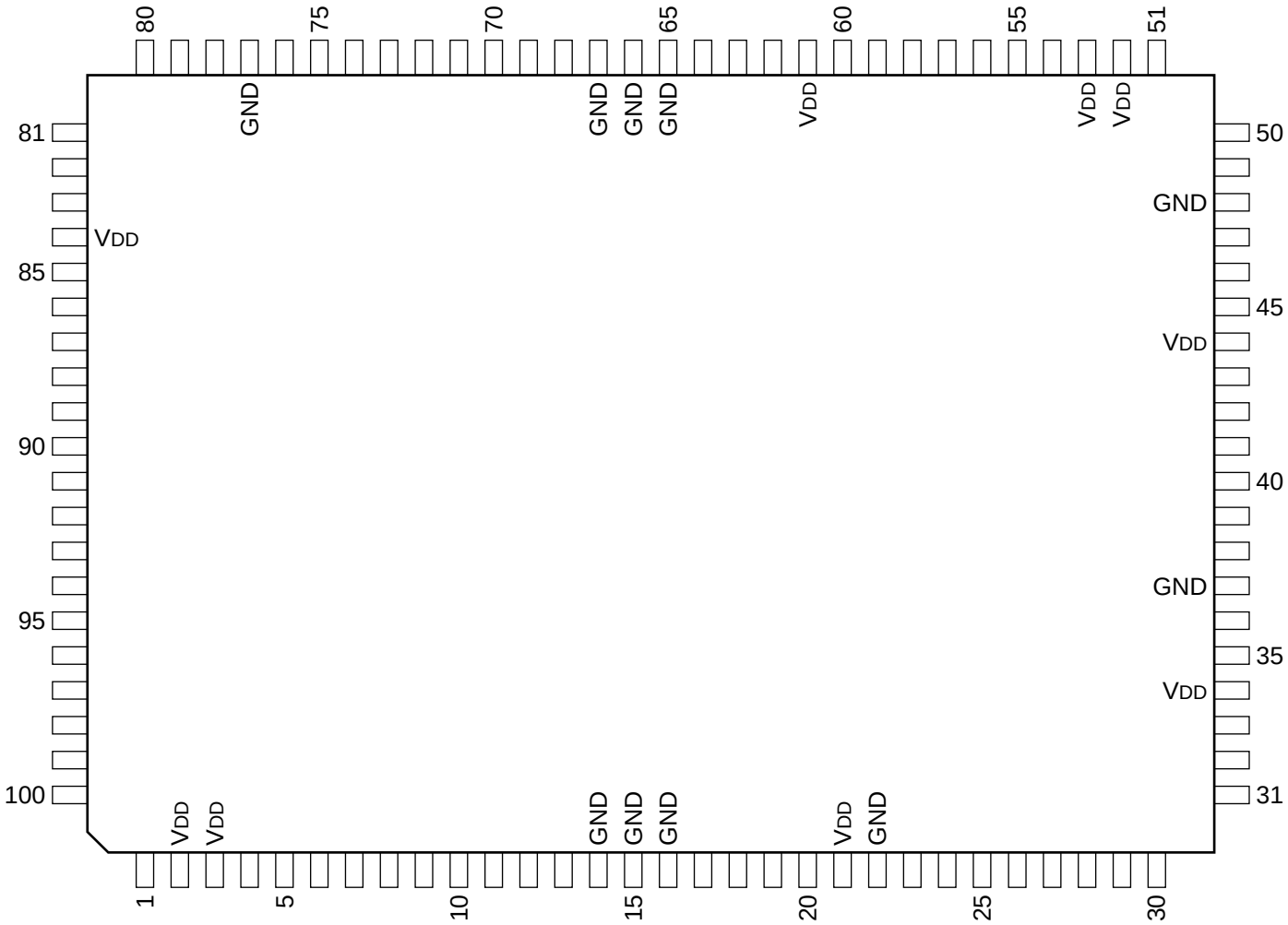
C-MOS HIGH SPEED 8-BIT MPU

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	P33/OUTBP2	26	I	MODE1	51	I/O	D7	76	I/O	P12/GATEA1
2	—	V_{DD}	27	I	MODE0	52	—	V_{DD}	77	—	GND
3	—	V_{DD}	28	I	ERDY	53	—	V_{DD}	78	I/O	P11/XCLK0
4	I/O	P32/OUTBP1	29	I	RXD	54	I/O	D6	79	I/O	P10/GATEA0
5	I/O	P31/SYNC	30	O	TXD	55	I/O	D5	80	I/O	P07/IR7
6	I/O	P30/OUTBS0	31	O	A15	56	I/O	D4	81	I/O	P06/IR6
7	O	$\overline{\text{EMRD}}$	32	O	A14	57	I/O	D3	82	I/O	P05/IR5
8	O	$\overline{\text{EMWR}}$	33	O	A13	58	I/O	D2	83	I/O	P04/IR4
9	O	$\overline{\text{EIORD}}$	34	—	V_{DD}	59	I	$\overline{\text{RESET}}$	84	—	V_{DD}
10	O	$\overline{\text{EIOWR}}$	35	O	A12	60	I/O	D1	85	I/O	P03/IR3/$\overline{\text{NMI}}$
11	I/O	P27	36	O	A11	61	—	V_{DD}	86	I/O	P02/IR2/GATEB2
12	I/O	P26	37	—	GND	62	I/O	D0	87	I/O	P01/IR1/GATEB1
13	I/O	P25	38	O	A10	63	I	XIN	88	I/O	P00/IR0/GATEB0
14	—	GND	39	O	A9	64	O	XOUT	89	I/O	P47/SYNDBD
15	—	GND	40	O	A8	65	—	GND	90	I/O	P46/$\overline{\text{RTS}}$
16	—	GND	41	O	A7	66	—	GND	91	I/O	P45/$\overline{\text{DTR}}$
17	I/O	P24	42	O	A6	67	—	GND	92	I/O	P44/$\overline{\text{BACK}}$
18	I/O	P23	43	O	A5	68	O	A18/$\overline{\text{M1CS}}$	93	I/O	P43/SYDTIN
19	I/O	P22	44	—	V_{DD}	69	O	A17/$\overline{\text{M0CS}}$	94	I/O	P42/$\overline{\text{CTS}}$
20	I/O	P21	45	O	A4	70	O	A16	95	I/O	P41/$\overline{\text{DSR}}$
21	—	V_{DD}	46	O	A3	71	I/O	P17/$\overline{\text{HALT}}$	96	I/O	P40/$\overline{\text{BREQ}}$
22	—	GND	47	O	A2	72	I/O	P16/$\overline{\text{M1}}$	97	I/O	P37/OUTBS2
23	I/O	P20	48	—	GND	73	I/O	P15/RXC	98	I/O	P36/OUTBP0
24	O	CLK	49	O	A1	74	I/O	P14/TXC	99	I/O	P35/OUTA1
25	I/O	BFSIO	50	O	A0	75	I/O	P13/XCLK1	100	I/O	P34/OUTA0

INPUT

$\overline{\text{BREQ}}$	:	BUS REQUEST FOR CPU
$\overline{\text{CTS}}$	:	CLEAR-TO-SEND SIGNAL FOR USART
$\overline{\text{DSR}}$	:	DATA SET READY SIGNAL FOR USART
ERDY	:	WAIT REQUEST FROM THE EXTERNAL DEVICE
GATEA0	:	GATE INPUT FOR COUNTER A CHANNEL 0
GATEA1	:	GATE INPUT FOR COUNTER A CHANNEL 1
GATEB0	:	GATE INPUT FOR COUNTER B CHANNEL 0
GATEB1	:	GATE INPUT FOR COUNTER B CHANNEL 1
GATEB2	:	GATE INPUT FOR COUNTER B CHANNEL 2
IR0 - IR7	:	EXTERNAL INTERRUPT INPUT LEVEL
MODE0, MODE1	:	MODE SELECT
$\overline{\text{NMI}}$	:	NON-MASKABLE INTERRUPT FOR CPU
$\overline{\text{RESET}}$	:	RESET
RXC	:	RECEIVE CLOCK FOR USART
RXD	:	SERIAL DATA FOR USART
SYDTIN	:	EXTERNAL SYNC DETECT SIGNAL FOR USART
TXC	:	TRANSMIT CLOCK FOR USART
XCLK0	:	EXTERNAL COUNTER CLOCK FOR COUNTER A CHANNEL0
XCLK1	:	EXTERNAL COUNTER CLOCK FOR COUNTER A CHANNEL1
XIN	:	EXTERNAL CRYSTAL OSCILLATOR

OUTPUT

A0 - A18	:	ADDRESS
$\overline{\text{BACK}}$	:	BUS ACKNOWLEDGE FOR CPU
CLK	:	CLOCK
$\overline{\text{DTR}}$	:	DATA TERMINAL READY FOR USART
$\overline{\text{EIORD}}$	:	EXTERNAL I/O DEVICE READ SIGNAL
$\overline{\text{EIOWR}}$	:	EXTERNAL I/O DEVICE WRITE SIGNAL
$\overline{\text{EMRD}}$	:	EXTERNAL MEMORY READ SIGNAL
$\overline{\text{EMWR}}$	:	EXTERNAL MEMORY WRITE SIGNAL
$\overline{\text{HALT}}$	:	CPU HALT SIGNAL
$\overline{\text{M0CS}}$	:	CHIP SELECT FOR EXTERNAL ROM
$\overline{\text{M1}}$	:	M1 CYCLE FOR CPU
$\overline{\text{M1CS}}$	:	CHIP SELECT FOR EXTERNAL RAM/ROM
OUTA0	:	COUNTER A CHANNEL 0
OUTA1	:	COUNTER A CHANNEL 1
OUTBP0	:	PULSE FOR COUNTER B CHANNEL 0
OUTBP1	:	PULSE FOR COUNTER B CHANNEL 1
OUTBP2	:	PULSE FOR COUNTER B CHANNEL 2
OUTBS0	:	STROBE FOR COUNTER B CHANNEL 0
OUTBS2	:	STROBE FOR COUNTER B CHANNEL 2
$\overline{\text{RTS}}$	:	REQUEST-TO-SEND SIGNAL
SYNC	:	SYNC SIGNAL FOR PRE-SCALAR OF COUNTER B
SYNDBD	:	SYNC DETECT SIGNAL/BREAK DETECT SIGNAL FOR USART
TXD	:	SERIAL DATA FOR USART
XOUT	:	EXTERNAL CRYSTAL OSCILLATOR

INPUT/OUTPUT

BFSIO	:	BUG FINDER PORT
D0 - D7	:	EXTERNAL DATA BUS
P00 - P07	:	P0 PORT OF PARALLEL PORT BLOCK A
P10 - P17	:	P1 PORT OF PARALLEL PORT BLOCK A
P20 - P27	:	P0 PORT OF PARALLEL PORT BLOCK B
P30 - P37	:	P1 PORT OF PARALLEL PORT BLOCK B
P40 - P47	:	P2 PORT OF PARALLEL PORT BLOCK B