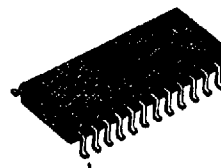


LEAD BATTERY CHARGE CONTROLLER

The KA7560 is a IC for charging control of lead battery. Charging current is controlled by detecting voltage difference between battery ports.

24-SOP-375



FEATURES

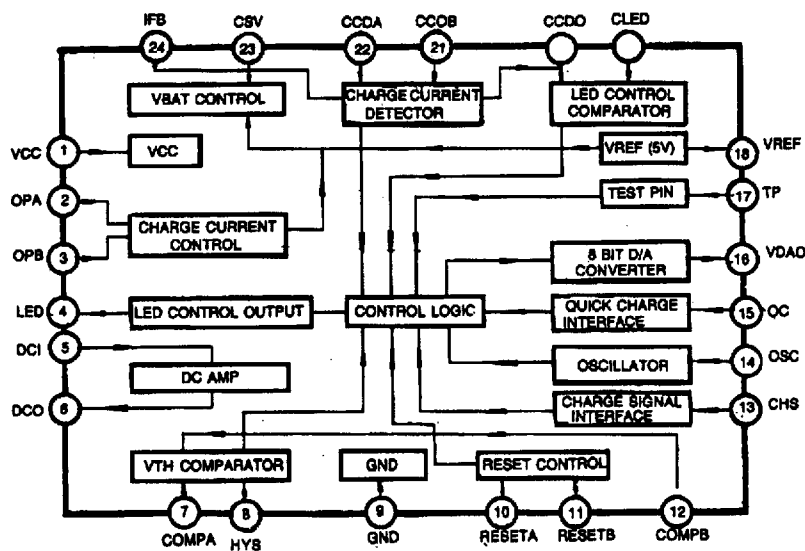
- Charging current linearly decreases when battery charging ends, by detecting battery voltage.
- Charging time is possible in about 1 hour (It can be changed by battery condition)
- Charging current ($I_{CHG(MAX)}$) can be adjusted by selecting external resistor value properly.

ORDERING INFORMATION

Device	Package	Operating Temperature
KA7560G	Chip	
KA7560D	24-SOP-375	-20 ~ + 75°C

24 SOP: Underdevelopment

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	20	V
Supply Current	I_{CC}	33	mA
Power Dissipation	P_D	660	mW
Operating Temperature	T_{OPR}	- 20 ~ + 75	°C
Storage Temperature	T_{STG}	- 55 ~ + 150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 18V$, $T_J = 25^\circ C$)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Fig. 1	13.5	19.0	24.5	mA
Reference Voltage	V_{REF}	Fig. 1	4.4	5.0	5.5	V
Low Input Voltage	V_{IL}	Fig. 3	3.8	5.0	6.2	V
V_H Low Voltage	V_{VHL}	Fig. 2	—	0.2	0.5	V
V_H Leakage Current	I_{LKG}	Fig. 4	-12	—	12	μA
DC Voltage Gain	A_V	Fig. 5	3.36	4.0	4.64	
Oscillator Frequency	f	Fig. 6	18	20	22	Hz
LED Low Voltage	V_{LED}	Fig. 7	—	0.4	1.0	V
LED Leakage Current	$I_{LKG(LED)}$	Fig. 7	-10	—	10	μA
IFB Low Voltage	I_{IFBL}	Fig. 8	—	1.3	2.1	V
DAO High Voltage	V_{DAOH}	Fig. 10	2.5	3.6	4.9	V
DAO Low Voltage	V_{DAOI}	Fig. 10	0.05	0.13	0.25	V
Linearity	A_{V20}	Fig. 9	0.7	1.0	1.3	—
Bit 1 Voltage	ΔV_1	Fig. 10	10	13	18	mV
Bit 2 Voltage	ΔV_2	Fig. 10	20	25	37	mV
Bit 3 Voltage	ΔV_3	Fig. 10	40	54	75	mV
Bit 4 Voltage	ΔV_4	Fig. 10	80	120	150	mV
Bit 5 Voltage	ΔV_5	Fig. 10	160	240	300	mV
Bit 6 Voltage	ΔV_6	Fig. 10	320	440	600	mV
Bit 7 Voltage	ΔV_7	Fig. 10	640	880	1200	mV
Bit 8 Voltage	ΔV_8	Fig. 10	1280	1720	2400	mV

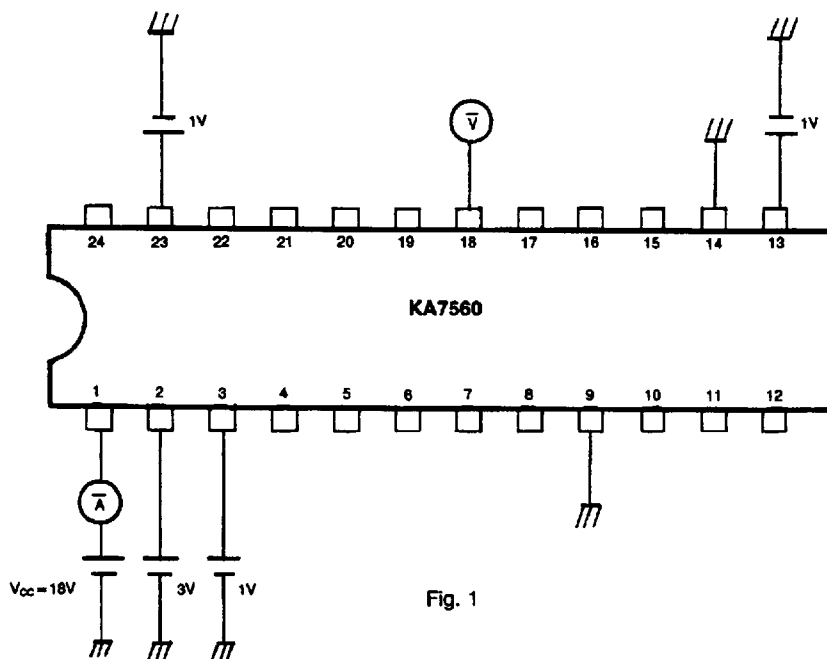


Fig. 1

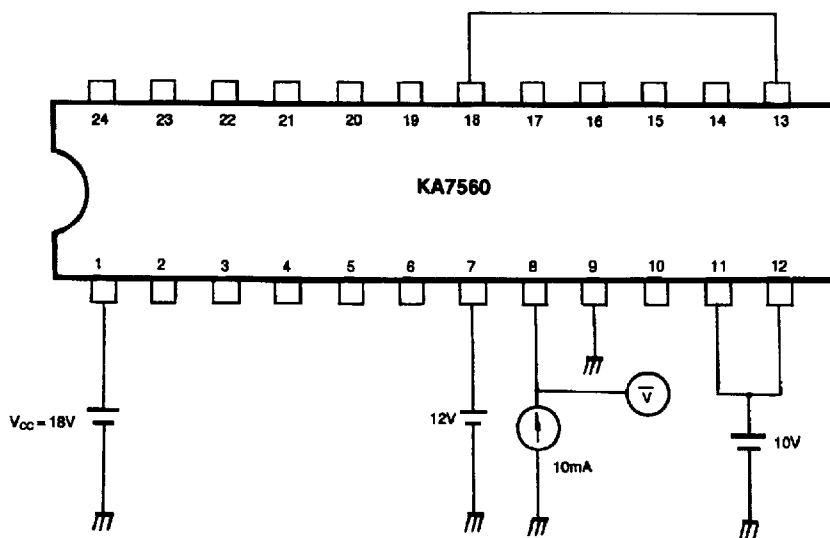


Fig. 2

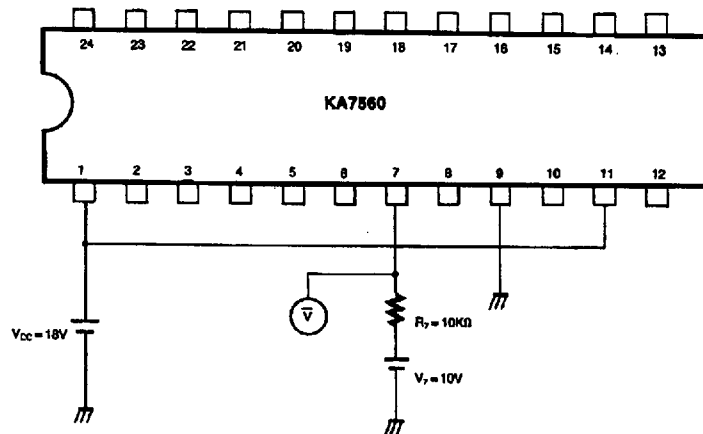
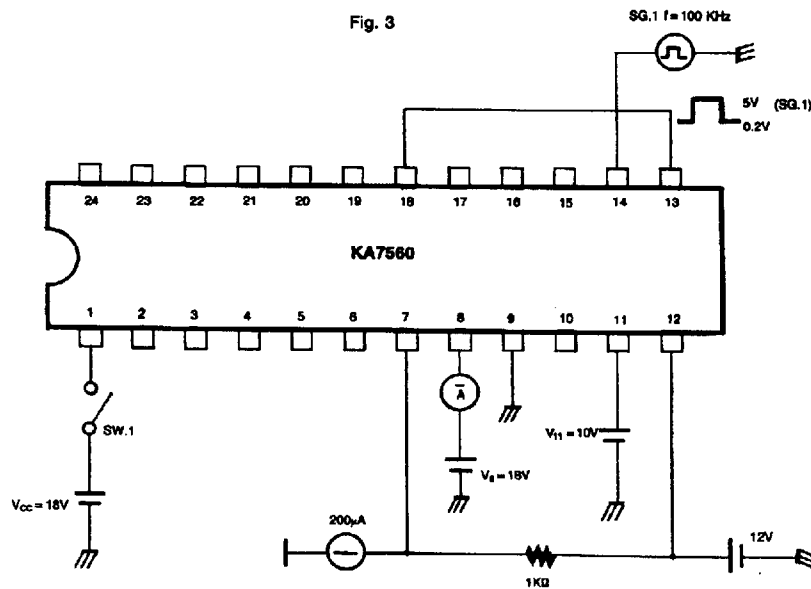


Fig. 3



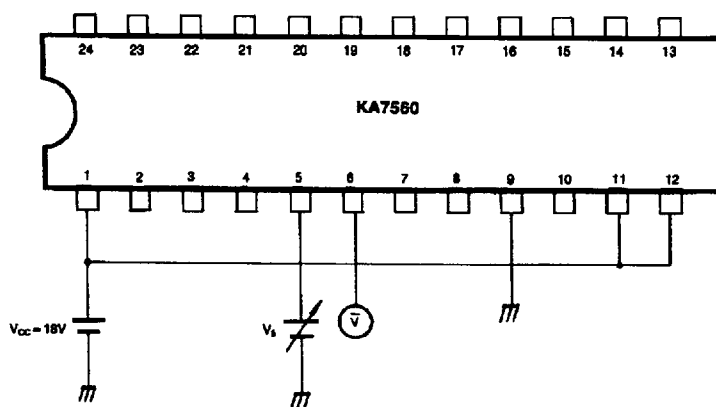


Fig. 5

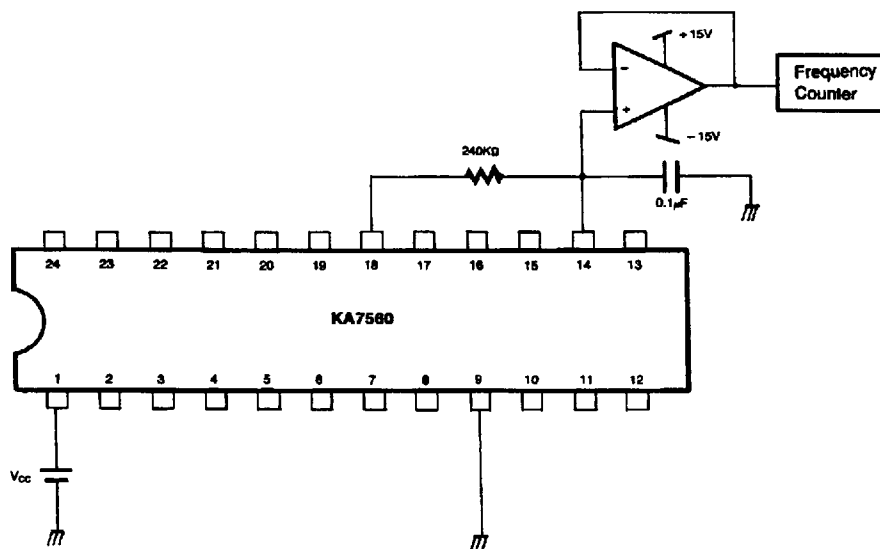


Fig. 6

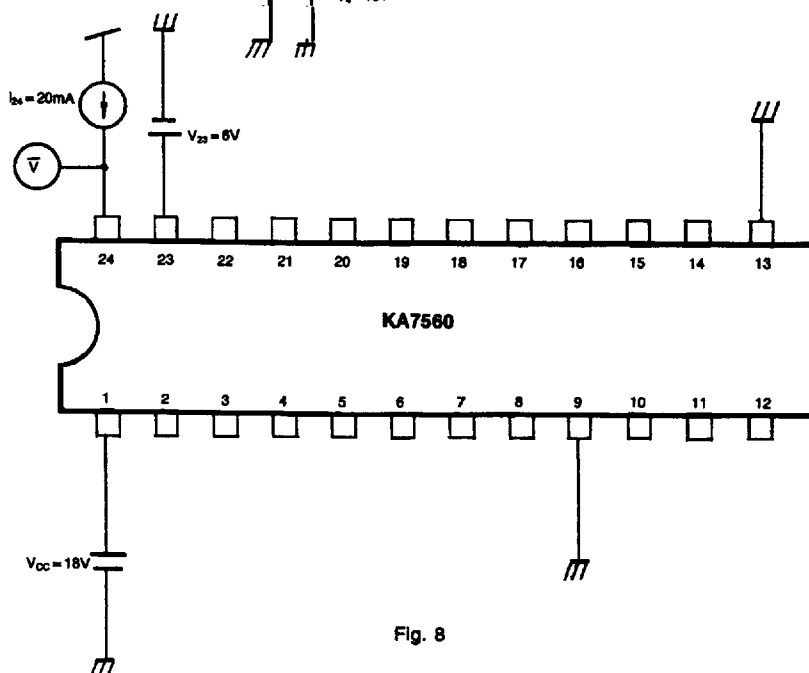
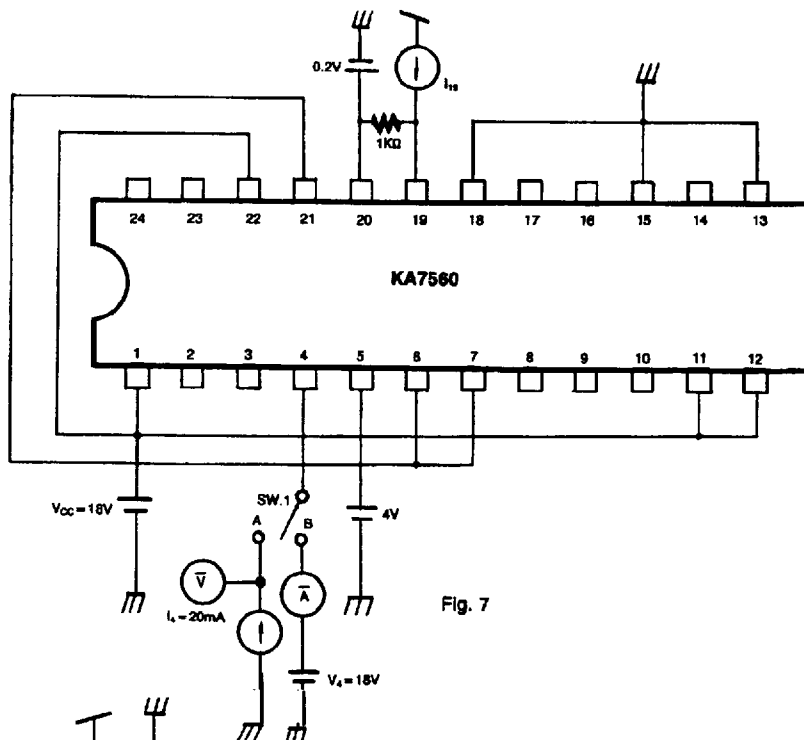
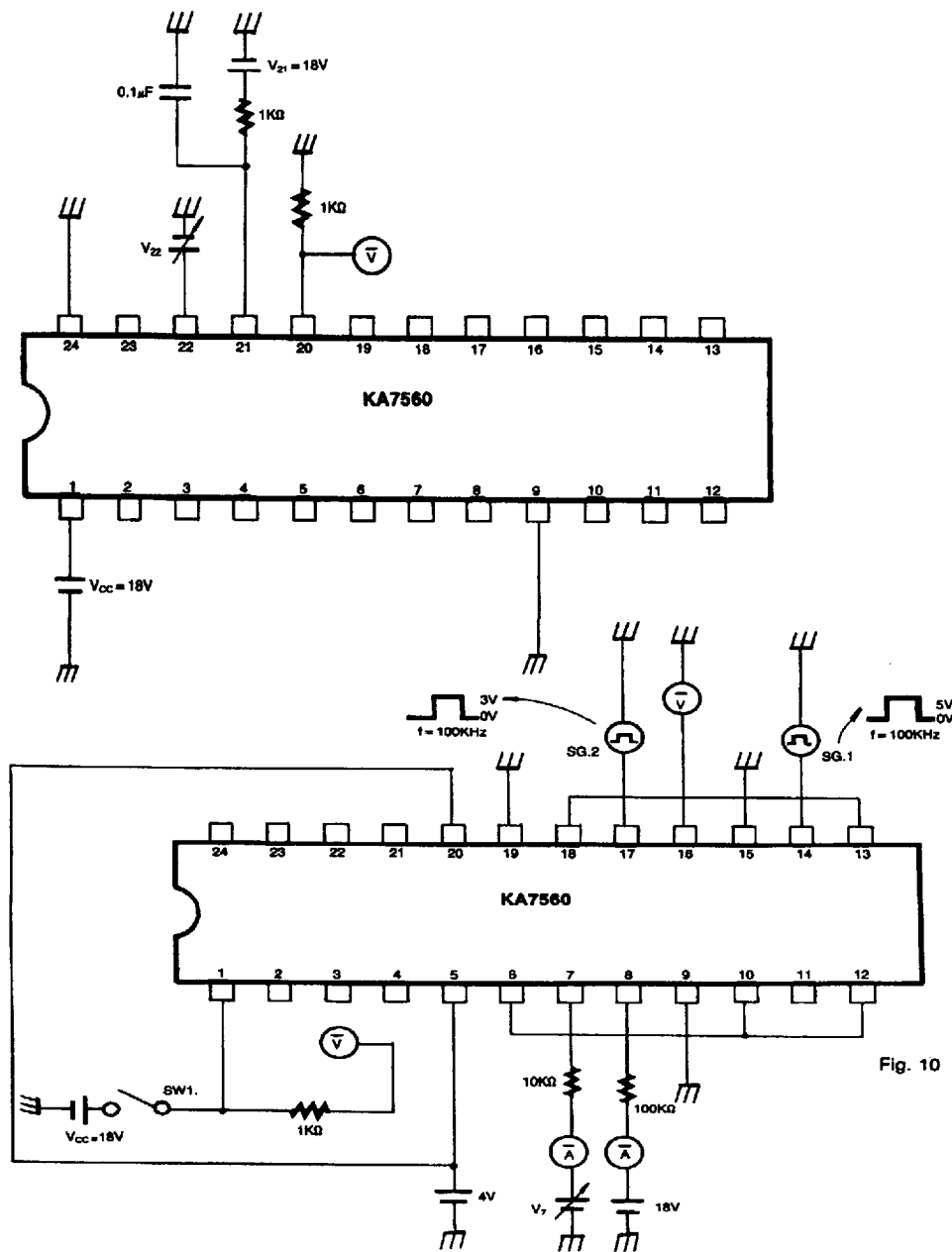


Fig. 8



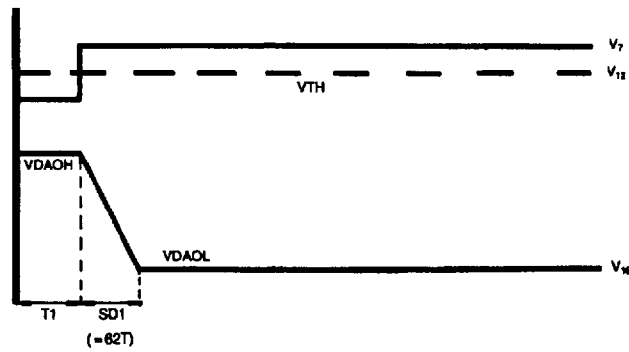


Fig. 11 $T_1 < 64T$, 5BIT STEP-DOWN

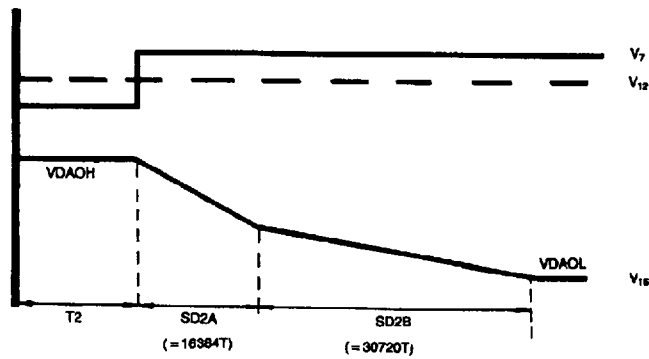
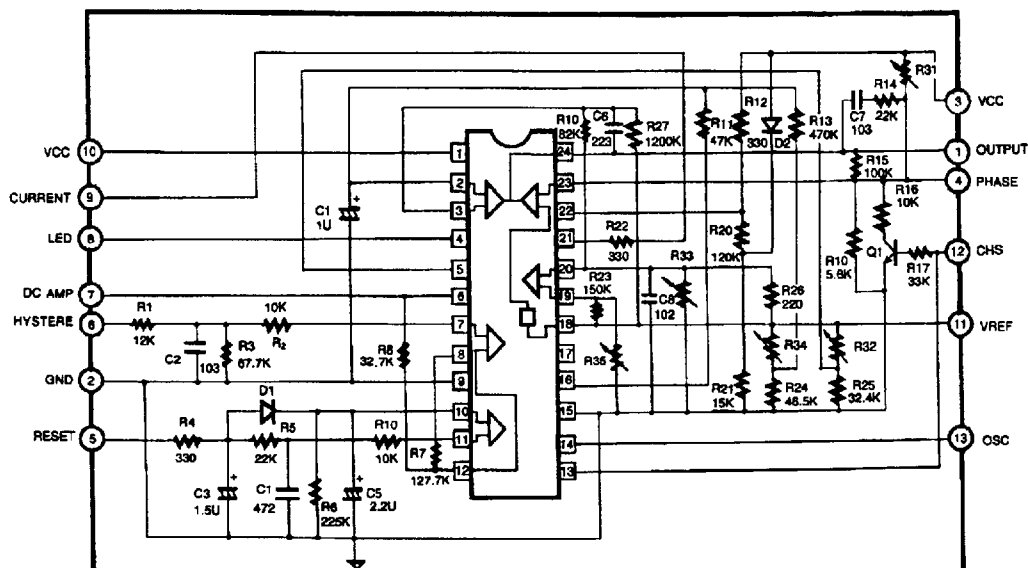
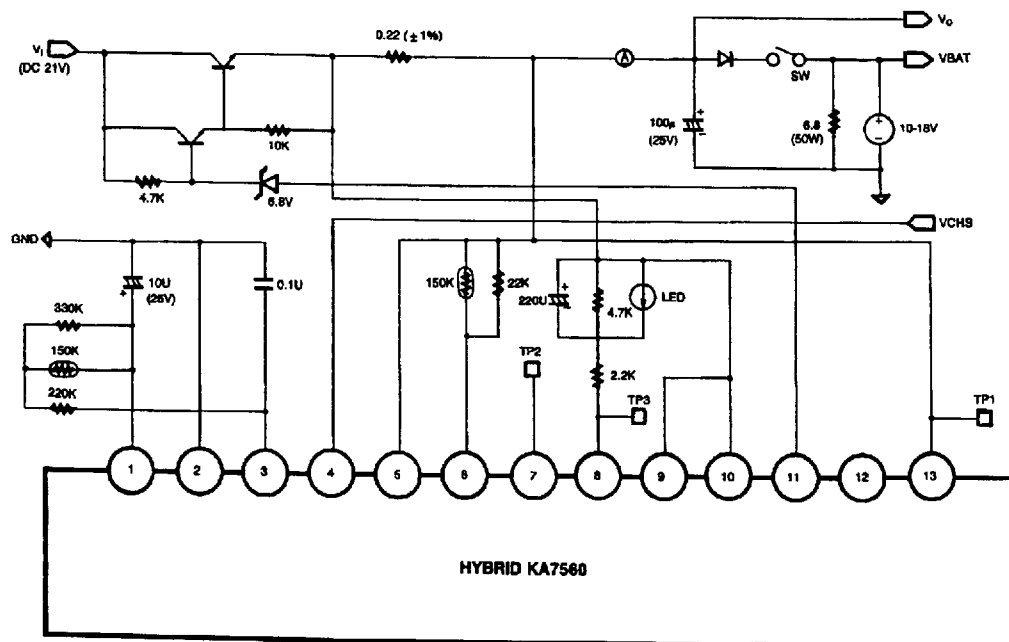


Fig. 12 $T_2 > 64T$, 8BIT STEP-DOWN ($V_{15} = GND$)

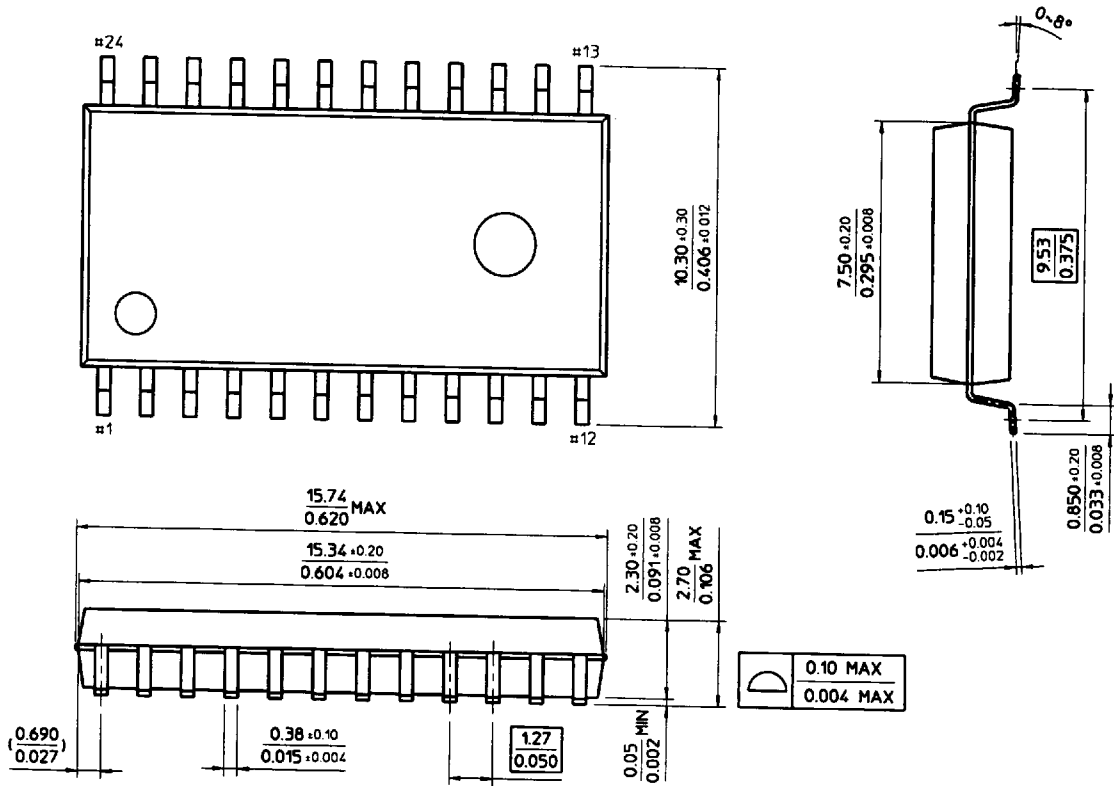
*** KA7560 Hybrid Application Example**



HYBRID KA7560 TEST & APPLICATION CIRCUIT



24-SOP-375



28-SOP-375

