A Two-Chip Receiver for Short Haul Links up to 3.5Gb/s with PIN-Preamp Module and CDR-DMUX

Jürgen Hauenschild, Dirk Friedrich, Jürgen Herrle, Joachim Krug

Siemens AG, HL HF M SL, P.O.BOX 80 17 09, D-81617 Munich, Germany,
Tel.: +49 89 636-23247 Fax.: +49 89 636-25446,
E-mail: b6hf@bipa.hl.siemens.de

Abstract:

A 3.5Gb/s two-chip receiver consisting of a preamp and a gate-array-based CDR-DMUX is fabricated in a 25GHz Si bipolar process. The preamp is mounted in the PIN-diode package. Measurements show an excess gain of >10dB if the offset of the CDR is restricted. The CDR features an SDH-compatible loss-of-signal detection. The two chips dissipate 200mW and 1500mW.

A Two-Chip Receiver for Short Haul Links up to 3.5Gb/s with PIN-Preamp Module and CDR-DMUX

Jürgen Hauenschild, Dirk Friedrich, Jürgen Herrle, Joachim Krug

Siemens AG, Semiconductor Group, Munich, Germany

Fiber optical links operating at 2.5Gb/s conventionally feature a receiver consisting of 3 or more chips. These are shown in figure 1(a) (page 3*): preamp, postamp and a clock and data recovery (CDR) possibly combined with a demultiplexer (DMUX). The three chips are AC-coupled. This enables the system designer to introduce offsets to optimize the decision level. The preamp is often realized as transimpedance amplifier with an open-loop gain around 40 and a transimpedance of 1 to 2kΩ. The postamp is clipping or gain controlled with a typical gain of 40 to 50 dB to deliver sufficiently 'digital' signal levels to the CDR. In long-haul receivers with an input sensitivity of -30 to -35dBm$_{optical}$ additional gain is provided by avalanche photo diodes (APD) or optical preamplifiers. These elements (as well as optical repeaters) require a decision level control as the mean value of the signal is not optimal.

For short-haul applications (-20 to -25dBm$_{optical}$) the non-optical chips are more cost sensitive. The 2-chip receiver depicted in figure 1(b) (page 3*) depends on a high-gain preamp and a high-sensitivity CDR-DMUX. The former postamp is effectively cut in two and now part of its former neighbors. If the high-gain preamp is integrated into the metal can of the PIN-diode (resulting in a PIN-preamp) the space saving due to this 'autoshielding' is significant. The gain bandwidth product of the amplifier is restricted by coupling inside the metal can. The sensitivity of the CDR-DMUX is possibly depending on second order effects like coupling to outputs (direct or via common mode). This article will show the necessities and limitations on gain of the proposed receiver architecture which is realized on the 25GHz bipolar Siemens B6HF process.

The block diagram of the amplifier is part of figure 1(b) (page 3*). The transimpedance resistor is 1.6kΩ with antiparallel clamp diodes to allow 0dBm optical input. Despite AC-coupling between the amplifier and the CDR-DMUX a DC-controller is implemented on chip. This loop sets the operating point of the input stage at high input levels as well as the duty cycle. It is necessary to prevent gross dc-overload of the symmetry- and the output stage with a total gain of (11.4+13.2=) 24.6dB. Fine symmetry is helpful to minimize common-mode-induced destabilizing feedback. Power supply is +4.5 to +5.0V at less than 42mA for this full custom chip. Figure 2 (page 7*) shows the optical/electrical transmission and the output reflection coefficient of the module measured differentially (reference given in [4]) and given for both outputs to verify symmetry. The eye diagrams correlate to the gain at half the bit rate ($f_b/2$) and are taken at a bit error rate (BER) of around $10^{-9\ to\ -10}$ and show an eye opening of $160mV_{pp}$ in both cases. The photograph of the TO-48 module (Figure 3 = page 6*) is taken with detached lens.

The CDR-DMUX is realized on the analog portion of a commercially available gate array and needs an external reference and opamp. It is packaged in a TQFP100 plastic package with heat slug and consumes 335mA from -4 to -5V supply. The on-chip oscillator is a 3-stage ring (figure 4 = page 10*). It features constant PLL-gain without additional delay-stages like in reference [1] even over a 2:1 tuning range. Figure 5 (page 11*) shows that a proportional gain stage which is designed proportional to absolute temperature (PTAT) is almost perfectly matching the VCO characteristic from -25 to +75°C with slight degradation towards 125°C. The figure of merit κ as given in [2] is measured to 12.2n√s from 2.5 to 3.8GHz and 19.1n√s at 1.6GHz. Frequency acquisition is done by a frequency window detector (FWD) based on an $f_b/128$ quartz oscillator (active elements on-chip). The FWD performs a comparison every $2^{16} / f_b$ and the window is +6080/-5600ppm. The phase detector as proposed in reference [3] has the same input sensitivity as the data recovering latch. Sensitivity is further enhanced by two gain blocks with cumulative gain of (21+4.7=) 25.7dB and shown in figure 6 (page 13*). The steepness of the BER-curves is higher than the dotted reference based on pure gaussian noise. For 3.5Gb/s a dead band of $0.95mV_{pp}$ and noise of $0.22mV_{rms}$ can be calculated (1.9Gb/s: $0.64mV_{pp}$; $0.17mV_{rms}$) which is higher than in [4] when referred to the

latch. The offset was compensated and will be discussed later. The jitter tolerance mask for SDH is exceeded by a factor of 13.3 and the generated jitter is below $5ps_{rms}$ for electrical inputs above $10mV_{pp}$.

Receiver measurements with the 1:2 CDR-DMUX are given for different cases in figure 7 (page 17*) without additional noise filtering. They show that a gain decrease of 10dB could be tolerated if the offset is constrained to <<1.5mV. The effect of the dead band or noise calculated from figure 6 (page 13*) cannot explain the degradation resulting from 20dB attenuation. With -10dB the 1.5mV offset should give the $0.27dB_{optical}$ penalty at a signal level of ($160mV_{pp}$ -10dB =) $50mV_{pp}$ as can be seen in figure 7 (page 17*). Measurements of a 1:16 CDR-DMUX with a long haul APD frontend with -34dBm at 2.488Gb/s give similar results: no optical penalty with attenuation of the CDR input signal from 650 down to $65mV_{pp}$ and 0.3 to 0.6dB at $20mV_{pp}$ depending on offset compensation (1.6mV).

The CDR-DMUX features a loss-of-signal (LOS) detector that is not level dependent. Pulses which are produced in the phase detector as an error condition are used in [5] and used as additional information in [1] : two equal subsequent bits with a differing intermediate sample. This represents high frequency noise which is a portion of the total noise at the input. A probability of a 10^{-3} of this portion guarantees the BER to be $>10^{-3}$ as stated in the SDH LOS requirements (and violated in [1]). Depending on the noise-color of the amplifier the LOS-BER is measured between 1.8e-3 at 1.9Gb/s, 6e-3 at 3.5Gb/s and 6e-2 for the long haul APD frontend described above. In contrast to [5] this LOS is evaluated digitally with a counter being reset every $2^{16}/f_b$. LOS is set if the count is higher than 128 and reset if three consecutive counts are less then 64. Despite this hysteresis the LOS toggles with a 9s rate which can be explained by the statistics. If the mean error count is 85 then the square root of the variance is $\sqrt{85} = 9.2$. Gaussian distribution assumed the probability for a count >128 is 1.6e-6, for <64 it is 1.5e-2 which gives 3.4e-6 reset probability. Both probabilities being similar their mean value can be used to calculate a 10.4s rate for f_b=2.5GHz. The LOS evaluation is now redesigned to accommodate standards that require a single LOS edge for monotonous change in optical power.

Acknowledgments:

The authors thank K. Delker and H.Wuertele for layout, H.H. Schlachter for digital simulations, W.Hilgers and T. Neuner for system measurements and J.Reill for mounting modules.

References:

[1] R. Walker, et al: "A 2.488Gb/s Si-Bipolar Clock and Data Recovery IC with Robust Loss of Signal Detection", in *ISSCC Dig. Tech. Papers*, Feb. 1997, pp. 246-247

[2] J. A. McNeill.: "Jitter in Ring Oscillators",. IEEE J. Solid-State Circuits, SC-32 (1997), pp. 870 - 879.

[3] J. D. H. Alexander: "Clock recovery from random binary signals", Electronic Letters 11 (1975), pp. 541-542.

[4] J. Hauenschild, et al.: "A Plastic Packaged 10Gb/s BiCMOS Clock and Data Recovering 1:4 Demultiplexer with External VCO",. IEEE J. Solid-State Circuits, SC-31 (1996), pp. 2056 - 2059.

[5] "OQ2541", preliminary data sheet, Philips Semiconductors, 1995.

Figure Captions

Figure 1: Block diagram of 3-chip(a) versus 2-chip(b) receiver.

Figure 2: S21, differential S22 of PIN-preamp module and eye diagram at 1.9Gb/s (-24dBm) and 3.5Gb/s (-20dBm)

Figure 3: Photograph of PIN-preamp module.

Figure 4: Circuit diagram of one stage of the ring oscillator.

Figure 5: VCO transfer function and impact of the proportional path of the CDR.

Figure 6: CDR-DMUX input sensitivity at 1.9Gb/s (solid line) and 3.5Gb/s (dashed line)

Figure 7: Receiver input sensitivity at 1.9Gb/s (solid line) and 3.5Gb/s (dashed line).

*** Figures are not longer attached to this publication but can be found under the issued ISSCC98-slides on the respective page.**