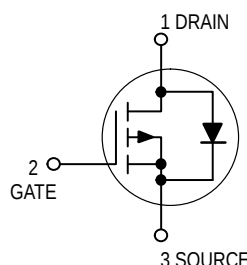


TMOS Field Effect Transistor

Dual In-Line Package

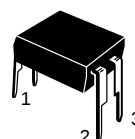
P-Channel Enhancement Mode

- Ideal for Peripheral Control Applications
- Intermediate 1 Watt Power Capability
- Standard DIP Outline



IRFD9120
IRFD9123

TMOS FET
TRANSISTORS
FET DIP



CASE 370-01, STYLE 1

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	IRFD9120	IRFD9123	Unit
Drain-Source Voltage	V_{DSS}	100	60	Vdc
Drain-Gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	V_{DGR}	100	60	Vdc
Gate-Source Voltage	V_{GS}	± 20		Vdc
Drain Current — Continuous $T_C = 25^\circ\text{C}$ — Pulsed	I_D I_{DM}	1.0 8.0	0.8 6.4	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0		Watts mW/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance — Junction-to-Ambient (Free Air Operation)	$R_{\theta JA}$	120	$^\circ\text{C/W}$
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TMOS is a registered trademark of Motorola, Inc.

REV 3

IRFD9120 IRFD9123

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage ($V_{GS} = 0$, $I_D = -250\ \mu\text{A}$)	$V_{(BR)DSS}$	100 60	— —	— —	Vdc
Zero Gate Voltage Drain Current ($V_{DSS} = \text{Rated } V_{DSS}$, $V_{GS} = 0\ \text{V}$)	I_{DSS}	—	—	250	μAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = -20\ \text{V}$)	I_{GSSF}	—	—	500	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20\ \text{V}$)	I_{GSSR}	—	—	500	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($I_D = -250\ \mu\text{A}$, $V_{DS} = V_{GS}$)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Static Drain-Source On-Resistance (1) ($V_{GS} = -10\ \text{Vdc}$, $I_D = -0.8\ \text{A}$)	$R_{DS(on)}$	— —	— —	0.6 0.8	Ohms
On-State Drain Current (1) ($V_{GS} = 10\ \text{V}$, $V_{DS} = -5.0\ \text{V}$)	$I_{D(on)}$	1.0 0.8	— —	— —	Adc
Forward Transconductance (1) ($I_D = -0.8\ \text{A}$, $V_{DS} = -5.0\ \text{V}$)	g_{FS}	0.8	—	—	mhos

CAPACITANCE

Input Capacitance	$(V_{DS} = -25\ \text{V}, V_{GS} = 0, f = 1.0\ \text{MHz})$	C_{iss}	—	—	450	pF
Output Capacitance		C_{oss}	—	—	350	
Reverse Transfer Capacitance		C_{rss}	—	—	100	

SWITCHING CHARACTERISTICS

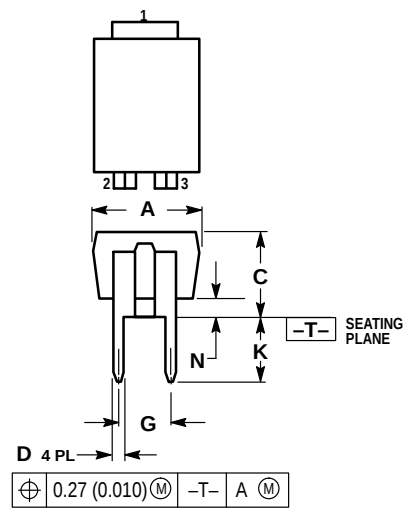
Turn-On Delay Time	$(V_{DS} \approx 0.5 V_{(BR)DSS}, I_D = -0.8\ \text{A}, Z_o = 50\ \Omega)$	$t_{d(on)}$	—	—	50	ns
Rise Time		t_r	—	—	100	
Turn-Off Delay Time		$t_{d(off)}$	—	—	100	
Fall Time		t_f	—	—	100	

SOURCE-DRAIN DIODE CHARACTERISTICS

Diode Forward Voltage ($V_{GS} = 0$)	$I_S = -1.0\ \text{A}$, IRFD9120 $I_S = -0.8\ \text{A}$, IRFD9123	V_F	— —	— —	6.3 6.0	Vdc
Continuous Source Current, Body Diode	IRFD9120 IRFD9123	I_S	— —	— —	1.0 0.8	Adc
Pulsed Source Current, Body Diode	IRFD9120 IRFD9123	I_{SM}	— —	— —	8.0 6.4	A
Forward Turn-On Time	$(I_S = \text{Rated } I_S, V_{GS} = 0)$	t_{on}	negligible			ns
Reverse Recovery Time		t_{rr}	—	150	—	

1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION J PRIOR TO SOLDER DIP PLATING.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.185	0.198	4.70	5.02
B	0.240	0.280	6.10	7.11
C	0.160	0.200	4.06	5.08
D	0.015	0.025	0.38	0.63
G	0.100 BSC		2.54 BSC	
J	0.012	0.017	0.30	0.43
K	0.110	0.150	2.79	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.070	0.51	1.77

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

CASE 370-01
ISSUE A

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How to reach us:

USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244-6609
INTERNET: <http://Design-NET.com>

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

