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TENTATIVE SPECIFICATIONS

Product Type CCD SIGNAL PROCESS & DIGITAL INTERFACE

Model No. IR3Y38M

※This tentative specifications contain 26 pages including the cover and appendix.
The contents might modify for the reform of characteristics or other reasons.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: T. Ohno
T. OHNO
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Engineering Dept. 4
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SHARP CORPORATION

●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).
- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.
- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.
- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

1. Description

The IR3Y38M is an one-chip signal processing IC for CCD area sensers. This device includes correlated double sampling circuit(CDS), automatic gain control amplifier(AGC),and 10bit analog-to-digital converter(ADC).

Features

- Low power consumption. (315mW TYP.)
- High speed sample-and-hold circuits.(pulse width 12ns MIN.)
- Wide AGC gain variation from 10.5dB to 41dB.
- 10bit ADC operating up to 18MHz.
- Serial interface to be able to control the AGC gain,maximum gain and offset adjustment.
- Standby mode is available for power saving applications.
- Operates at 5V simple voltage.
- Digital interface for 3V/3.3V operating logic ICs.

* Not designed or rated as radiation hardened.
* Packaging material: Plastic
* Chip material and wafer substrate type: P-type silicon
* Number of pins and package type: 48-pin quad-flat package
* Process(structure): Bipolar

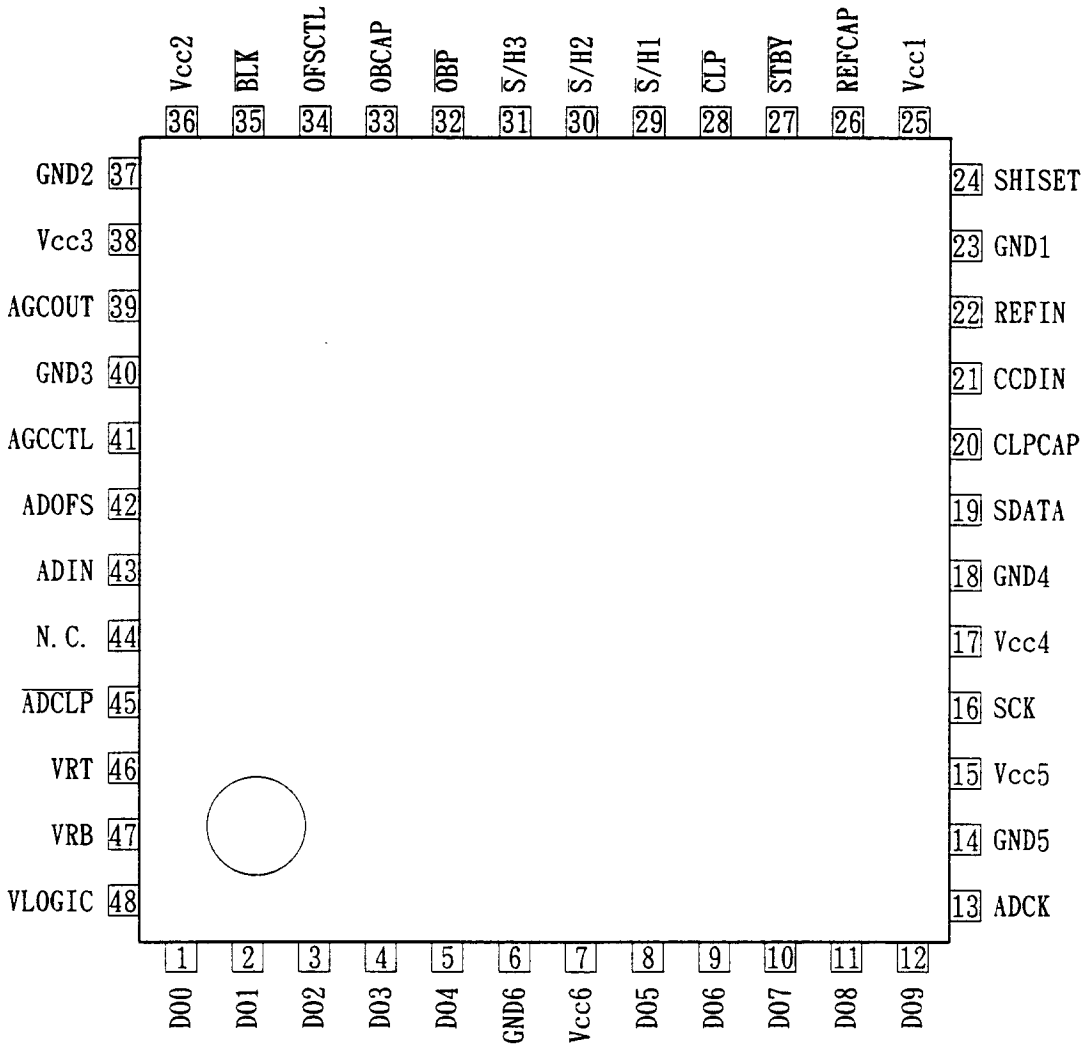
Applications

CCD camera
Digital still camera

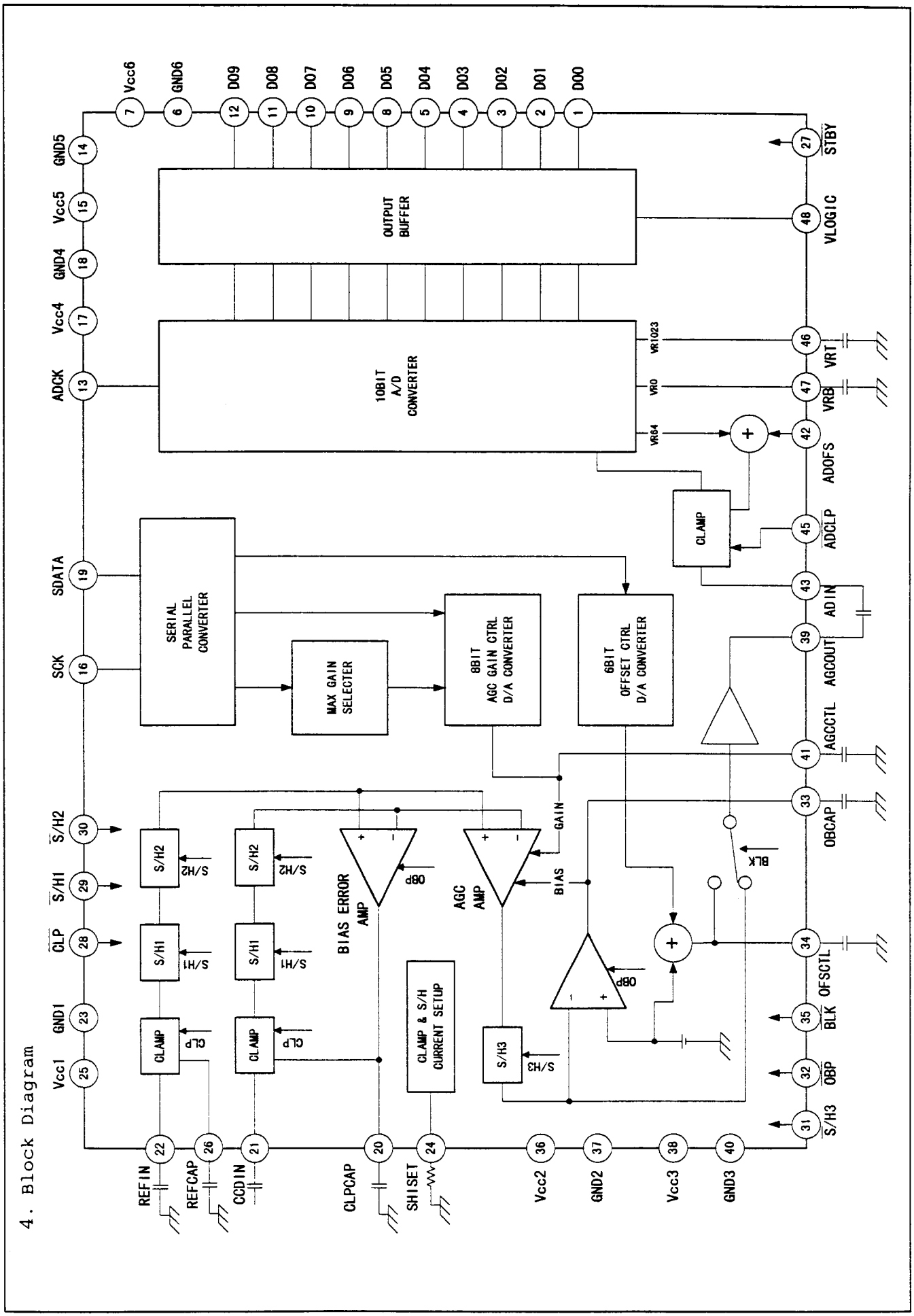
2. Terminal Names

Pin No.	Terminal Name	Pin No.	Terminal Name
1	DO0	25	Vcc1
2	DO1	26	REFCAP
3	DO2	27	$\overline{\text{STBY}}$
4	DO3	28	$\overline{\text{CLP}}$
5	DO4	29	$\overline{\text{S/H1}}$
6	GND6	30	$\overline{\text{S/H2}}$
7	Vcc6	31	$\overline{\text{S/H3}}$
8	DO5	32	$\overline{\text{OBP}}$
9	DO6	33	OBCAP
10	DO7	34	OFSCTL
11	DO8	35	$\overline{\text{BLK}}$
12	DO9	36	Vcc2
13	ADCK	37	GND2
14	GND5	38	Vcc3
15	Vcc5	39	AGCOUT
16	SCK	40	GND3
17	Vcc4	41	AGCCTL
18	GND4	42	ADOFS
19	SDATA	43	ADIN
20	CLPCAP	44	N.C.
21	CCDIN	45	$\overline{\text{ADCLP}}$
22	REFIN	46	VRT
23	GND1	47	VRB
24	SHISET	48	VLOGIC

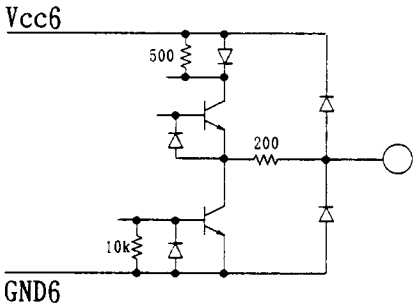
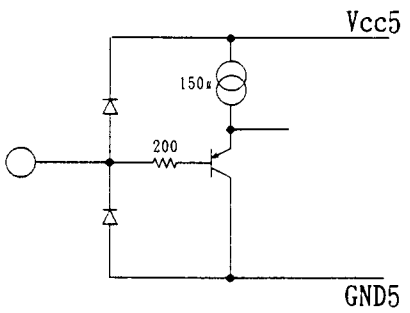
3. Terminal Configration (TOP VIEW)

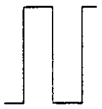
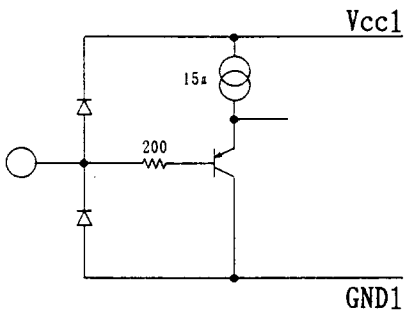


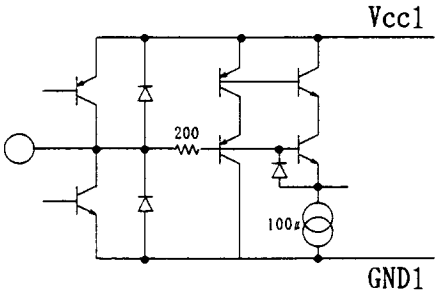
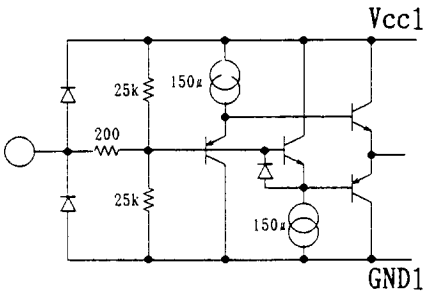
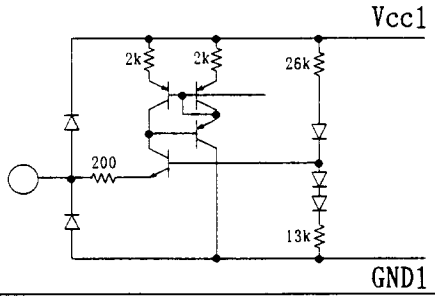
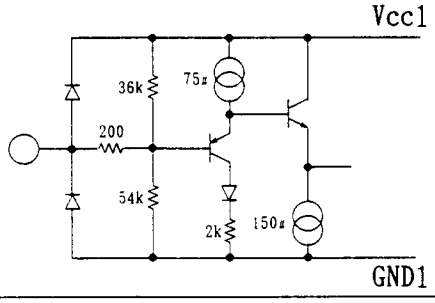
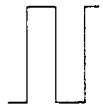
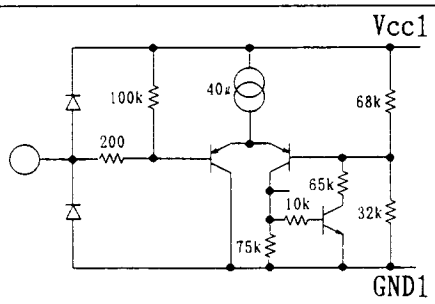
4. Block Diagram

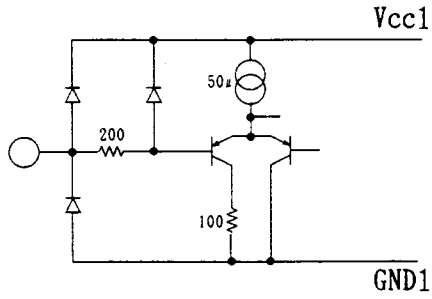
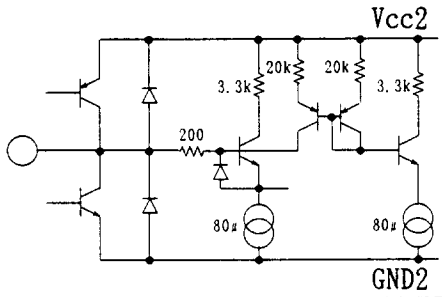
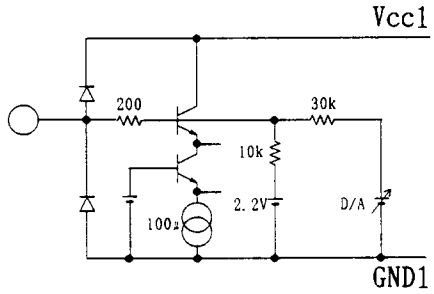
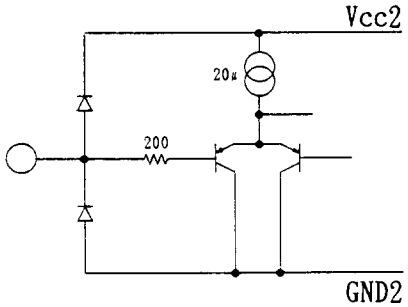
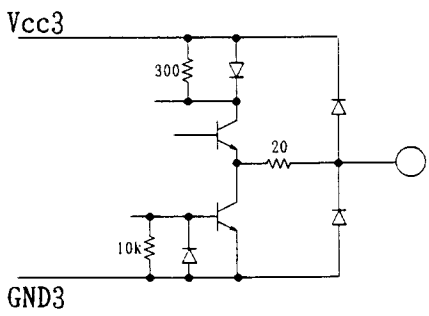


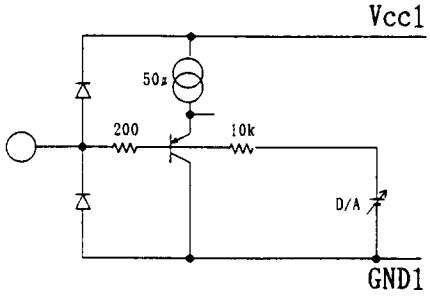
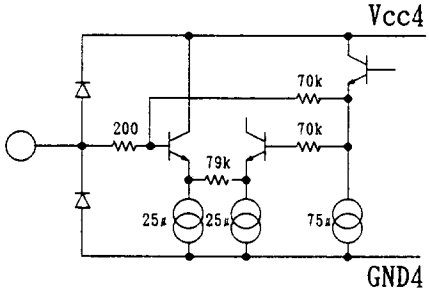
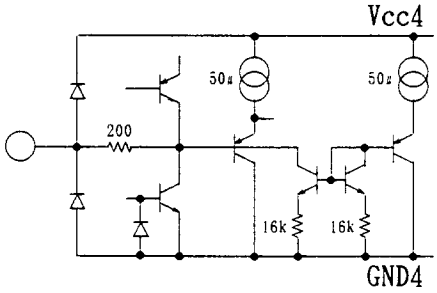
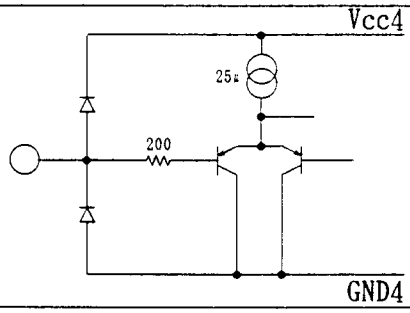
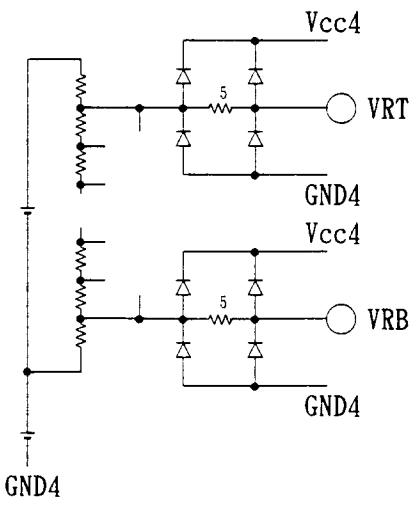
5. Description of terminal functions
(The voltage is measured on condition that Vcc1~6=5.0V, VLOGIC=3.3V)

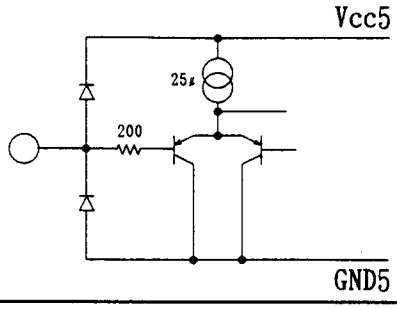
Pin #	Name	Voltage	Equivalent circuit	Description
25	Vcc1	5.0V		Power supply pins of the CDS/AGC. Pay careful attention to board layout of the GND1 because the CDS/AGC is noise sensitive circuits.
23	GND1	0.0V		
36	Vcc2	5.0V		Power supply pins of the S/H3 and OPB-clamp circuits.
37	GND2	0.0V		
38	Vcc3	5.0V		Power supply pins of the output buffer circuit connected to the AGCOUT pin.
40	GND3	0.0V		
17	Vcc4	5.0V		Analog power supply pins of the A/D converter.
18	GND4	0.0V		
15	Vcc5	5.0V		Digital power supply pins of the A/D converter.
14	GND5	0.0V		
7	Vcc6	5.0V		Power supply pins of the output buffer of the A/D converter.
6	GND6	0.0V		
1	D00	3.1V 0.2V		Digital data output pins of the A/D converter. D00 is LSB and D09 is MSB. The data format is a straight binary code. V_{OL}: 0.2V (typ.) V_{OH}: VLOGIC - 0.2V (typ.)
2	D01			
3	D02			
4	D03			
5	D04			
8	D05			
9	D06			
10	D07			
11	D08			
12	D09			
13	ADCK	>2.1V <0.7V		Clock input pin of the A/D converter. The A/D conversion is executed with the rise edge of the ADCK, and the data is outputed with the fall edge of the one. duty : 50% fmax : 18MHz min.

<table>
<tr><th>Pin #</th><th>Name</th><th>Voltage</th><th>Equivalent Circuit</th><th>Description</th></tr>
<tr><td>16</td><td>SCK</td><td rowspan="2">>2.1V
 
<0.7V</td><td rowspan="2"> 
</td><td rowspan="2">Clock or data input pins of the serial interface.

<table>
<tr><th>SDATA</th><th>SCK</th><th>action</th></tr>
<tr><td>DATA</td><td>↑</td><td>SHIFT</td></tr>
<tr><td>0</td><td>↓</td><td>—</td></tr>
<tr><td>1</td><td>↓</td><td>STORE</td></tr>
</table></td></tr>
<tr><td>19</td><td>SDATA</td></tr>
<tr><td>20</td><td>CLPCAP</td><td>3.2V</td><td> 
</td><td>Bias decoupling pin of the CDS signal clamp circuit. This pin is connected to the GND1 via a capacitor.</td></tr>
<tr><td>21</td><td>CCDIN</td><td>2.5V</td><td rowspan="2"> 
</td><td>Signal input pin of the CDS. Input CCD signal to this pin via a capacitor.</td></tr>
<tr><td>22</td><td>REFIN</td><td>2.5V</td><td>Reference input pin of the CDS. This pin is connected to the GND1 via a capacitor.</td></tr>
<tr><td>24</td><td>SHISET</td><td>1.7V</td><td> 
</td><td>Operation current setting pin of the CDS and S/H3 circuits.
This pin is connected to the GND1 via a resister.
The slew rates of the S/Hs are in inverse proportion to the value of the resister.</td></tr>
<tr><td>26</td><td>REFCAP</td><td>3.2V</td><td> 
</td><td>Bias decoupling pin of the CDS reference clamp circuit.
This pin is connected to the GND1 via a capacitor.</td></tr>
<tr><td>27</td><td>$\overline{\text{STBY}}$</td><td>5.0V
(open)
>2.1V
 
<0.7V</td><td> 
</td><td>Stand-by function control pin. All the actions stop and the power dissipation is decreased when low.
The threshold voltage has 0.4V hysteresys.
Connect to the Vcc if not used.</td></tr>
</table>

Pin #	Name	Voltage	Equivalent Circuit	Description
28	$\overline{CLP}$	>2.1V <0.7V		Pulse input pin of the CDS feed-through level clamp. Signal is clamped when low.
29	$\overline{S/H1}$			Pulse input pin of the CDS S/H1 signal sampler. Signal is sampled when low.
30	$\overline{S/H2}$			Pulse input pin of the CDS S/H2. Signal is sampled when low.
31	$\overline{S/H3}$			Pulse input pin of the S/H3. Signal is sampled when low.
32	$\overline{OBP}$			Pulse input pin of the OPB clamp and bias error amp. Signal is clamped when low.
33	OBCAP	3.7V		Clamp capacitor pin of the optical black clamp (OPB clamp) circuit. Connect to the GND2 via a capacitor.
34	OFSCTL	2.15V ~2.30V		Decoupling capacitor pin of the blanking offset control D/A converter. Connect to the GND1 via a capacitor.
35	$\overline{BLK}$	>2.1V <0.7V		Blanking pluse input pin. The output of the AGCOUT pin is blanked when low. The blanking level can be controlled by the serial interface.
39	AGCOUT	0.9V ($\overline{OBP}$=L)		Signal output pin of the AGC. Connect to the ADIN pin via a capacitor.

Pin #	Name	Voltage	Equivalent Circuit	Description
41	AGCCTL	2.5V ~3.8V		Decoupling capacitor pin of the AGC gain control D/A converter. Connect to the GND1 via a capacitor.
42	ADOFS	3.3V (open) input range 1.6V ~ 5.0V		Voltage adjustment pin of the ADC black level clamp. This pin is biased at 3.3V from the inside of the IC. Connect to the GND4 via a capacitor if not used.
43	ADIN	1.2V (ADCLP=L)		Signal input pin of the ADC. Connect to the AGCOUT pin via a capacitor. This capacitor is also used as the clamp capacitor of the ADC blank level clamp.
44	N.C.			Non connection. It is recommended to connect to GND for better heat radiation and avoiding noise.
45	$\overline{\text{ADCLP}}$	>2.1V <0.7V		Pulse input pin of the ADC black level clamp. Signal is clamped when low. When the ADOFS is open, the clamped level is setted to make the ADC output 62 (decimal).
46	VRT	3.9V		Upper reference decoupling pin of the ADC. Connect to the GND4 via a capacitor.
47	VRB	1.9V		Lower reference decoupling pin of the ADC. Connect to the GND4 via a capacitor.

Pin #	Name	Voltage	Equivalent Circuit	Description
48	VLOGIC	3.3V		ADC output voltage setting pin. The high level voltage of the D00~D09 pins is set-ed to VLOGIC - 0.2V. It is recommended to con-nect to the power supply of the following logic ICs.

6. Description of Operations

・CDS circuit

The clamp circuit clamps the feed-through level of the CCD signal with the $\overline{CLP}$ pulse. Then the $\overline{S/H1}$ circuit samples the signal period of the one with the $\overline{S/H1}$ pulse and holds on. Thus the video signal is obtained. But this signal has the level drop caused by the reset pulse of the CCD signal, and for removing it, the $\overline{S/H2}$ circuit samples this signal again with the $\overline{S/H2}$ pulse.
For reducing the effect of the sampling pulse or other noise sources, the CDS circuit is formed with a differential structure.

・Bias error amplifier circuit

For stabilizing the bias level of the CDS circuit and reducing the offset of the AGC circuit, the bias error amplifier acts with the $\overline{OBP}$ pulse during the OPB period.

・AGC amplifier circuit

The AGC amplifier amplifies the video signal obtained by the CDS circuit. The gain of the AGC is controlled by the value of the AGCGAIN serial register. And maximum gain of the AGC is controlled by the value of the GAINSEL serial register.

・OPB clamp circuit

For clamping the level of the amplified signal to the black level, the OPB clamp circuit acts with the $\overline{OBP}$ pulse during the OPB period.

・Blanking circuit

The output signal is fixed to the blanking level with the $\overline{BLK}$ pulse. The blanking level is the sum of the black level and the offset value decided by the value of the OFFSET serial register.

・A/D converter

The $\overline{S/H3}$ circuit samples the amplified signal with $\overline{S/H3}$ pulse and the A/D converter converts the sampled signal to the 10bit straight binary digital data. The clamp circuit placed in front of the A/D converter clamps the signal level beside the lower limit of the convertible input range with the $\overline{ADCLP}$ pulse. The clamped level is controllable by the voltage of the ADOFS pin.

The A/D conversion is executed with a rise edge of the ADCK clock, and the data is outputed with a fall edge of the one.

The high level voltage of the outputs is controlled by the voltage of the VLOGIC pin.

・Standby function

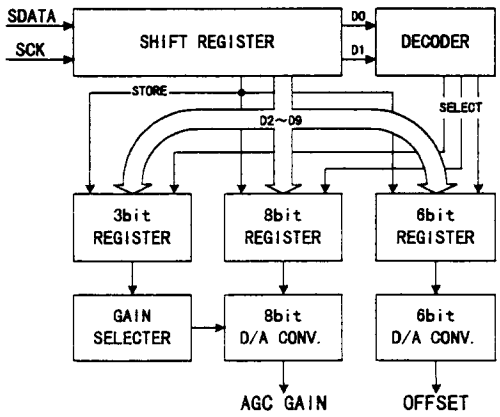
By making the $\overline{STBY}$ pin low, all the action of this IC stops and the power dissipation is decreased.

The outputs of the A/D converter (D00~D09) turn to high impedance when standby.

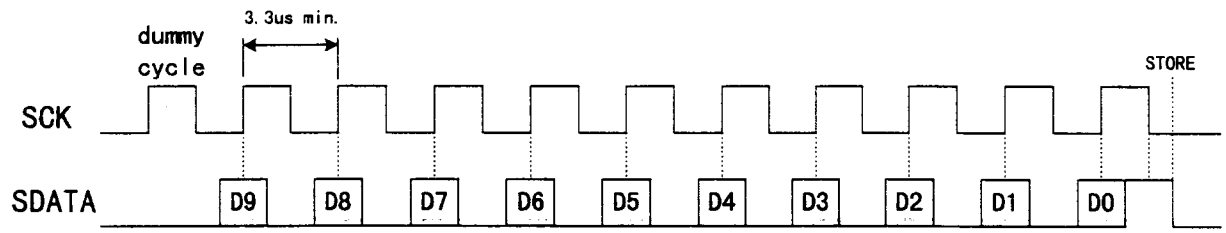
・ Serial Interface

The IR3Y38M has a serial interface to control the gain of the AGC amplifier and the offset of the blanking level. This interface is constituted by a shift register for serial-parallel conversion, data registers and D/A converters.

The data inputted to SDATA is fetched and shifted with the rise edge of the SCK. While transmitting data, the SDATA must be low when the SCK falls. When the SDATA is high and the SCK falls, the data on the shift register is stored to the selected data register with a following fall edge of the SDATA. The stored data register is selected by the data of the D0 and D1 bits.

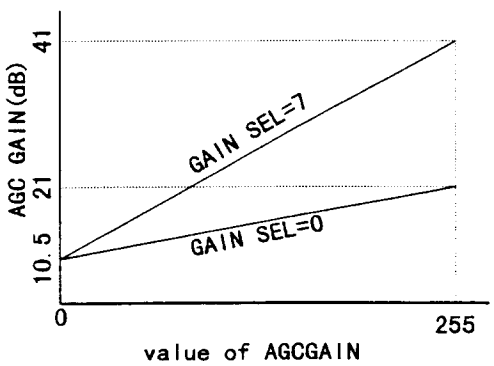


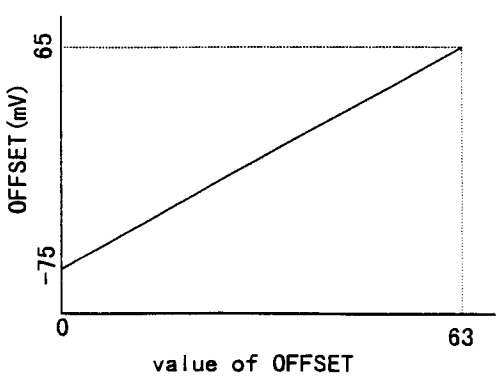
GAINSEL	Maximum Gain(dB)
0	21
1	24
2	27
3	30
4	33
5	36
6	38.5
7	41



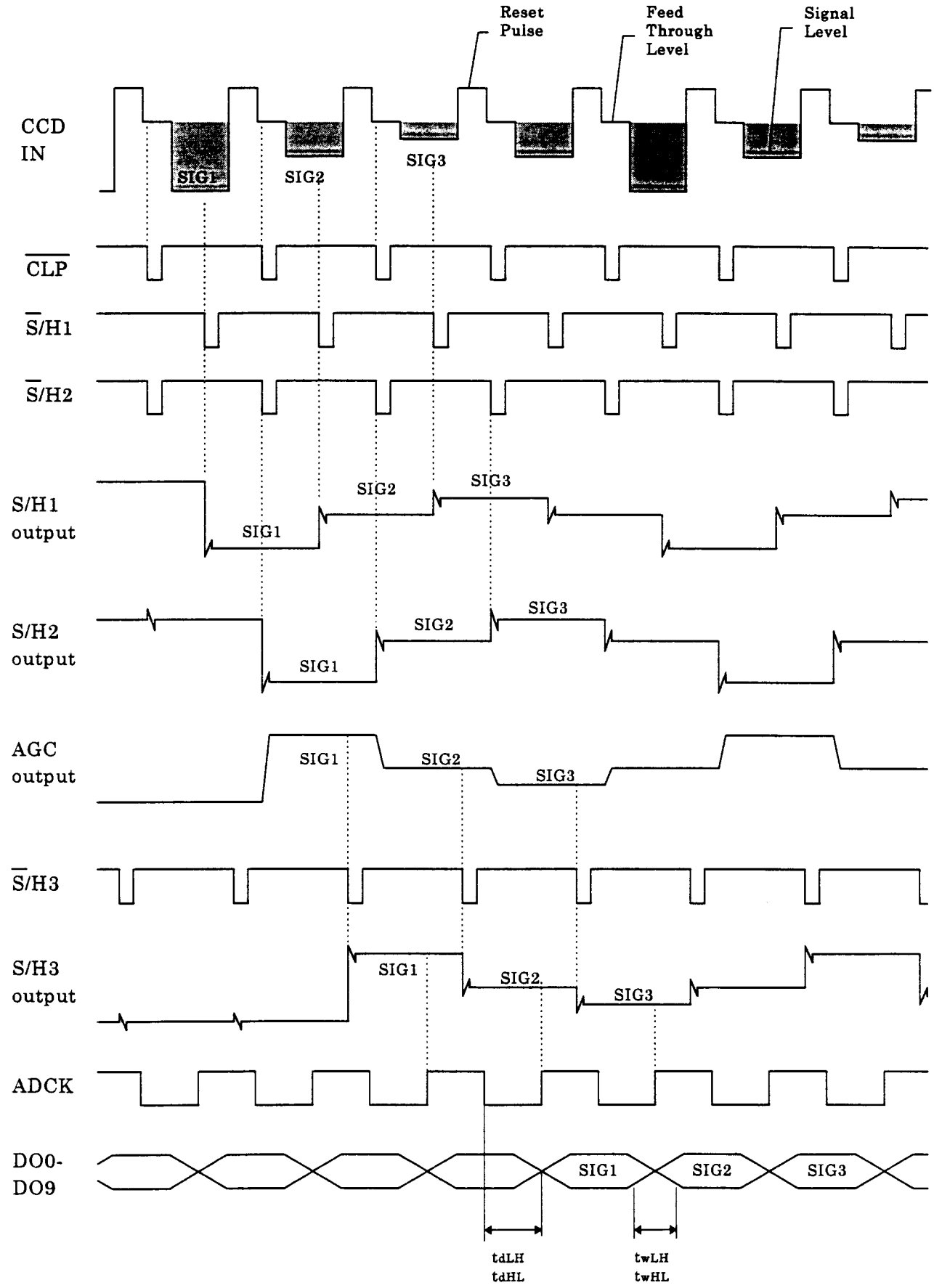
Data Register	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
GAIN SEL						d0	d1	d2	0	0
AGC GAIN	d0	d1	d2	d3	d4	d5	d6	d7	0	1
OFFSET			d0	d1	d2	d3	d4	d5	1	0
(don't care)									1	1

LSB MSB





7. Timing Diagram



8. Precautions

The each Vcc1~Vcc6 pins correspond to the each GND1~GND6 pins. Connect a ceramic capacitor as near the IC as possible between the each corresponding Vcc pins and GND pins.

The GND1 pin is the ground of the CDS circuit handling weak signal. Pay careful attention to board layout of the GND1 pattern in order to avoid the potential fluctuation of the GND1 caused by the current of the other GND pins. Especially pay attention to the current of the GND6 pin flowing spiky current.

All the GND pins must be at the same potential and not open. And keep the potential difference of the each Vcc pins within 0.3V.

The high level voltage of the outputs of the A/D converter is controllable by the voltage of the VLOGIC pin, but take care about the high level voltage do not become below about 1.5V in spite of making the VLOGIC pin 0V. This may cause the latch up of the following logic ICs if the power supply of this IC stands up faster than the power supply of the following logic. To avoid this problem, it is recommended to make the $\overline{\text{STBY}}$ pin low until the voltage of the logic power supply becomes stable. Take care too about the high level voltage do not become above about Vcc - 1.0V in spite of making the VLOGIC pin the Vcc potential.

9. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	Vcc1 ~ Vcc6		7	V
Power Dissipation	P_D	Ta ≦ 25℃	570	mW
Derating Ratio		Ta > 25℃	4.5	mW/℃
Operating Temperature Range	T_{opr}		-30 ~ 70	℃
Storage Temperature Range	T_{stg}		-55 ~ 150	℃
Input Voltage Range	V_{IN}		-0.3 ~ Vcc+0.3	V

10. Recommended Operating Conditions

Parameter	Symbol	Applications	Rating	Unuit
Supply Voltage	Vcc1 ~ Vcc6		4.75 ~ 5.25	V
Standard CCD Input Signal Level	V_{CCD}	CCDIN	200	mV_{P-P}
Input Voltage (High)	V_{IH}	$\overline{ADCK}$, SCK, SDATA, $\overline{STBY}$, $\overline{CLP}$, $\overline{S/H1}$, $\overline{S/H2}$, $\overline{S/H3}$, $\overline{OBP}$, $\overline{BLK}$, $\overline{ADCLP}$	2.1 ~ Vcc	V
Input Voltage (Low)	V_{IL}		0 ~ 0.7	V
S/H Pulse Width	$t_{WS/H}$	$\overline{CLP}$, $\overline{S/H1}$, $\overline{S/H2}$, $\overline{S/H3}$	12 ~	ns
Clamp Pulse Width	t_{WC}	$\overline{OBP}$, $\overline{ADCLP}$	1.5 ~	μs
A/D Converter Clock Frequency	f_{ADCK}	ADCK	~ 18	MHz
Serial Interface Clock Frequency	f_{SCK}	SCK	~ 300	kHz

11. Electrical Characteristics

• DC Electrical Characteristics

If not indicated, Ta=25℃ , Vcc1=Vcc2=Vcc3=Vcc4=Vcc5=Vcc6=5.0V , VLOGIC=3.3V
ADCK = 0V, SCK = 0V, SDATA = 0V, $\overline{\text{STBY}}$ = 3.3V, $\overline{\text{CLP}}$ = 0V
$\overline{\text{S}}$/H1 = 0V, $\overline{\text{S}}$/H2 = 0V, $\overline{\text{S}}$/H3 = 0V, $\overline{\text{BLK}}$ = 3.3V, $\overline{\text{OBP}}$ = 0V
SW42 = OFF SW43 = a, $\overline{\text{ADCLP}}$=3.3V
The current direction flowing into the pin is positive direction.

* General

Pin#	Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
1	Supply Current(1)	I_{CC1}	Vcc1		27		mA
2	Supply Current(2)	I_{CC2}	Vcc2		2.3		mA
3	Supply Current(3)	I_{CC3}	Vcc3		0.7		mA
4	Supply Current(4)	I_{CC4}	Vcc4		13		mA
5	Supply Current(5)	I_{CC5}	Vcc5		16		mA
6	Supply Current(6)	I_{CC6}	Vcc6		5.0		mA
7	Total Supply Current	I_{CC}	Total of Icc1~Icc6.		63		mA
8	Standby Supply Current	I_{STBY}	$\overline{\text{STBY}}$=0V, Total of Icc1~Icc6.		4.0		mA
9	Input Current (High) (1)	I_{IH1}	Apply to $\overline{\text{CLP}}$, $\overline{\text{S}}$/H1, $\overline{\text{S}}$/H2, $\overline{\text{S}}$/H3 and $\overline{\text{OBP}}$ pins. V_{IH}=3.3V		0		μA
10	Input Current (Low) (1)	I_{IL1}	Apply to $\overline{\text{CLP}}$, $\overline{\text{S}}$/H1, $\overline{\text{S}}$/H2, $\overline{\text{S}}$/H3 and $\overline{\text{OBP}}$ pins. V_{IL}=0V		-1.2		μA
11	Input Current (High) (2)	I_{IH2}	Apply to SCK and SDATA pins. V_{IH}=3.3V		0		μA
12	Input Current (Low) (2)	I_{IL2}	Apply to SCK and SDATA pins. V_{IL}=0V		-0.2		μA
13	Input Current (High) (3)	I_{IH3}	Apply to $\overline{\text{BLK}}$ and $\overline{\text{ADCLP}}$ pins. V_{IH}=3.3V		0		μA
14	Input Current (Low) (3)	I_{IL3}	Apply to $\overline{\text{BLK}}$ and $\overline{\text{ADCLP}}$ pins. V_{IL}=0V		-0.3		μA
15	Input Current (High) (4)	I_{IH4}	Apply to ADCK pin. V_{IH}=3.3V		0		μA
16	Input Current (Low) (4)	I_{IL4}	Apply to ADCK pin. V_{IL}=0V		-2.0		μA
17	$\overline{\text{STBY}}$ Voltage	V_{27}	Open $\overline{\text{STBY}}$ pin.		5.0		V
18	$\overline{\text{STBY}}$ Impedance	Z_{27}			110		kΩ

* CDS/AGC Part

Pin#	Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
19	CLPCAP Voltage	V_{20}			3.2		V
20	CCDIN Voltage	V_{21}			2.5		V
21	REFIN Voltage	V_{22}			2.5		V
22	SHISET Voltage	V_{24}			1.7		V
23	REFCAP Voltage	V_{26}			3.2		V
24	OBCAP Voltage	V_{33}			3.7		V

Pin#	Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
25	AGCOUT Voltage	V_{39}			0.9		V
26	CCDIN Impedance	Z_{21}			14		kΩ
27	REFIN Impedance	Z_{22}			14		kΩ
28	REFCAP Impedance	Z_{26}			26		kΩ
29	OFSCTL Impedance	Z_{34}			9.5		kΩ
30	AGCCTL Impedance	Z_{41}			12		kΩ
31	CLPCAP Charge Current	I_{L20}	CLPCAP=2.8V, OBP=0V Measure the current of CLPCAP.		-135		μA
32	CLPCAP Discharge Current	I_{H20}	CLPCAP=3.6V, OBP=0V Measure the current of CLPCAP.		135		μA
33	CLPCAP Leakage Current	I_{Z20}	CLPCAP=3.2V, OBP=3.3V Measure the current of CLPCAP.	-0.5	0	0.5	μA
34	OBCAP Charge Current	I_{L33}	OBCAP=3.3V, OBP=0V Measure the current of OBCAP.		-90		μA
35	OBCAP Discharge Current	I_{H33}	OBCAP=4.1V, OBP=0V Measure the current of OBCAP.		90		μA
36	OBCAP Leakage Current	I_{Z33}	OBCAP=3.7V, OBP=3.3V Measure the current of OBCAP.	-0.5	0	0.5	μA

* A/D Converter Part

Pin#	Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
37	ADOFS Voltage	V_{42}			3.3		V
38	ADIN Voltage	V_{43}	ADCLP=0V		1.4		V
39	VRT Voltage	V_{46}			3.9		V
40	VRB Voltage	V_{47}			1.9		V
41	ADOFS Impedance	Z_{42}			70		kΩ
42	ADIN Charge Current	I_{L43}	ADIN=1.0V, ADCLP=0V Measure the current of ADIN.		-45		μA
43	ADIN Discharge Current	I_{H43}	ADIN=1.8V, ADCLP=0V Measure the current of ADIN.		45		μA
44	ADIN Leakage Current	I_{Z43}	ADIN=1.4V, ADCLP=3.3V Measure the current of ADIN.	-0.3	0	0.3	μA
45	Output Voltage (Low)	V_{OL}	SW43=b, ADCIN=0.8V Change the level of ADCK to L→H→L, then measure the voltage of D00~D09 pins.		0.20		V
46	Output Voltage (High)	V_{OH}	SW43=b, ADCIN=3.5V Change the level of ADCK to L→H→L, then measure the voltage of D00~D09 pins.		3.10		V

• AC Electrical Characteristics

If not indicated, Ta=25℃ , Vcc1=Vcc2=Vcc3=Vcc4=Vcc5=Vcc6=5.0V , VLOGIC=3.3V
ADCK = 0V, SCK = 0V, SDATA = 0V, STBY = 3.3V, CLP = 3.3V
S/H1 = 0V, S/H2 = 0V, S/H3 = 0V, BLK = 3.3V, OBP = 3.3V
SW42 = OFF SW43 = a, ADCLP=3.3V
(OFFSET)=32 The value of the serial register is written with DECIMAL system.

* CDS/AGC Part

Pin#	Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
100	AGC Mimimum Gain	G_{AN}	(GAINSEL)=0, (AGCGAIN)=0 CLP=SG2, OBP=SG3 Input the attenuated SG1(f=2MHz, V=1.6V_{P-P}) to the SIN and seek the attenuation amount to make the amplitude of AGCOUT 1.6V_{P-P}.		10.5		dB
101	AGC Maximum Gain (0)	G_{AX0}	(GAINSEL)=0, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		21.0		dB
102	AGC Maximum Gain (1)	G_{AX1}	(GAINSEL)=1, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		24.0		dB
103	AGC Maximum Gain (2)	G_{AX2}	(GAINSEL)=2, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		27.0		dB
104	AGC Maximum Gain (3)	G_{AX3}	(GAINSEL)=3, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		30.0		dB
105	AGC Maximum Gain (4)	G_{AX4}	(GAINSEL)=4, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		33.0		dB
106	AGC Maximum Gain (5)	G_{AX5}	(GAINSEL)=5, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		36.0		dB
107	AGC Maximum Gain (6)	G_{AX6}	(GAINSEL)=6, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		38.5		dB
108	AGC Maximum Gain (7)	G_{AX7}	(GAINSEL)=7, (AGCGAIN)=255 Measure the gain alike the measurement of G_{AN}.		41.0		dB
109	AGC Gain Variable Width	G_{AR}	$G_{AR} = G_{AX7} - G_{AN}$		30.5		dB
110	Bandwidth (1) (Mimimum Gain)	f_{tN}	(GAINSEL)=0, (AGCGAIN)=0 CLP=SG2, OBP=SG3 Input the SG1(f=2MHz, V=0.25V_{P-P}) to the SIN and measure the amplitude of the AGC-OUT. Increase the frequency and measure the frequency when the amplitude attenuates to -3dB.		32		MHz
111	Bandwidth (2) (Maximum Gain)	f_{tX}	(GAINSEL)=7, (AGCGAIN)=255 CLP=SG2, OBP=SG3 Input the SG1(f=2MHz, V=7.5mV_{P-P}) to the SIN and measure the amplitude of the AGC-OUT. Increase the frequency and measure the frequency when the amplitude attenuates to -3dB.		17		MHz

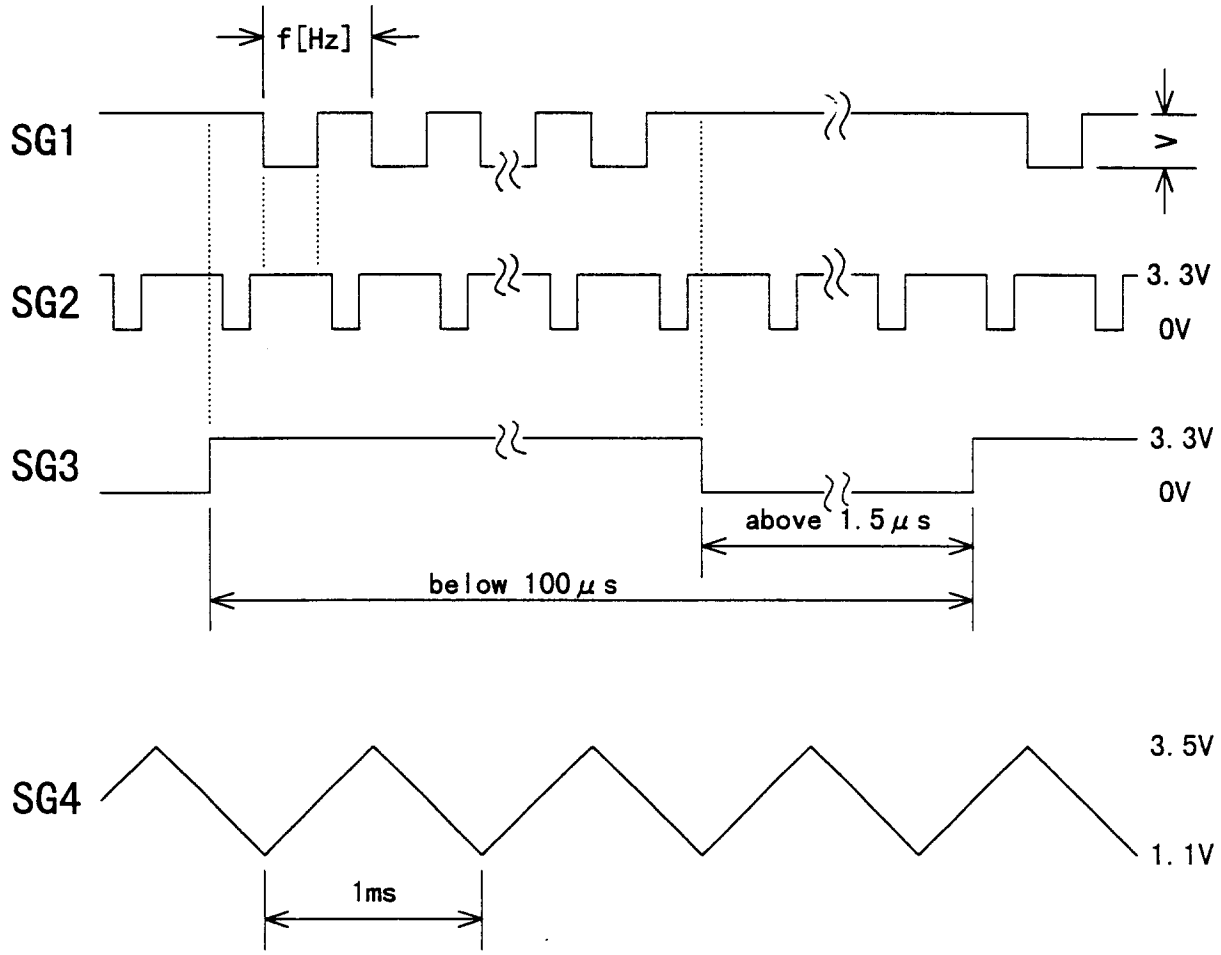
Pin#	Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
112	OFFSET Adjustment Limit (1) (OFFSET=0)	V_{BON}	(GAINSEL)=0 (AGCGAIN)=0 SIN=GND1, (OFFSET)=0, $\overline{CLP}$=0V, $\overline{OBP}$=0V Measure the voltage of the AGCOUT at BLK=3.3V and define it V_{BO11}. Measure the one similarly at BLK=0V and define it V_{BO12}. $V_{BON} = V_{BO12} - V_{BO11}$		-75		mV
113	OFFSET Adjustment Limit (2) (OFFSET=63)	V_{BOX}	(GAINSEL)=0 (AGCGAIN)=0 SIN=GND1, (OFFSET)=63, $\overline{CLP}$=0V, $\overline{OBP}$=0V Measure the V_{BO21} and V_{BO22} similarly to above-mentioned method. $V_{BON} = V_{BO22} - V_{BO21}$		65		mV
114	Output Dynamic Range (1) (Minimum Gain)	V_{DYN}	(GAINSEL)=0, (AGCGAIN)=0 $\overline{CLP}$=SG2, $\overline{OBP}$=SG3 Input the SG1(f=2MHz, V=0.8V_{P-P}) to the SIN and measure the amplitude of the AGCOUT.	2.0	2.3	-	V_{P-P}
115	Output Dynamic Range (2) (Maximum Gain)	V_{DYX}	(GAINSEL)=0 (AGCGAIN)=0 $\overline{CLP}$=SG2, $\overline{OBP}$=SG3 Input the SG1(f=2MHz, V=50mV_{P-P}) to the SIN and measure the amplitude of the AGCOUT.	2.0	2.3	-	V_{P-P}

* A/D Converter Part

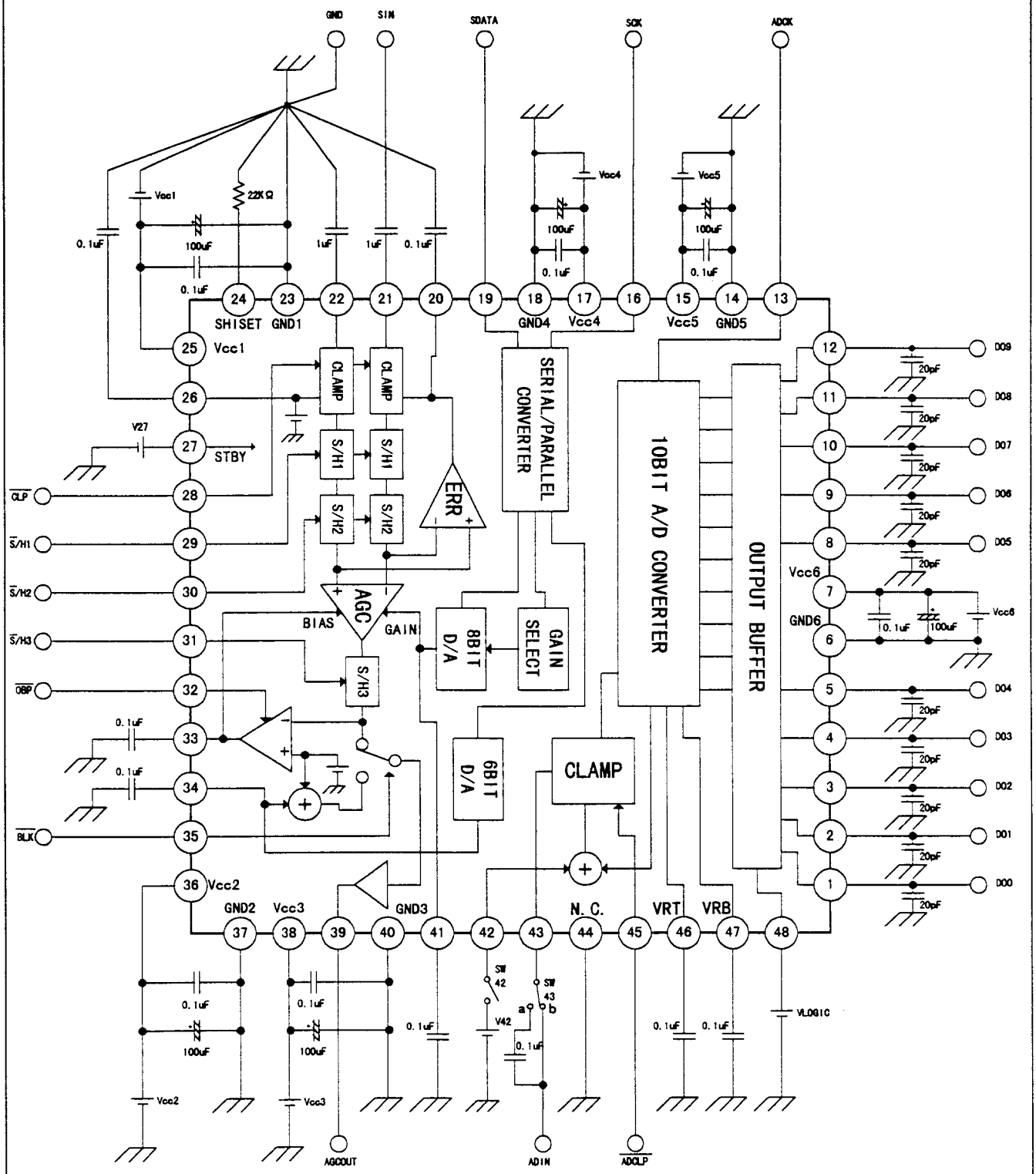
If not indicated, Ta=25℃ , Vcc1=Vcc2=Vcc3=Vcc4=Vcc5=Vcc6=5.0V , VLOGIC=3.3V
ADCK = 18MHz SQUARE WAVE, SCK = 0V, SDATA = 0V, STBY = 3.3V
CLP = 3.3V, S/H1 = 0V, S/H2 = 0V, S/H3 = 0V, BLK = 3.3V
OBP = 3.3V, SW42 = OFF, SW43 = b, ADCLP = 3.3V

Pin#	Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
116	Clamp Value	D_{CLP}	SW43=a ADCLP=0V ADCIN=GND4 Read the output value of D00~D09.		62		-
117	Clamp Value Adjustment Limit(1)	D_{CLPN}	SW42=ON, V42=5.0V, ADCLP=0V, ADCIN=GND4 Read the output value of D00~D09.		37		-
118	Clamp Value Adjustment Limit(2)	D_{CLPX}	SW42=ON, V42=1.6V, ADCLP=0V, ADCIN=GND4 Read the output value of D00~D09.		87		-
119	Differential Linearity Error	DLE	ADCIN=SG4 Read the output value of D00~D09 at about 10^6 times and make it a histogram. Normalize the histogram and obtain the DLE. And integrate the histogram and obtain the ILE.		±0.5		LSB
120	Integral Linearity Error	ILE			±1.5		LSB
121	Propagation Delay (L→H)	T_{dLH}	ADCIN=SG4, C_L=20pF Measure the delay time from the rise edge (50%) of the ADCK to the rise edge (50%) of the D00~D09.		25		ns
122	Propagation Delay (H→L)	T_{dHL}	ADCIN=SG4, C_L=20pF Measure the delay time from the rise edge (50%) of the ADCK to the fall edge (50%) of the D00~D09.		25		ns
123	Output Rise Time	T_{wLH}	ADCIN=SG4, C_L=20pF Measure the rise time (10% → 90%) of the D00~D09.		20		ns
124	Output Fall Time	T_{wHL}	ADCIN=SG4, C_L=20pF Measure the fall time (90% → 10%) of the D00~D09.		20		ns

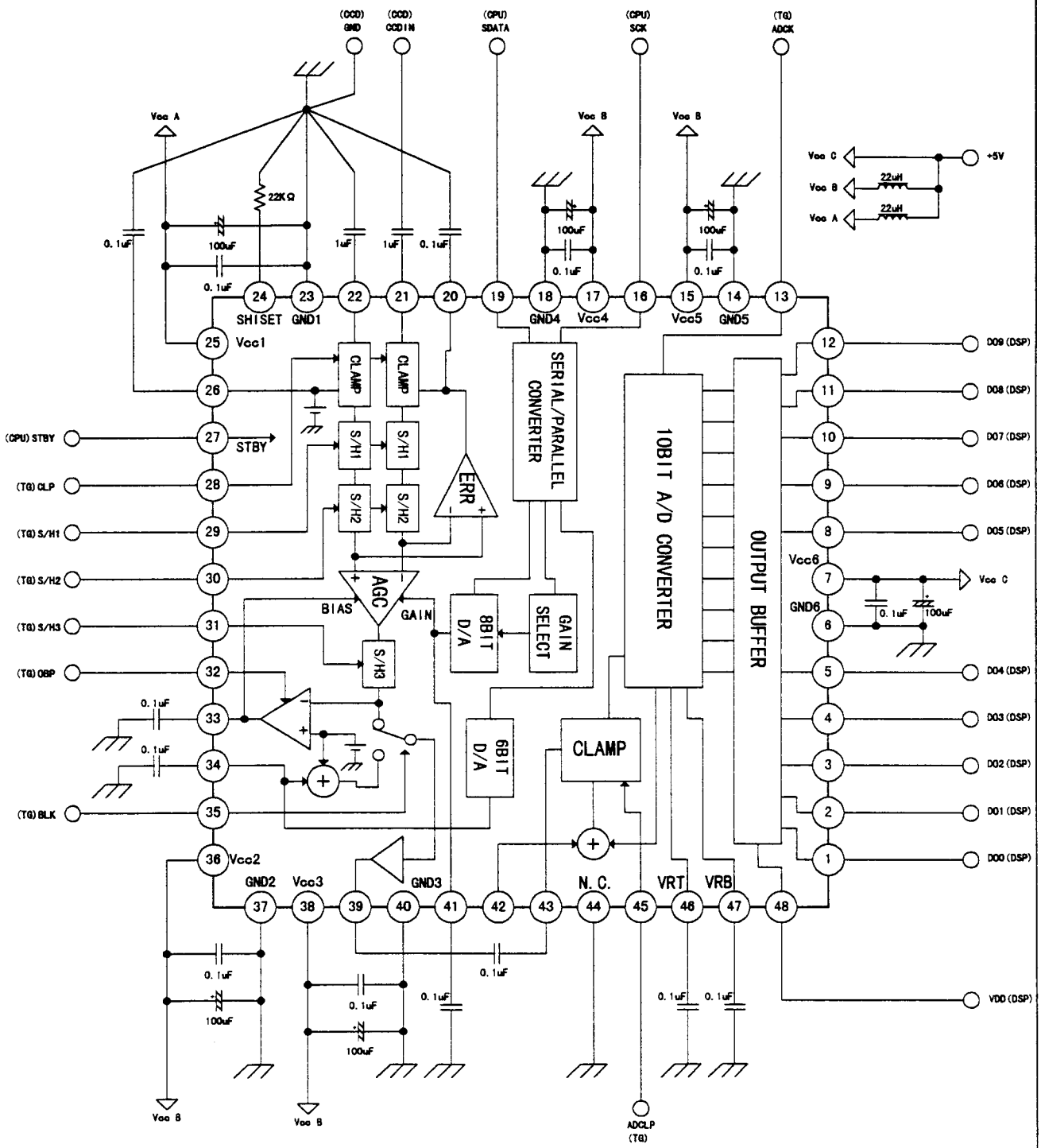
12. Measurement Waveforms



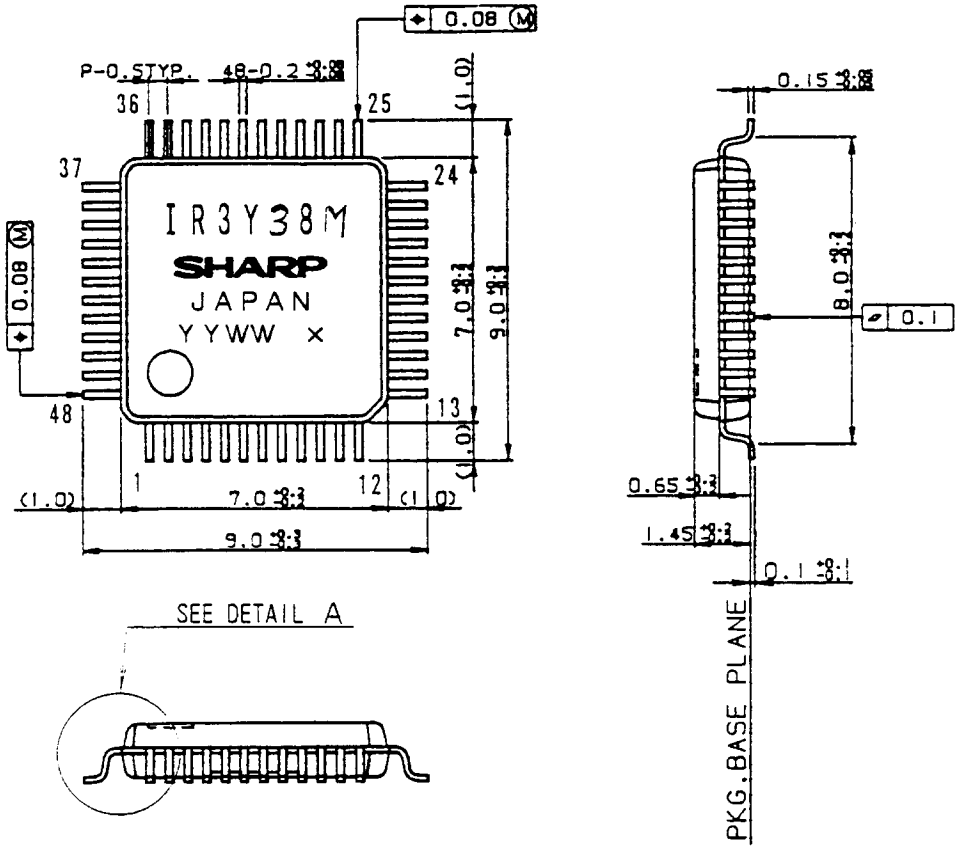
13. Measurement Circuit

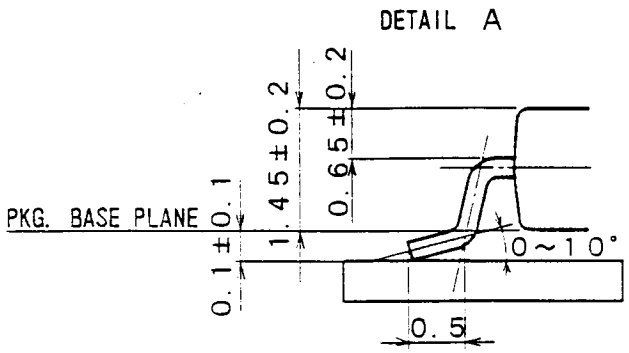


14. Application Circuit Example



15. Package Outline





名称 NAME	QFP48-P-0707	リード仕上 LEAD FINISH	TIN-LEAD PLATING	単位 UNIT	mm
シャープ株式会社 SHARP CORP.	IC事業本部 IC GROUP		DRAWING NO.	AA1035	

備考 プラスチックパッケージ外形寸法は、バリを含まないものとする。

NOTE Plastic body dimensions do not include burr of resin.