SHARP

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To ;

SPECIFICATIONS

Product Type MONOCHROME CCD SIGNAL PROCESS

Model No. IR3Y30M

※This specifications contains 33 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE:

BY:

PRESENTED

BY: T. Ohno
T. OHNO
Dept. General Manager

REVIEWED BY: K. Hatanaka

PREPARED BY: S. Okuda

Devices Engineering Dept.
TENRI Division
Tenri Integrated Circuits Group
SHARP CORPORATION

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●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- ·Office electronics
- ·Instrumentation and measuring equipment
- ·Machine tools
- ·Audiovisual equipment
- ·Home appliances
- ·Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- ·Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- ·Mainframe computers
- ·Traffic control systems
- ·Gas leak detectors and automatic cutoff devices
- ·Rescue and security equipment
- ·Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- ·Aerospace equipment
- ·Communications equipment for trunk lines
- ·Control equipment for the nuclear power industry
- ·Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

CONTENTS

1 Description

(1)Description

The IR3Y30M is one-chip signal processing IC for monochrome CCD video cameras. Since it has built-in low-pass filter and delay line, it makes possible both downsizing and cost reduction of the finished set.

(2)Features

1.Can handle signals from the CCD output to 75Ω video output.
2.Built-in the capasitor for clamp and sample-hold.
3.Wide AGC range (-3 to 29dB)
4.Built-in operational amplifier.
5.Built-in low-pass filter.
6.Built-in the comparator for electronic iris control.
7.Built-in aperture circuit and delay line.
8.Low power dissipation (265mW(typ))

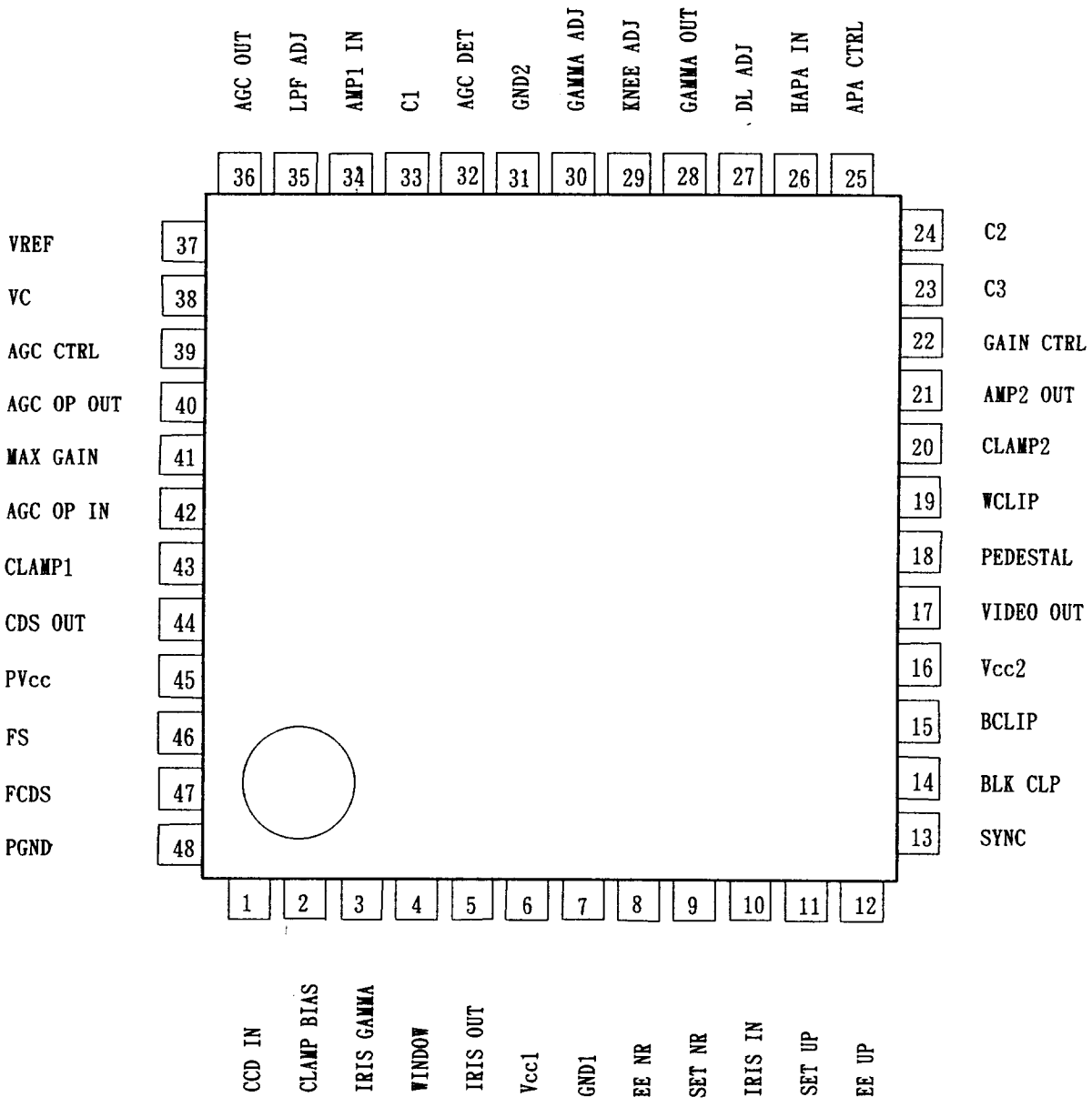
Not designed or rated as radiation hardened

Packaging material:	Plastic
Chip material and wafer substrate type:	P type silicon
Number of pins and package type:	48-pin quad-flat Package
Process(structure):	Bipolar

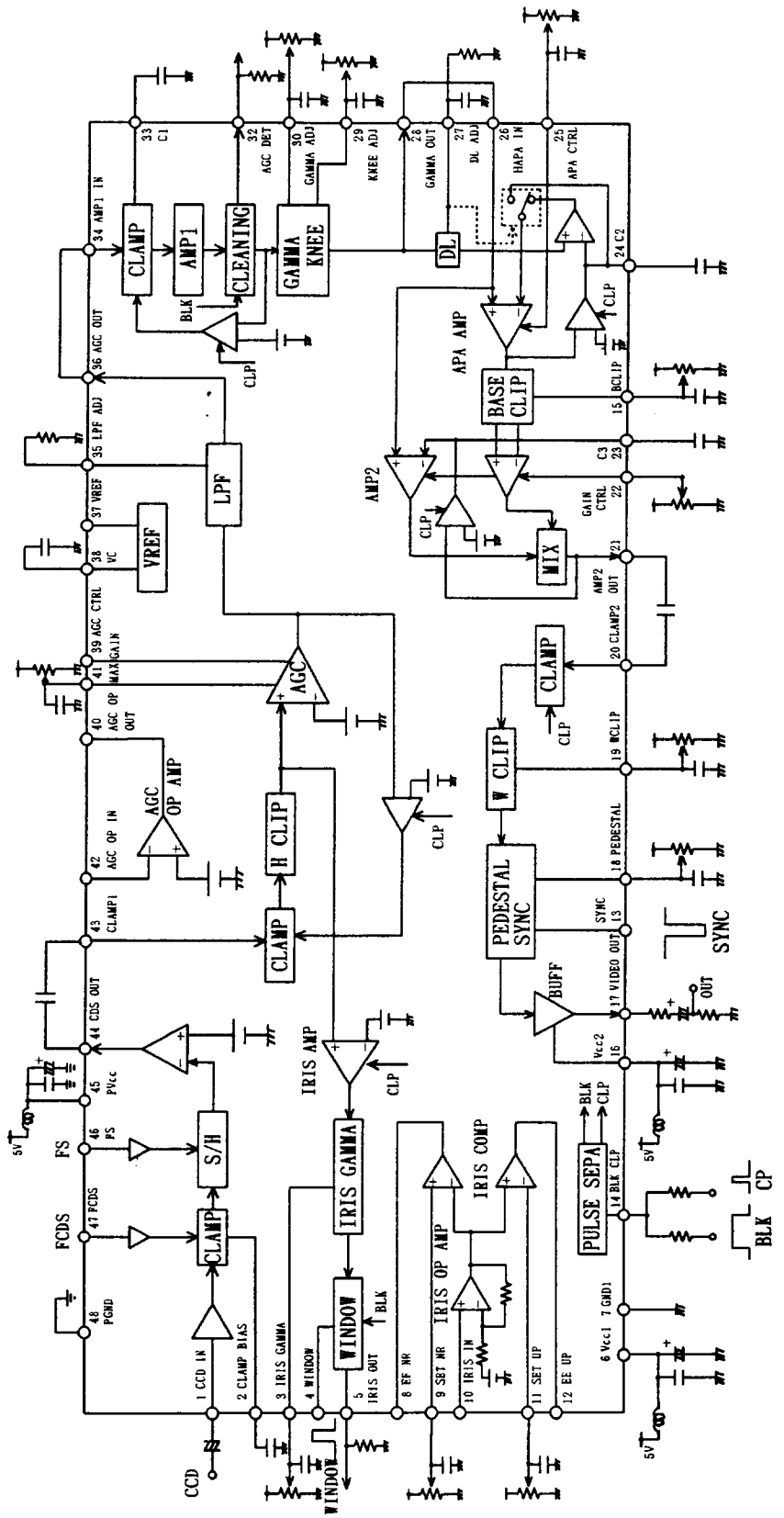
(3)Applications

Monitor camera, TV doorphone camera

2 Terminal Connections



3 Block Daigram



4 Description of Functional Operation

(1)Function of terminals

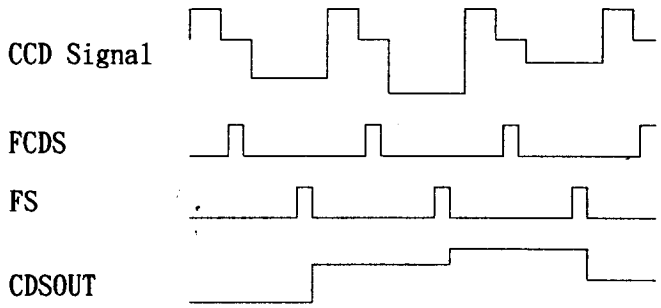
Term No	Name	Voltage	Function
1	CCDIN	2.5V	Input for the signal from CCD area sensor. 2.5V bias applied internally.
2	CLAMP BIAS	2.9V	Feedthrough level of the input signal is clamped to this terminal voltage. 2.9V bias applied internally. Connect capacitor between this terminal and GND.
3	IRIS GAMMA	3.1V	Gamma adjustment of the iris circuit. This terminal is preseted 3.1V, and Gamma becomes 0.45 at open.
4	WINDOW		Window pulse input for the iris circuit.Outputs the sinal while "H".
5	IRIS OUT	2.3V	Output for the iris signal.Connect a resistor between this terminal and GND
6	Vcc1		Power supply for analog circuits
7	GND1		Ground for analog circuits
8	EE NR		Comparqtor output for electronic iris control.
9	SET NR		High reference voltage input of the comparator for electronic iris control.
10	IRIS IN		Input of the amplifier for iris control This amplifier has 5 times gain.
11	SET UP		Low reference voltage input of the comparator for electronic iris control.
12	EE UP		Output of the comparator for electronic iris control.
13	SYNC		Synchronizing signal input.
14	BLK CLP		Composite pulse input. (pulse for optical black clamp and pulse for blanking)
15	BCLIP		Adjustment for the base clip level in the aperture circuit. Eliminate the low-level noise of aperture signal. At opened, base clip cancel.
16	Vcc2		Power supply for output amplifier circuits
17	VIDEO OUT	1.5V	Video signal output. at 75Ω terminated : 1Vp-p (Sync 0.3Vp-p)
18	PEDES-TAL	2.5V	Blanking level adjustment. 100mV at opened.
19	WCLIP	3.3V	White clip adjustment. 120% at opened.

Term No	Name	Voltage	Function
20	CLAMP2	2.3V	Input for encoder circuit. Black level of input signal is clamped to 2.3V
21	AMP2 OUT	1.0V	Output for the gain control amplifier
22	GAIN CTRL	2.5V	Control the output amplitude at terminal No.21 . Gain is controled in the range from 6 to 12 dB. It is approximately 10 dB when this pin is opened.
23	C3	1.8V	Feedback clamp detector. Connect capacitor between this terminal and GND
24	C2	1.8V	Feedback clamp detector. Connect capacitor between this terminal and GND When the external DL circuit is used, it will be input terminal to make aperture signal.
25	APA CTRL	1.8V	Adjustment for the horizontal aperture amount. It is approximately 12 dB when this terminal is open.
26	HAPA IN		Input for signal from terminal No.28 . This signals is used as main signals when aperture signals are mixed.
27	DL ADJ	1.2V	Adjustment for built-in delay line. When 200kΩ resistor is connected between this terminal and GND, delay line can be turned off.
28	GAMMA OUT	2.3V	Gamma and knee processed signal output.
29	KNEE ADJ	2.8V	Knee adjustment. 120% at opened.
30	GAMMA ADJ	2.0V	Gamma correction adjustment. 0.7 at opened.
31	GND2		Ground for analog circuits
32	AGC DET	2.0V	Signal output for AGC control. Connect resistor between this terminal and GND.
33	C1		Feedback clamp detector. Connect capacitor between this terminal and GND
34	AMP1 IN		Input for gamma and knee signal process

Term No	Name	Voltage	Function
35	LPF ADJ		Adjustment for built-in LPF characteristic. When connected resistor is 220kΩ or more between this terminal and GND, LPF can be turned off.
36	AGC OUT	2.3V	AGC processed signal output.
37	VREF	2.0V	Reference voltage.
38	VC	2.0V	Bias for reference voltage. Connect capacitor between this terminal and GND.
39	AGC CTRL		Gain control for AGC amplifier. Be sure to input the voltage within the range from 2 to 4V.
40	AGC OP OUT		Output of the operation at amplifier for AGC control.
41	MAX GAIN	3.3V	Adjustment for AGC amplifier maximum gain.Maximum gain is 18 dB at opened. When applied voltage is 0.62V or less, AGC circuit tern off and the amplifier is fixed at 0 dB.
42	AGC OP IN		The operational amplifier for AGC control.
43	CLAMP1	2.0V	Input of AGC amplifier. Black level is clamped at 2.0V .
44	CDS OUT	2.4V	CDS processed signal output.
45	PVcc		Power supply for pulse circuits
46	FS		Pulse input for sample-hold
47	FCDS		Pulse input for feedthrough level clamp
48	PGND		Ground for Pulse circuits

(2)Description of operations

*CDS
The feed-through level of the input signal is clamped by the clamp circuit. Then the signal period is sampled and other period are hold by the sample and hold circuit, so that signals can be obtained.



*Highlight clip
Before the AGC circuit, excessive signals more than approximately 0.5Vp-p are clipped.

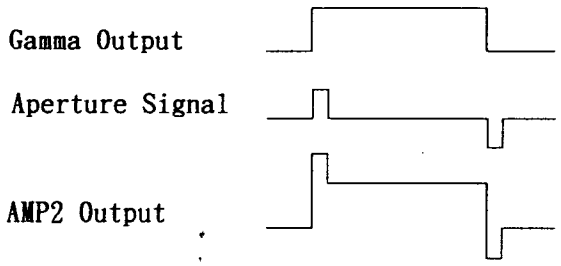
*AGC
The amplitude of output signals from AGC amplifier is externally detected and the gain is controlled with control signals from the AGC operational amplifier. Decreasing voltage at pin No.41 to 0.62V or less causes the amplifier to be fixed at 0dB.

*LPF
The characteristics can be controlled with an external resistor at pin No.35. Increasing the resistor to 220kΩ or more allows signals passing over the LPF to be output.

*Gamma and knee corrections
In order to comply with the characteristics of CRT, the high-bright part is suppressed. Pin No.29 and 30 can be used to control this suppression. If voltage at pin NO.30 is increased to 4V or more gamma will be 1.

*Iris
Signals which have not been processed by AGC are amplified, suppressed by gamma correction, and then output. Control signals can be generated by inputting the above signals to pin No.10 after detecting them.

*Aperture
The video articulation can be increased by enhancing the signal contour. If the built-in delay line is not used, it can be turned off by using an external resistor of 200kΩ minimum at pin No.27.
To control the aperture amount, use base clip.



*Output circuit
The load of 75Ω can be driven directly. In addition, the pedestal level can be controlled vertically.

(3)Cautions

*To control the aperture amount, apply base clip by controlling pin No.24.

*Avoid connecting or disconnecting an external resistor at pin No.27 to refrain from the malfunction of the built-in delay line.

*Use the shortest distance to connect the bypass capacitors between the power supply and ground pins. The addition or removal of any external component should be determined depending on how the existing components are mounted.

*This device is electronic sensitive. Please handle only ay electrostatic safe work stations.

(4)Input/Output Circuit Types

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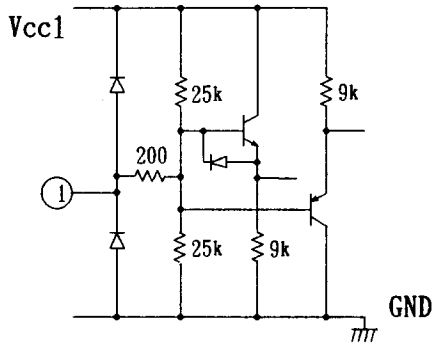
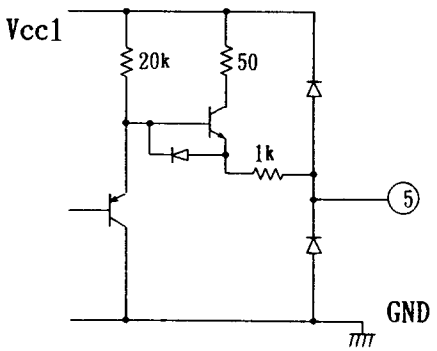
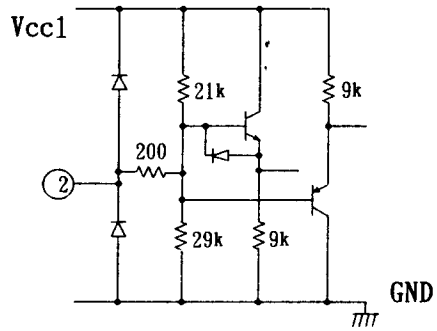
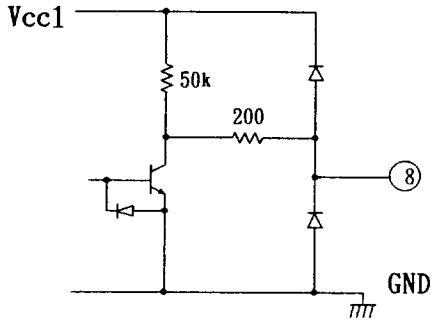
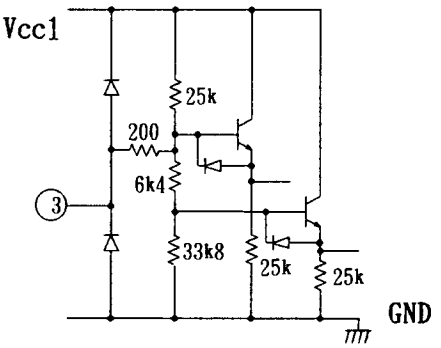
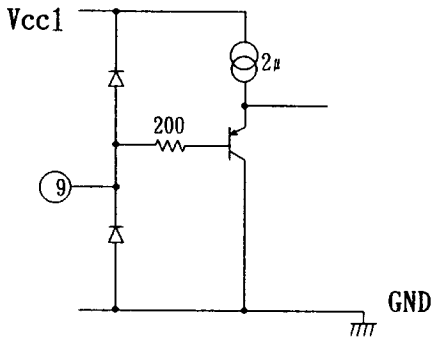
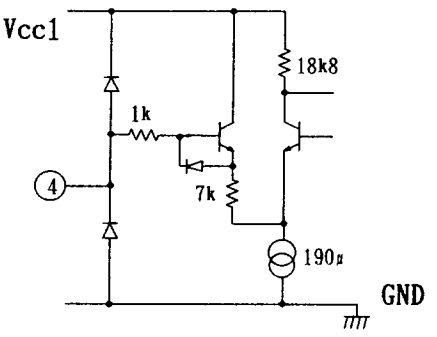
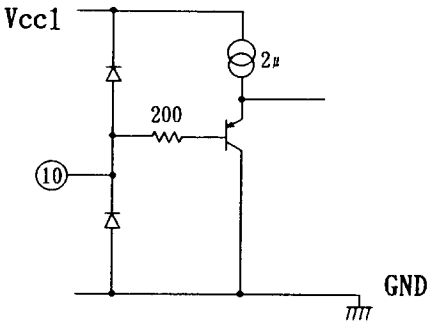
1		5	
2		8	
3		9	
4		10	

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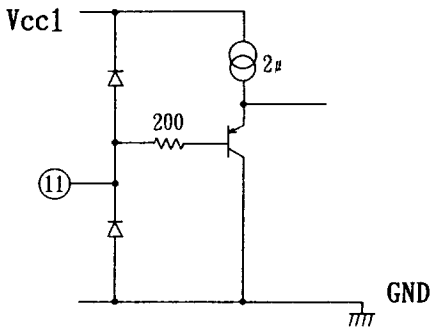
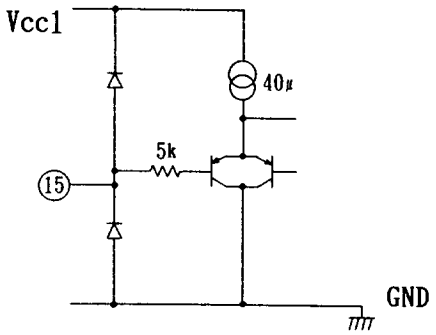
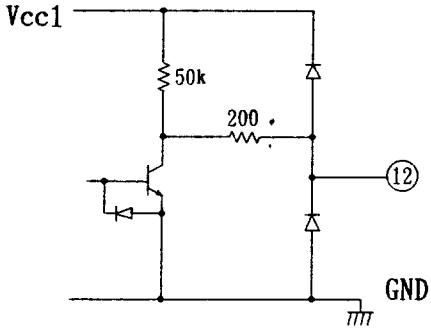
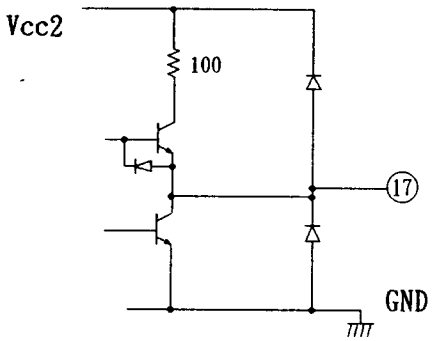
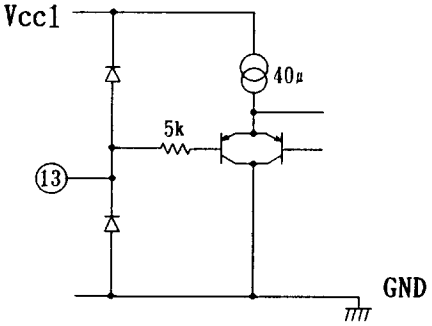
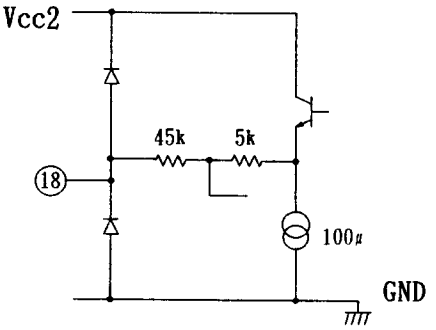
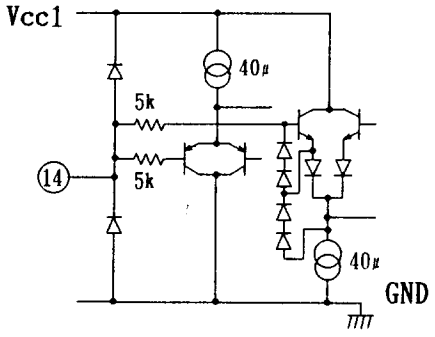
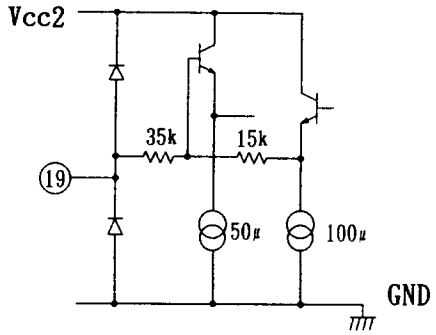
11		15	
12		17	
13		18	
14		19	

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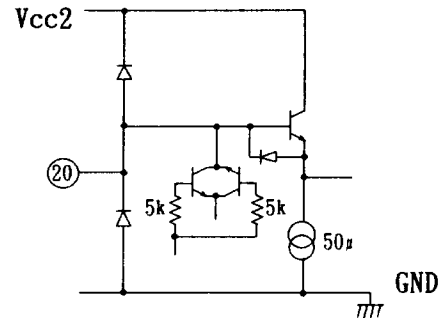
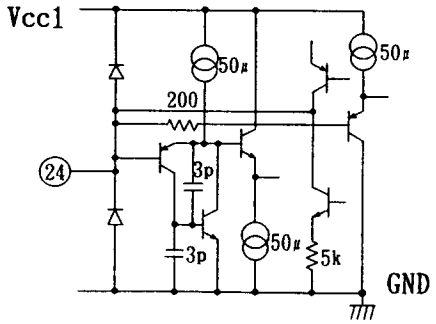
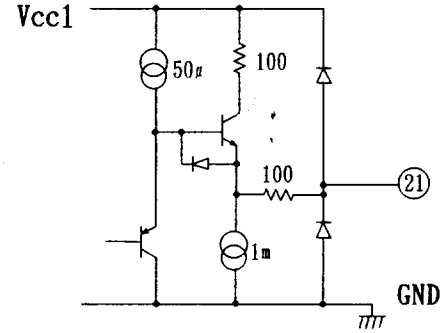
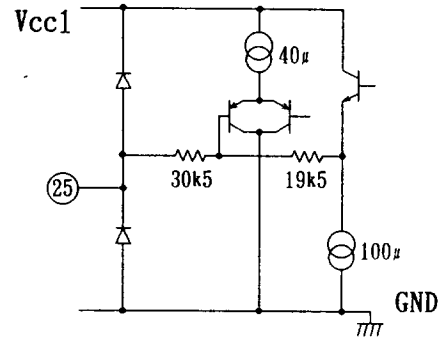
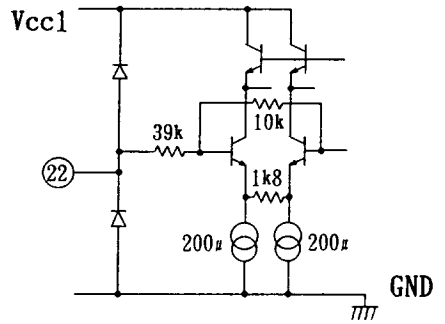
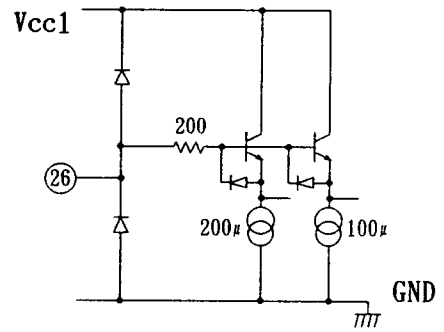
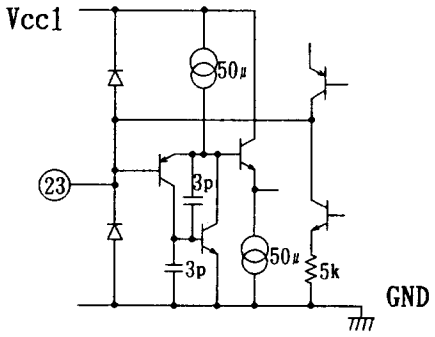
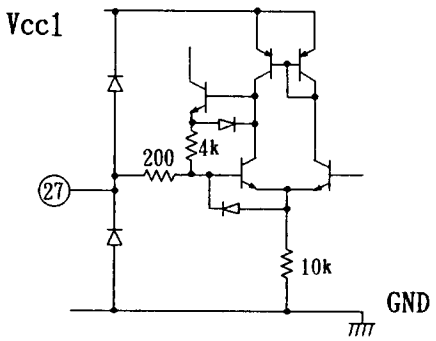
20		24	
21		25	
22		26	
23		27	

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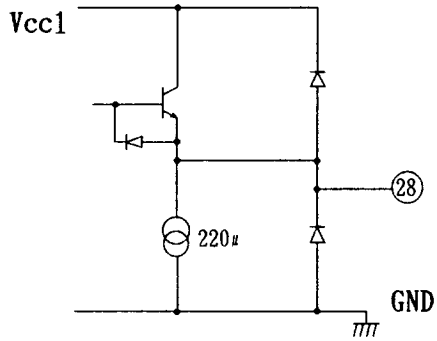
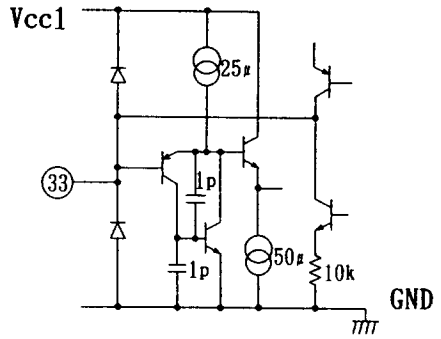
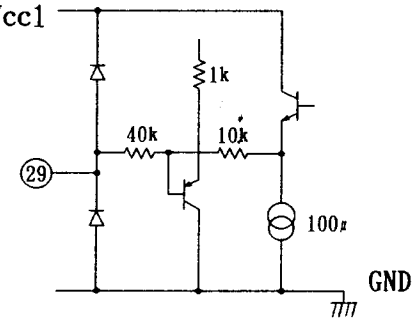
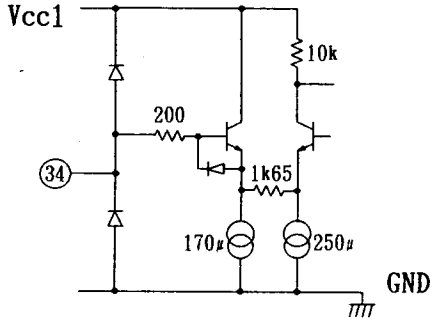
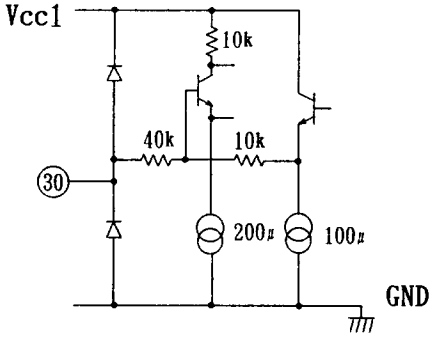
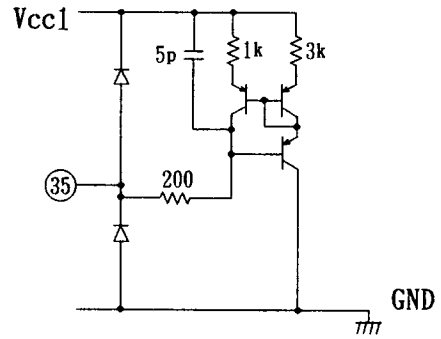
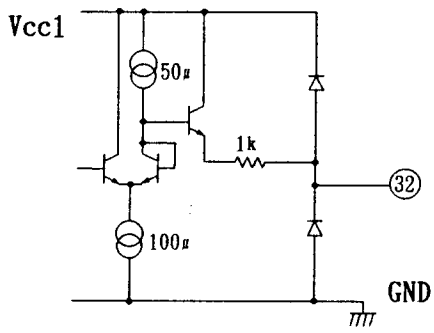
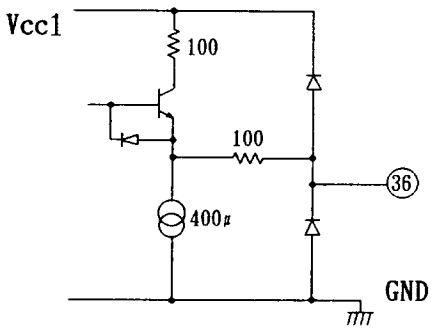
28		33	
29		34	
30		35	
32		36	

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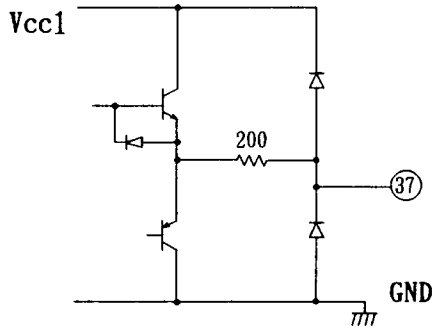
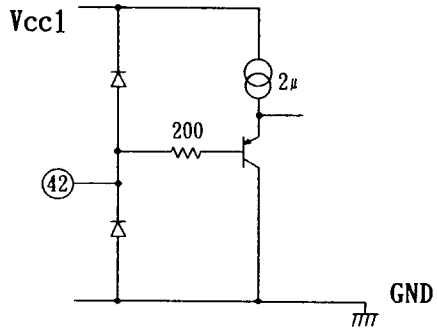
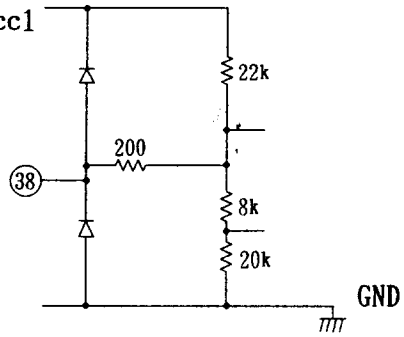
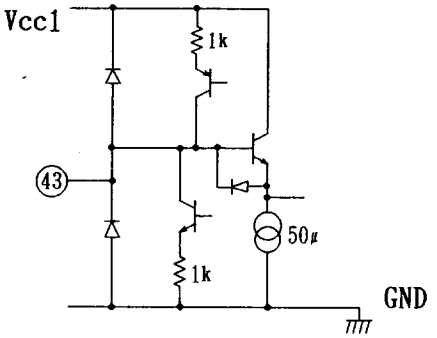
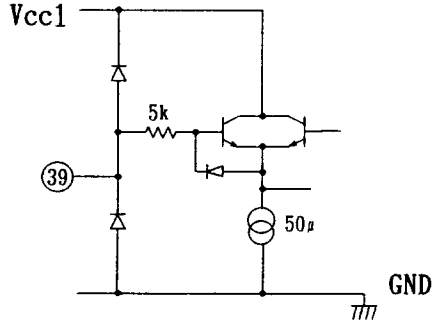
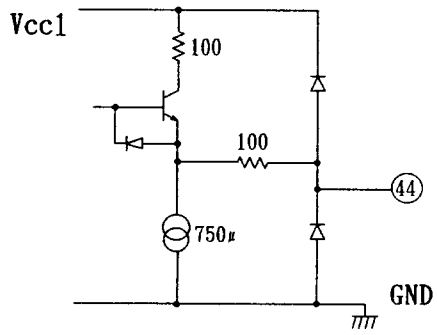
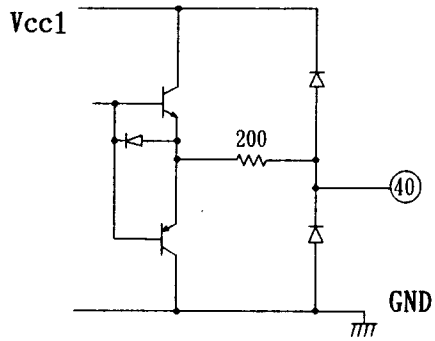
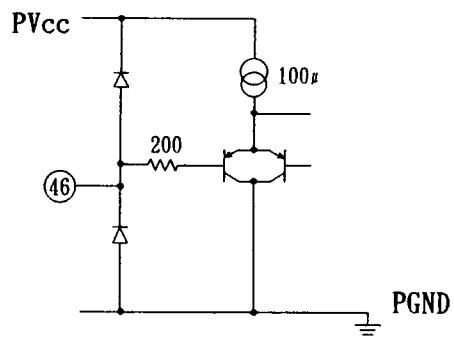
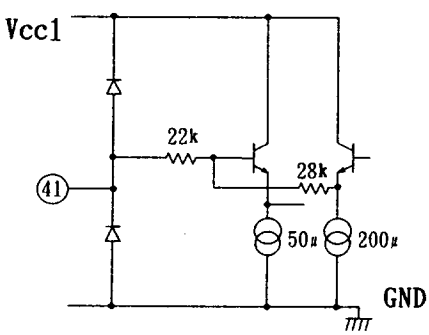
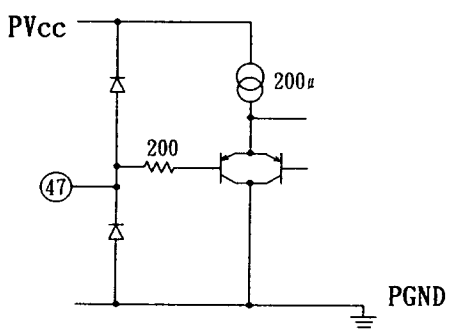
37		42	
38		43	
39		44	
40		46	
41		47	

5 Absolute Maximum Ratings

(Unless otherwise specified, Ta=25℃)

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	Vcc1, 2		7	V
	PVcc		7	V
Input voltage	Via	Except for Pins 46, 47	Vcc	V
	Vip	Pins 46, 47	−0.2～PVcc+0.2	V
Comparator Output voltage	Vsd		Vcc	V
Power dissipation	P_D	Ta ≦ 25℃	725	mW
P_D derating ratio		Ta > 25℃	5.8	mW/℃
Operating temperature	Topr		-30~+ 75	℃
Storage temperature	Tstg		-55~+150	℃

Operating Conditions

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	Vcc	Pins, 6, 16 and 45	4.75~5.25	V
H-Aperture signal	Vh-ap	Pin 26	MAX 600	mVp-p
Standard CCD input signal	Vccd	Pin 1	TYP 200	mVp-p
Clamp pulse width	Tfs	Pin 46		
Sample-hold pulse width	Tfcds	Pin 47	MIN 15	ns

6 Electrical Characteristics

(1)Electrical Characteristics

Unless otherwise specified Ta=25℃, Vcc=5.0V, SW Conditions ⟶(a)
V26=2.3V, V34=2.0V, V39=3V
R27=30kΩ, R35=22kΩ

NO	Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
1	Current dissipation	Icc1	Measure pin 6.			43.0	54.5	mA
		Icc2	Measure pin 16.			5.7	7.8	mA
		Icc3	Measure pin 45.			4.3	5.4	mA
	CDS circuit							
2	Low frequency attenuation	G_{LF}	With signal 1 applied to SG1, measure the signal attenuation on TP44. FS=5V, FCDS=Signal 2(FCDS) V_A=TP44 amplitude(f=100kHz), V_B=TP44 amplitude(f=10MHz) $G_{LF}=20*LOG(V_A/V_B)$			-30	-25	dB
3	Gain	G_{CDS}	Signal 2 applied to SG1, FS and FCDS, measure the amplitude on TP44. SG1=200mVp-p, f=10MHz		-2	0	2	dB
4	Clamp bias	$V_{CP/BIAS}$			2.7	2.9	3.1	V
	AGC operational amplifier circuit							
5	Low level	A_{OPL}	Measure the voltage on TP40B. SW40, SW42→(b)	V42=3V, I40=+200μA		1.0	1.2	V
	High level	A_{OPH}		V42=1V, I40=-200μA	3.9	4.1		
	Iris operational amplifier, comparator circuit							
6	Operational amplifier gain	G_{OP}	With V10=2.3V, measure the voltage of V9a(TP8:L→H) and V11a(TP12:H→L). With V10=2.4V, measure the voltage of V9b(TP8:L→H) and V11b(TP12:H→L) G_{OP}=(V9b-V9a)or(V11b-V11a) SW9, SW10, SW11→(b)		0.40	0.46	0.51	V
7	Comparator low level	I_{OPL}	Change the voltage of V9, V11, and measure the voltage on TP8, TP12. V10=2.3V SW9, SW10, SW11→(b)			0	0.2	V
	high level	I_{OPH}			4.70	4.95		

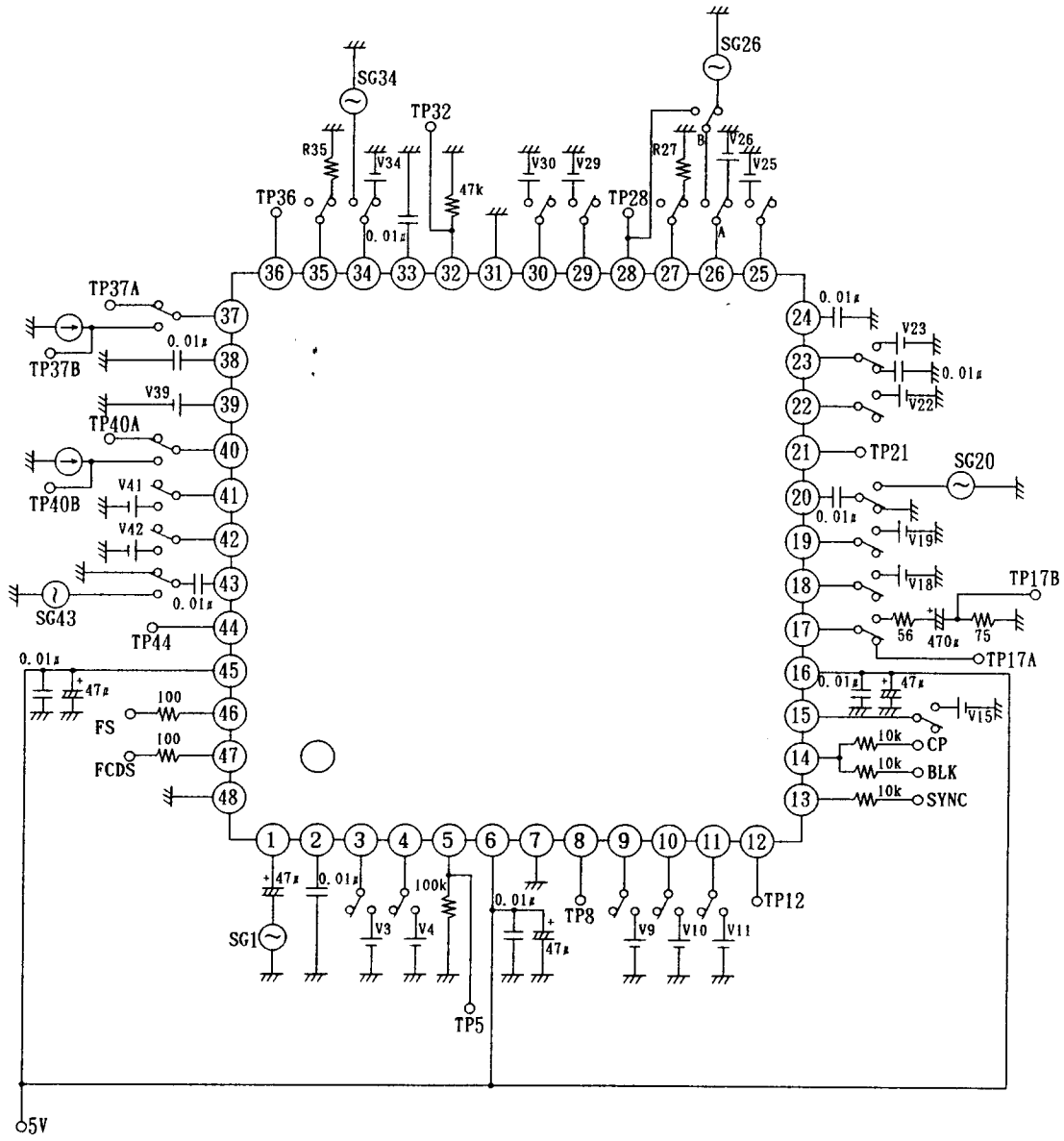
NO	Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
	AGC circuit							
8	Highlight clip level	H_{CL}	Change The amplitude of signal 3 which is applied to SG43, and measure the amplitude on TP36 when TP36's output signal is clipped. SW43, SW41→(b), Pulse→CP, V41=0V, R35=220kΩ		0.4	0.5	0.6	Vp-p
9	AGC MAX gain(1)	G_{AMAX1}	Signal 3 applied to SG43, measure the amplitude on TP36. GA1~4=20*LOG(TP36 amplitude/SG43 amplitude) SW41, SW43→(b) Pulse→CP, R35=220kΩ	SG43=20mVp-p V39=4V, V41=5V	27	29	31	dB
	AGC MAX gain(2)	G_{AMAX2}		SG43=20mVp-p V39=4V, SW41→(a)	15.5	18.0	20.5	
	AGC MIN gain	G_{AMIN}		SG43=400mVp-p V39=2V, V41=5V	-6.5	-3.5	-0.5	
	AGCOFF gain	G_{AOFF}		SG43=200mVp-p V39=4V, V41=0V	-2	0	2	
10	Output dynamic range	D_A	Signal 3 applied to SG43, measure the amplitude on TP36. SG43=50mVp-p SW41, SW43→(b), Pulse→CP, V39=4V, V41=5V, R35=220kΩ		0.55	0.75		Vp-p
11	Frequency characteristic(1)	f_{A1}	Apply signal 4 to SG43. Increase the frequency of the signal 4 until the frequency components of the signal on TP36 are 3dB lower than that at f=100kHz, and measure the frequency of the signal 4. SW41→(b), Pulse→CP, V41=5V When measure (2)case, adjust the V39 such that the amplitude of the output on TP36 is 200mVp-p	SG43=10mVp-p R35=22kΩ, V39=4V	3.5	4.5		MHz
	Frequency characteristic(2)	f_{A2}		SG43=200mVp-p R35=220kΩ	7.0	10.0		
	Frequency characteristic(3)	f_{A3}		SG43=10mVp-p R35=22kΩ, V39=4V f=9.5MHz		-35	-25	dB
12	AGC ON/OFF switching voltage	V_{AGC}	Signal 3 applied to SG43, change V41, and measure the voltage of V41 when the gain on TP36 change from -3.5dB to 0dB. The gain on TP36:20*LOG(TP36 amplitude/SG43 amplitude) SG43=400mVp-p, SW43, SW41→(b), Pulse→CP, V39=2V, R35=220kΩ		0.4	0.6	0.8	V
13	Reference voltage 1	V_{REF}	Measure the voltage on TP37A.		1.84	1.94	2.04	V
	Reference voltage 2	ΔV_{REF2}	With I37=+500μA, measure the change in voltage on TP37B. SW37→(b)		0	0.15	0.30	V
	Reference voltage 3	ΔV_{REF3}	With I37=-500μA, measure the change in voltage on TP37B. SW37→(b)		-0.30	-0.15	0	V

NO	Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
	Iris circuit							
14	Iris AMP gain	G_I	Signal 3 applied to SG43, measure the amplitude on TP5. SW3, SW4, SW43→(b) Pulse→CP, BLK	SG43=200mVp-p V3=5V, V4=5V	10.5	11.5	12.5	dB
15	γ output level	γ_{PRE}		SW3→(a)	0.25	0.32	0.40	Vp-p
16	Output dynamic range	D_I		SG43=800mVp-p V3=5V, V4=5V	1.5	1.9		Vp-p
17	Black level	B_I	Measure the voltage on TP5. SW4→(b), Pulse→CP, BLK, V4=0V		2.15	2.30	2.45	V
18	Black level offset1	B_{IOFF1}	Measure the voltage on TP5. SW4→(b), Pulse→CP, BLK	V4=5V	-50	0	50	mV
	Black level offset2	B_{IOFF2}		V4=0V	-50	0	50	
19	Frequency characteristic	f_I	Apply signal 4 to SG43. Increase the frequency of the signal 4 until the frequency components of the signal on TP5 are 3dB lower than that at f=100kHz, and measure the frequency of the signal 4. SG43=200mVp-p, V4=5V, SW4, SW43→(b), Pulse→CP, BLK		0.7	1.1		MHz
20	Window OFF output level	O_{WOFF}	Signal 3 applied to SG43, measure the amplitude on TP5. SG43=200mVp-p, SW4, SW43→(b), Pulse→CP, BLK, V4=0V			40	70	mVp-p
21	Window ON switching voltage	V_W	Same as in the Window OFF output level measurement. Increase V4, and measure V4 when the amplitude of output signal on TP5 is not changed.		1.2	1.4	1.6	V
22	Window input current	I_W	With V4=5V, measure input current on pin 4. SW4→(b)		0.5	1.2	3.0	μA
	AMP1 circuit							
23	AMP1 gain	G_{AMP1}	Signal 3 applied to SG34, measure the amplitude on TP32. SW34→(b), Pulse→CP, BLK, SG34=100mVp-p, Black level=2V		13	14	15	dB
24	Output dynamic range	D_{AMP1}	Same as in the AMP1 gain measurement. Measure output dynamic range on TP32.		1.20	1.40		Vp-p
25	Black level	B_{AMP1}	Measure the voltage on TP32. Pulse→CP, BLK		1.9	2.0	2.1	V

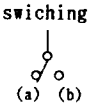
NO	Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
	γ, knee circuit							
26	γ gain(1)	$G_{\gamma 1}$	Signal 3 applied to SG34, measure the amplitude on TP28. Input black level=2V SW34→(b), Pulse→CP, BLK	SG34=100mVp-p	310	410	510	mVp-p
	γ gain(2)	$G_{\gamma 2}$		SG34=30mVp-p		-6.4		dB
	γ gain(3)	$G_{\gamma 3}$		SG34=200mVp-p		1.3		
27	γ OFF gain	$G_{\gamma OFF}$	Signal 3 applied to SG34, measure the amplitude on TP28. SW29, SW30, SW34→(b), Pulse→CP, BLK SG34=100mVp-p, Black level=2V, V29=5V, V30=5V		450	510	580	mVp-p
28	Cleaning offset	(1) C_{L1}	Measure the amplitude of TP28 between BLK level and black level. Pulse→CP, BLK	SW30→(a)	-50	0	50	mV
		(2) C_{L2}		SW30→(b), V30=5V	-50	0	50	
29	Frequency characteristic	f_γ	Apply signal 4 to SG34. Increase the frequency of the signal 4 until the frequency components of the signal on TP28 are 3dB lower than that at f=100kHz, and measure the frequency of the signal 4. SW34→(b), Pulse→CP, BLK, SG34=100mVp-p, Black level=2V		6.0			MHz
	Aperture, AMP2 circuit							
30	Aperture gain MAX	G_{APMAX}	Signal 3 applied to SG26, measure the amplitude on TP21. SW26A→(b), Pulse→CP, BLK SG26=100mVp-p, black level=2.3V	SW25→(b), V25=5V	840	1130		mVp-p
	Aperture gain PRE	G_{APPRE}			740	840	940	
	Aperture gain MIN	G_{APMIN}		SW25→(b), V25=0V	320	420	520	
31	Base clip output	B_{CL}		SW15→(b), V15=0V, SW25→(b), V25=5V	250	350	450	
32	Delay line output	DL_{OUT}	Signal 3 applied to SG34, measure the amplitude on TP21. SW15, SW23, SW25, SW29, SW30, SW34→(b), Pulse→CP, BLK SG34=50mVp-p, Black level=2V, V15=V25=V29=V30=5V V23=1.2V, V26=2.3V		1100	1700		mVp-p
33	AMP2 MAX gain	$G_{AMP2MAX}$	Signal 3 applied to SG26, measure the amplitude on TP21. Pulse→CP, BLK SW15, SW22, SW25, SW26A→(b) Input black level=2.3V, V15=V25=0V	SG26=100mVp-p, V22=5V	370	440	510	mVp-p
	AMP2 MIN gain	$G_{AMP2MIN}$		SG26=100mVp-p, V22=0V	180	230	280	
34	Output dynamic range	D_{AMP2}		SG26=800mVp-p, V22=5V	2000	2550		
35	Frequency characteristic	f_{AMP2}	Apply signal 4 to SG26. Increase the frequency of the signal 4 until the frequency components of the signal on TP21 are 3dB lower than that at f=100kHz, and measure the frequency of the signal 4. SW15, SW25, SW26A, →(b), V15=0V, V25=0V, Pulse→CP, BLK, SG26=100mVp-p, Black level=2.3V		8.0			MHz

NO	Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
	Encoder circuit							
36	White clip(1)	W_{C1}	Signal 3 applied to SG20, measure the amplitude on TP17A. SW20→(b) Pulse→CP, BLK	SW19→(b), V19=5V	1.9	2.0		V
	White clip(2)	W_{C2}		SW19→(b), V19=0V		0.75	0.85	
	White clip preset	W_{CPRE}		SW19→(a)	1.75	1.85	1.95	
37	Setup(1)	S_{UP1}	Measure the amplitude of TP17A between BLK level and black level. Pulse→CP, BLK	SW18→(b), V18=5V	230	280		mV
	Setup(2)	S_{UP2}		SW18→(b), V18=0V		-310	-260	
	Setup preset	S_{UPPRE}		SW18→(a)	-150	-100	-50	
38	SYNC level	V_{SYNC}	Measure the amplitude of TP17A between SYNC level and black level. Pulse→CP, BLK, SYNC		530	580	630	mV
39	Gain	G_{out}	Signal 3 applied to SG20, measure the amplitude on TP17A. SW20→(b), Pulse→CP, BLK, SG20=1Vp-p		-1	0	1	dB
40	Output dynamic range	D_{OUT}	Signal 3 applied to SG20, measure the amplitude of TP17A between SYNC level and white level. SW19, SW20→(b) Pulse→CP, BLK, SYNC, V19=5V		2.2	2.5		Vp-p
41	Frequency characteristic	f_{OUT}	Apply signal 4 to SG20. Increase the frequency of the signal 4 until the frequency components of the signal on TP17B are 3dB lower than that at f=100kHz, and measure the frequency of the signal 4. SG20=1Vp-p, SW17, SW20→(b), Pulse→CP, BLK, SYNC		10			MHz
42	Output voltage	V_{OUT}	Signal 3 applied to SG20, measure the amplitude of TP17B between SYNC level and white level. SW17, SW20→(b) Pulse→CP, BLK, SYNC, SG20=1.3Vp-p		0.9	1.0		Vp-p
	Pulse circuit							
43	Threshold voltage		Voltage applied to FS, FCDS, SYNC, BLK and CLP、measure the threshold voltage of each circuit.					V
	clamp	V_{FCDS}				1.3		
	sample-hold	V_{FS}				1.5		
	sync	V_{SYNC}				2.5		
	blanking	V_{BLK}				1.5		
	clamp	V_{CP}				3.5		

(2)Test Circuit



1. swiching polarity

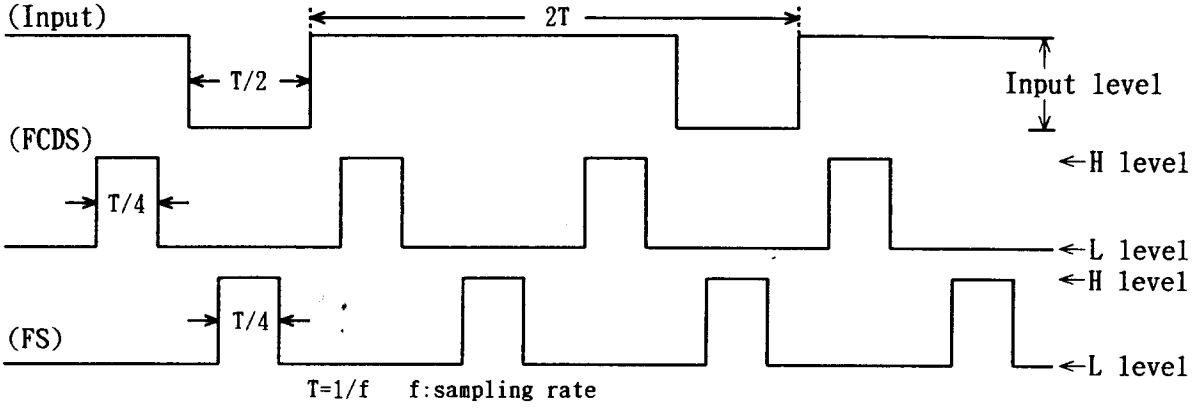


(3)Input Signals

Signal 1

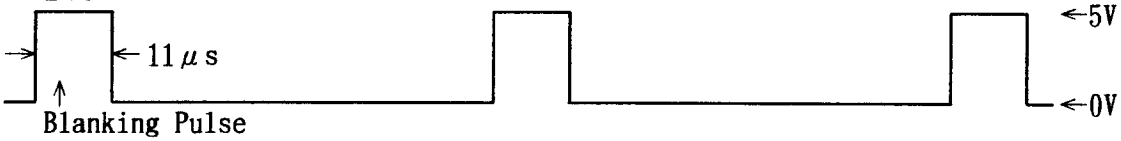
Sine wave amplitude:200mVp-p
Low frequency attenuation:100kHz/10MHz (10MHz=0dB)

Signal 2
(Input)



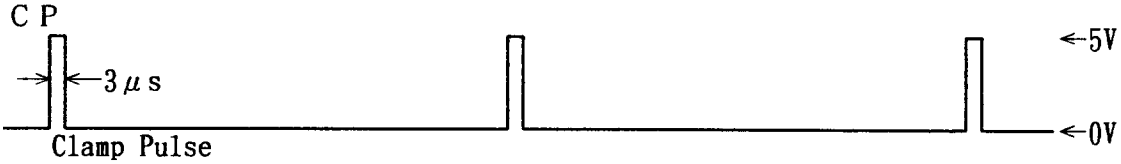
T=1/f f:sampling rate

BLK



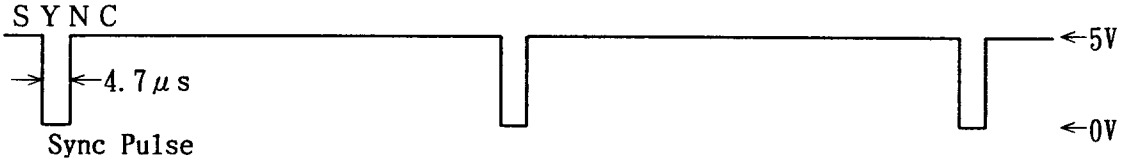
Blanking Pulse

CP



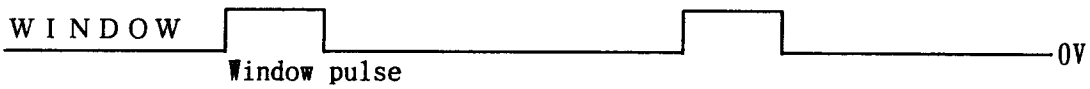
Clamp Pulse

SYNC



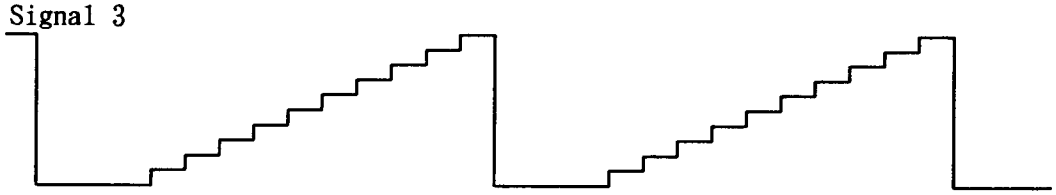
Sync Pulse

WINDOW

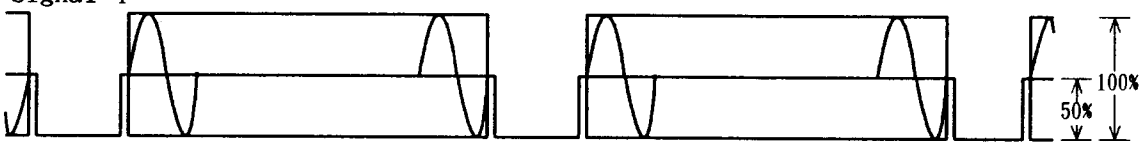


Window pulse

Signal 3



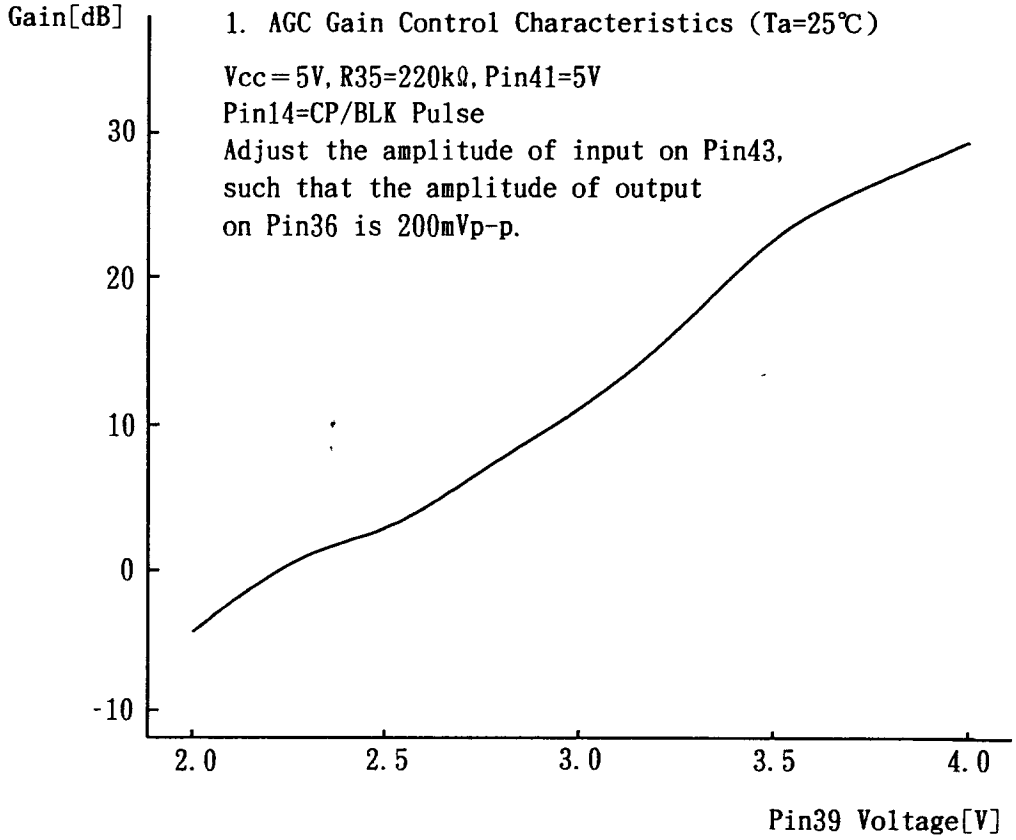
Signal 4



7. Typical Characteristic Example

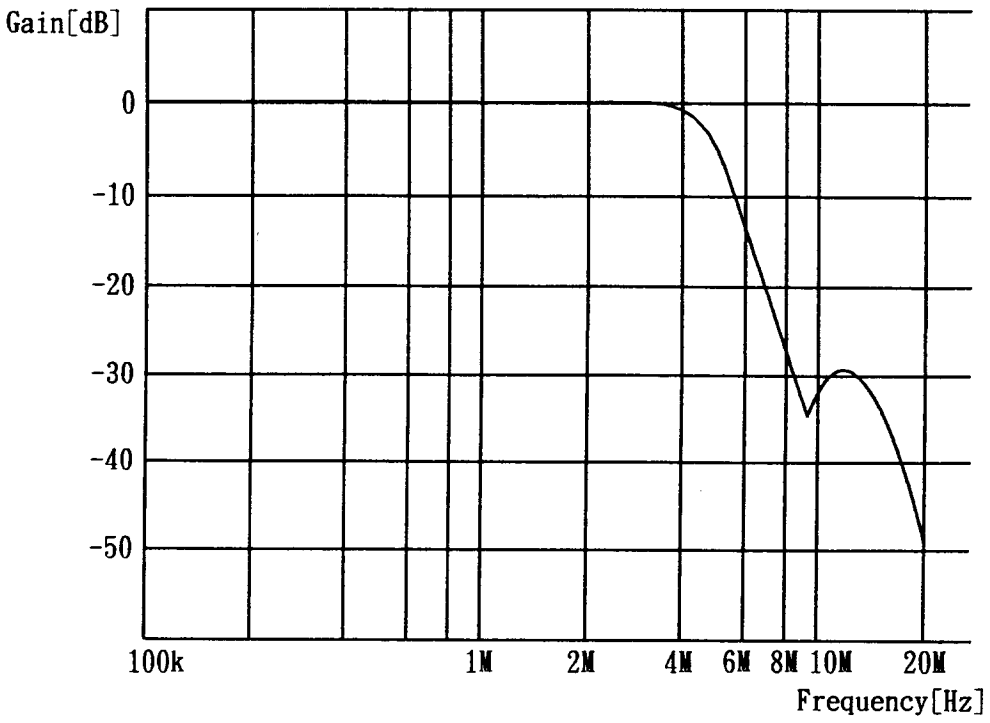
1. AGC Gain Control Characteristics (Ta=25℃)

Vcc=5V, R35=220kΩ, Pin41=5V
Pin14=CP/BLK Pulse
Adjust the amplitude of input on Pin43, such that the amplitude of output on Pin36 is 200mVp-p.

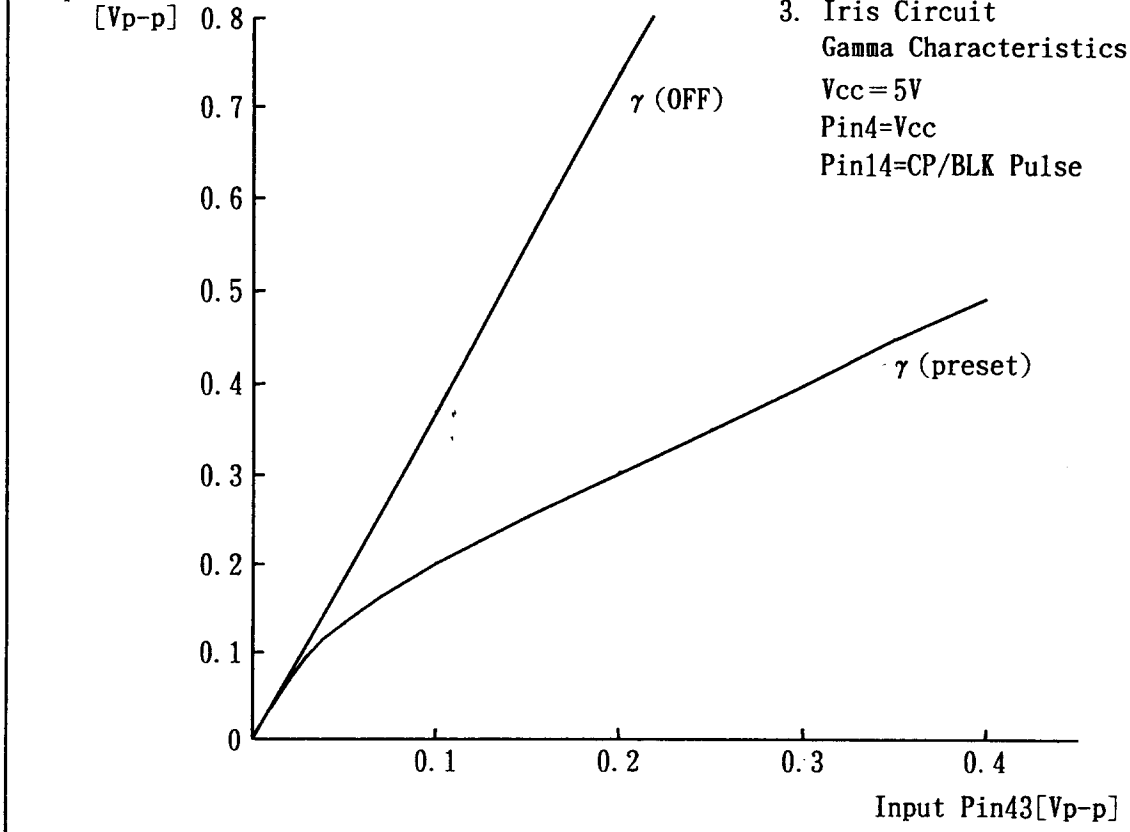


2. LPF Characteristics (Ta=25℃)

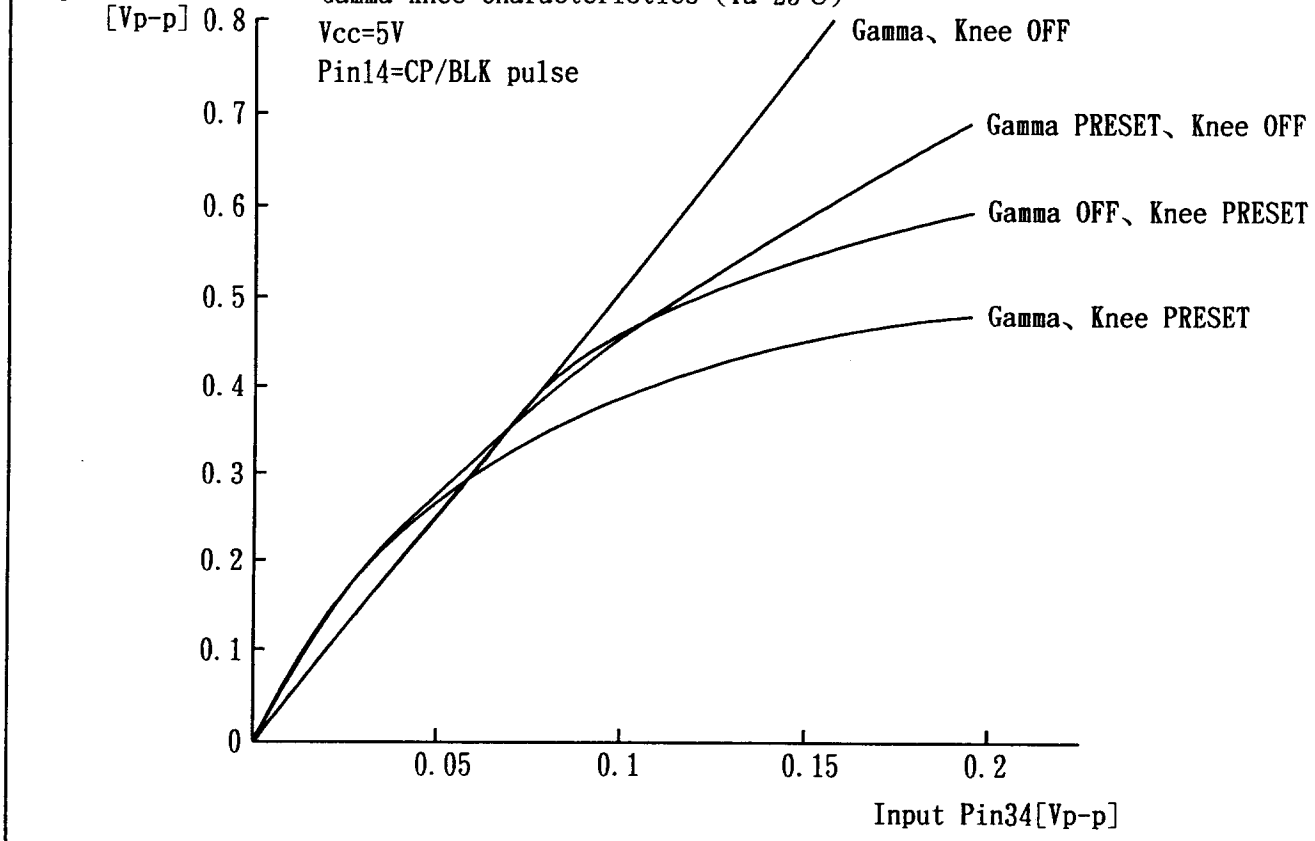
Vcc=5V
Pin41=0V, Pin14=CP/BLK pulse
R35=22kΩ, Pin43=10mVp-p, TP=Pin36

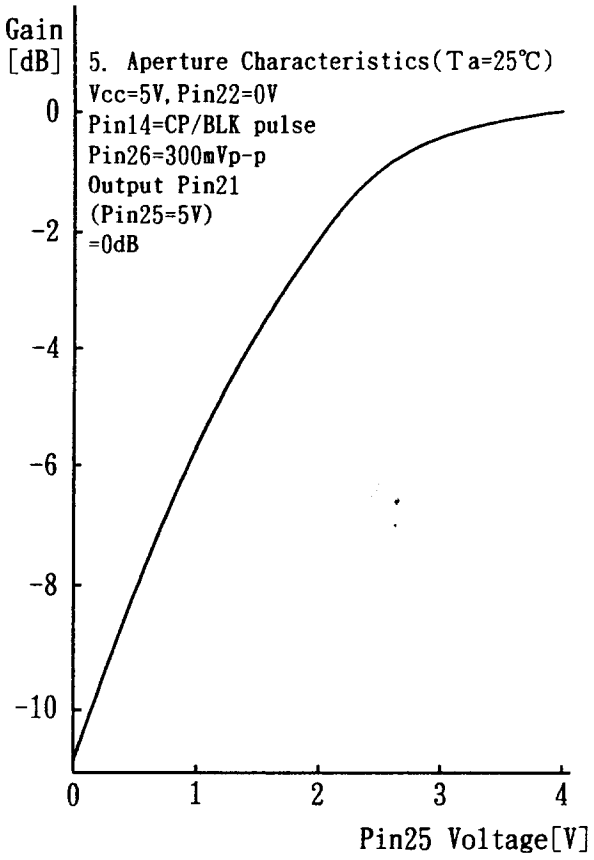


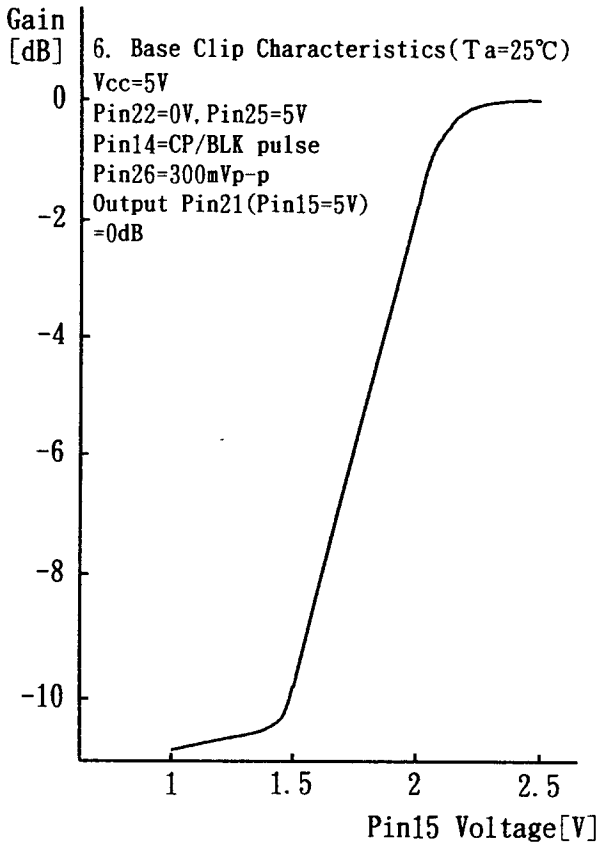
3. Iris Circuit
Gamma Characteristics (Ta=25℃)
Vcc=5V
Pin4=Vcc
Pin14=CP/BLK Pulse

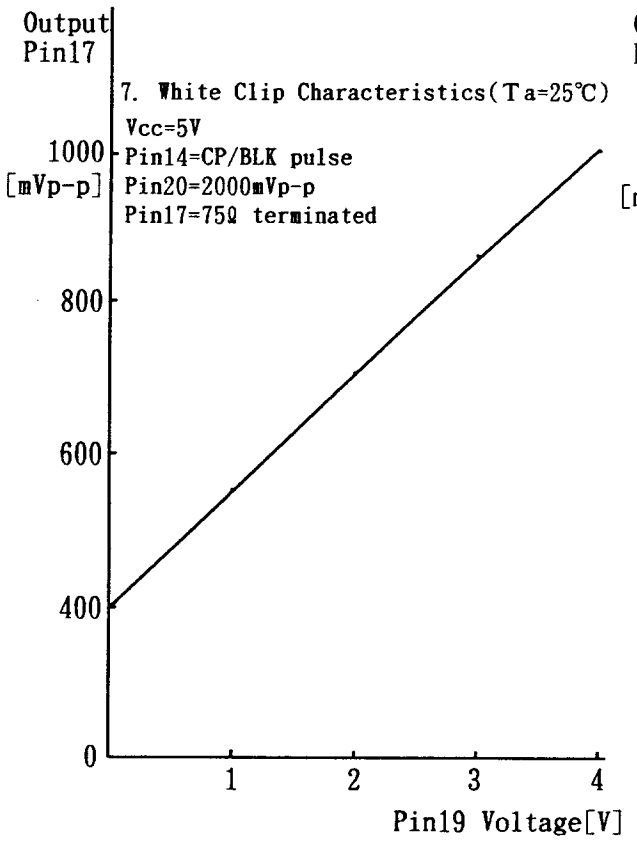


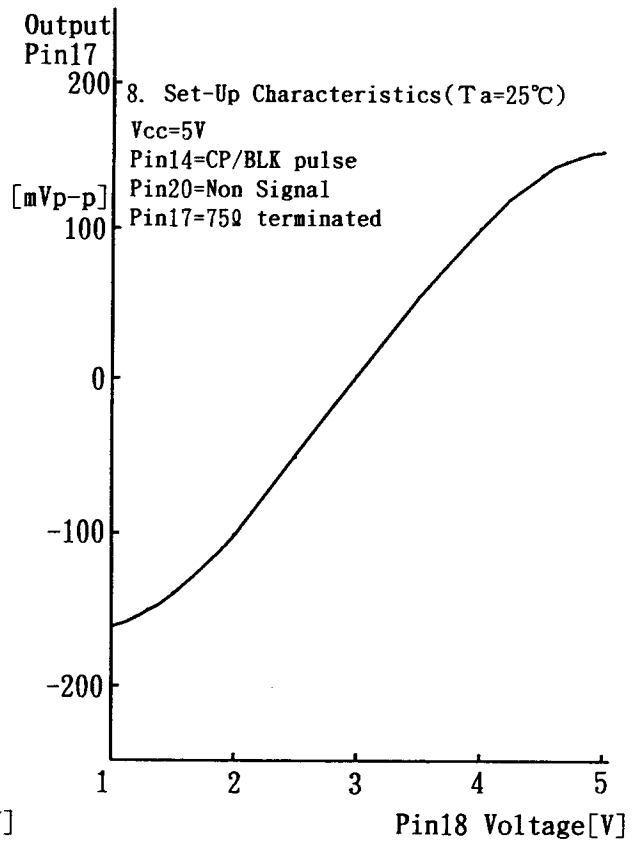
4. Main Signal
Gamma·Knee Characteristics (Ta=25℃)
Vcc=5V
Pin14=CP/BLK pulse



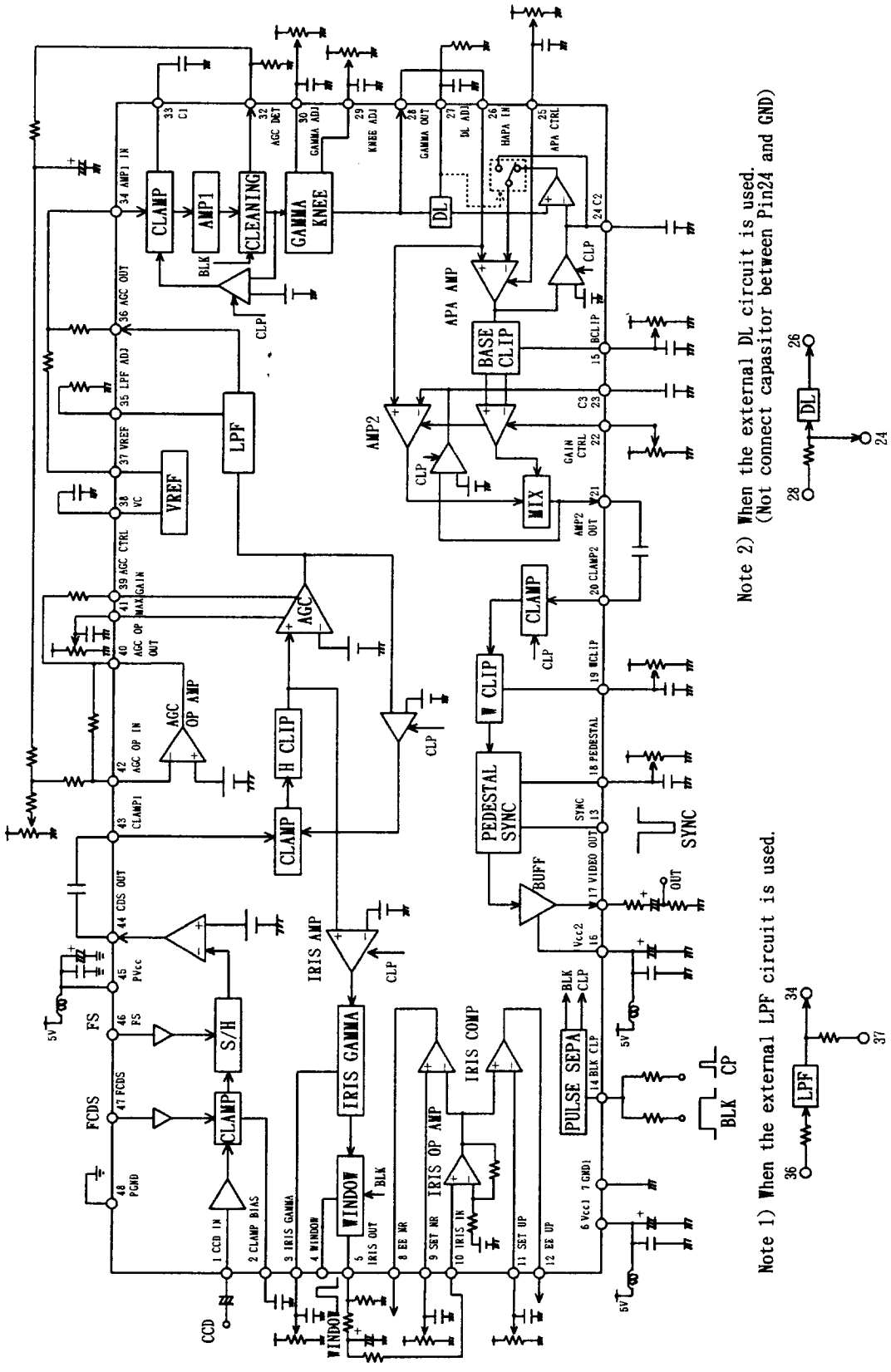

Gain
[dB]
5. Aperture Characteristics(Ta=25℃)
Vcc=5V, Pin22=0V
Pin14=CP/BLK pulse
Pin26=300mVp-p
Output Pin21
(Pin25=5V)
=0dB
0
-2
-4
-6
-8
-10
0
1
2
3
4
Pin25 Voltage[V]


Gain
[dB]
6. Base Clip Characteristics(Ta=25℃)
Vcc=5V
Pin22=0V, Pin25=5V
Pin14=CP/BLK pulse
Pin26=300mVp-p
Output Pin21(Pin15=5V)
=0dB
0
-2
-4
-6
-8
-10
1
1.5
2
2.5
Pin15 Voltage[V]


Output
Pin17
7. White Clip Characteristics(Ta=25℃)
Vcc=5V
Pin14=CP/BLK pulse
Pin20=2000mVp-p
Pin17=75Ω terminated
1000
[mVp-p]
800
600
400
0
1
2
3
4
Pin19 Voltage[V]


Output
Pin17
200
8. Set-Up Characteristics(Ta=25℃)
Vcc=5V
Pin14=CP/BLK pulse
Pin20=Non Signal
Pin17=75Ω terminated
[mVp-p]
100
0
-100
-200
1
2
3
4
5
Pin18 Voltage[V]

8 Application Circuit Example



9 Package and packing specification

1. Package Outline Specification

Refer to drawing No.AA873

2. Markings

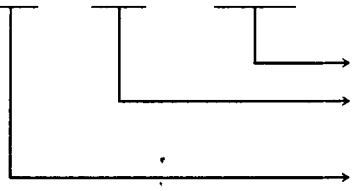
2－1. Marking contents

(1) Product name : IR3Y30M

(2) Company name : SHARP

(3) Date code

(Example) YY WW ××× Indicates the product was manufactured in the WWth week of 19YY.



Denotes the production ref.code (1~3)

Denotes the production week. (01,02,03,・・・・・52,53)

Denotes the production year. (Lower two digits of the year.)

(4) The marking of "JAPAN" indicates the country of origin.

2－2. Marking layout

Refer to drawing No.AA873

(This layout do not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3－1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (80devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (800devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

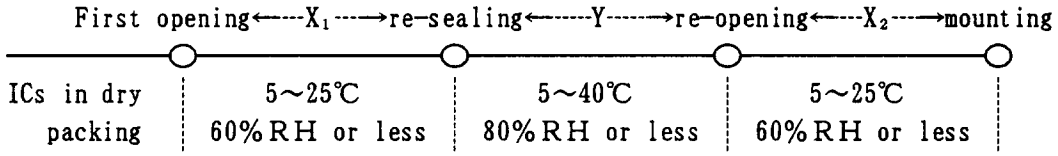
3－2. Outline dimension of tray
Refer to attached drawing

4. Storage and Opening of Dry Packing

4－1. Store under conditions shown below before opening the dry packing
(1) Temperature range : 5～40℃
(2) Humidity : 80% RH or less

4－2. Notes on opening the dry packing
(1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

4－3. Storage after opening the dry packing
Perform the following to prevent absorption of moisture after opening.
(1) After opening the dry packing, store the ICs in an environment with a temperature of 5～25℃ and a relative humidity of 60% or less and mount ICs within 4 days after opening dry packing.
(2) To re-store the ICs for an extended period of time within 4 days after opening the dry packing, use a dry box or re-seal the ICs in the dry packing with desiccant (whoes indicater is blue), and store in an environment with a temperature of 5～40℃ and a relative humidity of 80% or less, and mount ICs within 2 weeks.
(3) Total period of storage after first opening and re-opening is within 4 days, and store the ICs in the same environment as section 4-3.(1).



X_1+X_2 : within 4 days
Y : within 2 weeks

4－4. Baking (drying) before mounting
(1) Baking is necessary
(A) If the humidity indicator in the desiccant becomes pink
(B) If the procedure in section 4－3 could not be performed
(2) Recommended baking conditions
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16～24 hours at 120℃.
Heat resistance tray is used for shipping tray.
(3) Storage after baking
After baking ICs, store the ICs in the same environment as section 4-3.(1).

5. Surface Mount Conditions

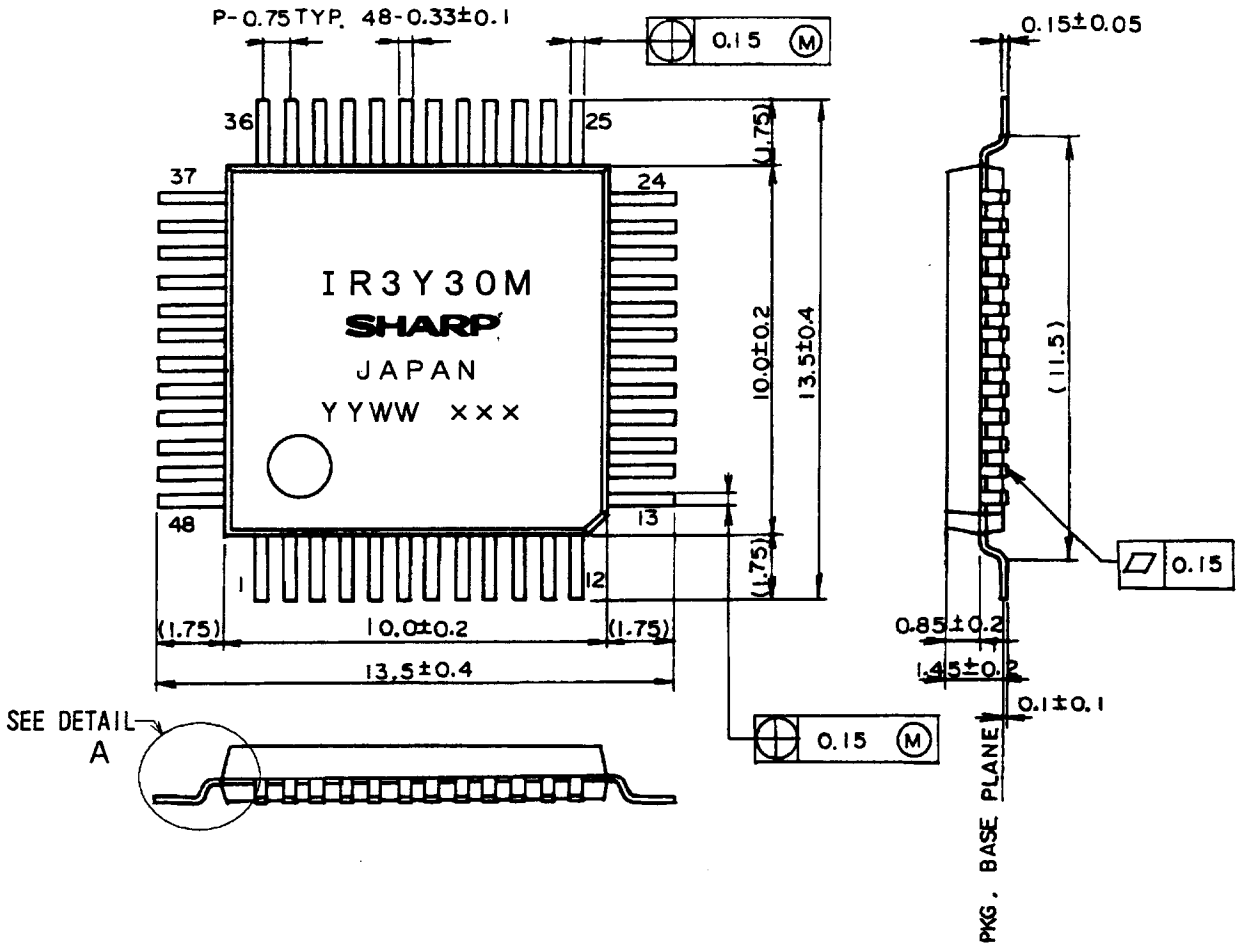
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

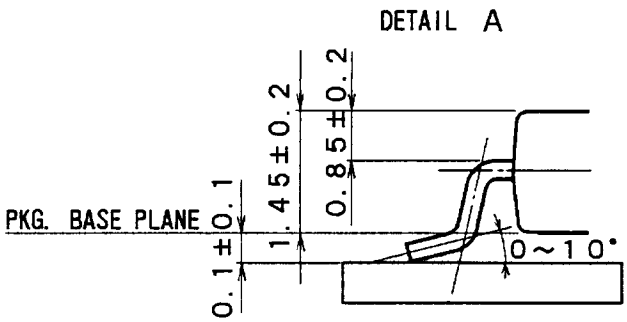
5－1.Soldering conditions(The following conditions are valid only for one time soldering.)

Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 240℃, duration less than 15 seconds above 230℃, temperature increase rate of 1～4℃/second	IC surface
Solder dipping	245℃ or less, duration less than 3 seconds/dip, total of 5 seconds	Solder bath
Vapor phase solderring	215℃ or less, duration less than 40 seconds above 200℃	Steam
Manual soldering (soldering iron)	260℃ or less, duration less than 10 seconds	IC outer lead surface

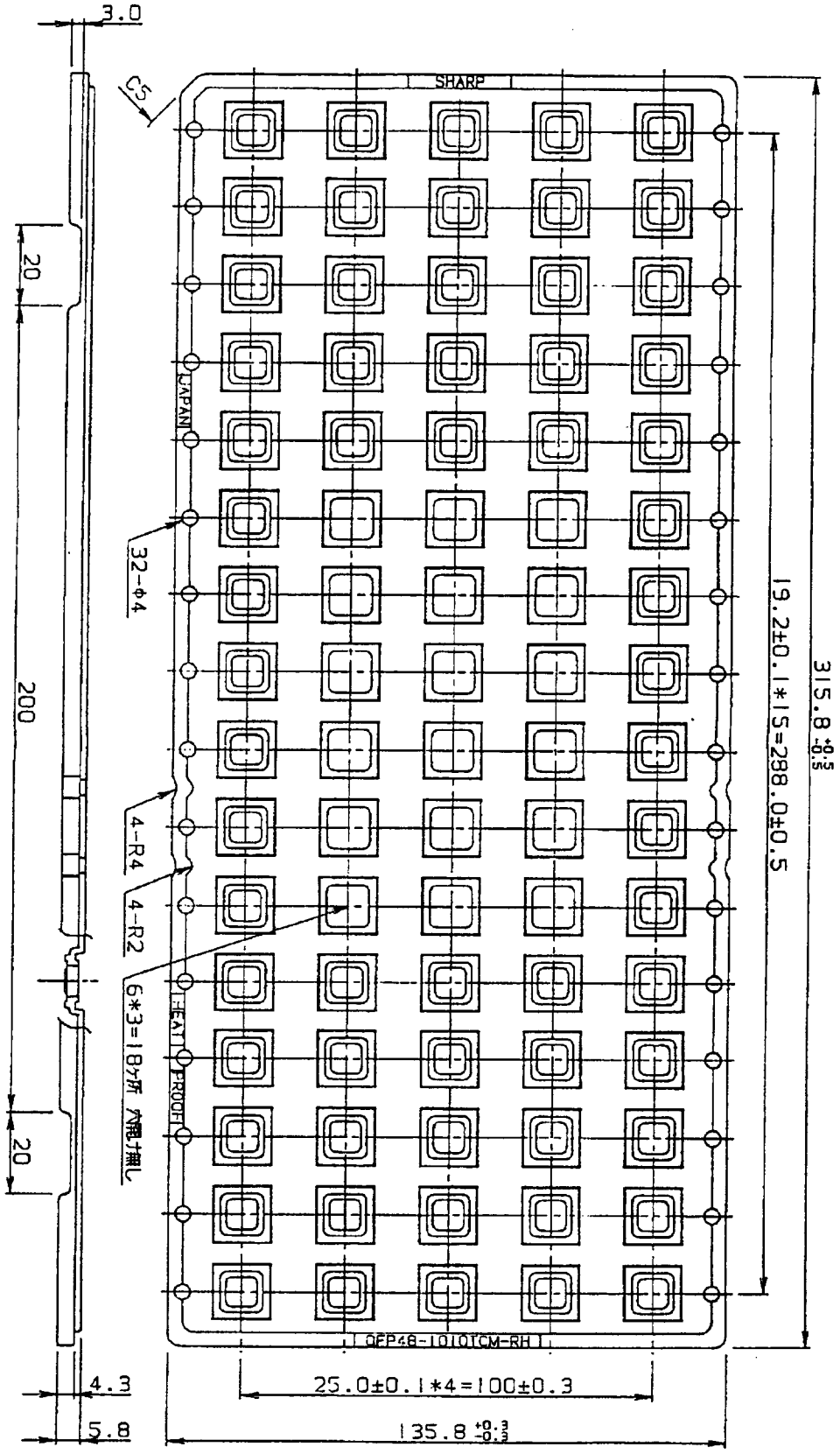
5－2. Conditions for removal of residual flux

(1) Ultrasonic washing power : 25 Watts/liter or less
(2) Washing time : Total 1 minute maximum
(3) Solvent temperature : 15～40℃





名称 NAME	QFP48-P-1010	リード仕上 LEAD FINISH	TIN-LEAD PLATING	備考 NOTE	プラスチックパッケージ外形寸法は、バリを含まないものとする。 Plastic body dimensions do not include burr of resin.
DRAWING NO.	AA873	単位 UNIT	mm		



名称 NAME	QFP48−1010TCM−RH			備考 NOTE
DRAWING NO.	CV741	単位 UNIT	mm	