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IMPROVED IP3 BEHAVIOUR OF THE 900MHz LOW NOISE AMPLIFIER WITH THE BFG425W

UPDATE OF REPORT RNR-T45-96-B-771

Abstract:
This application note contains an example of a Low Noise Amplifier with the new BFG425W Double Poly RF-transistor. The LNA is designed for a frequency f=900MHz, V_{SUP}~3.8V, I_{SUP}=10mA. *Measured* performance at f=900MHz: Noise Figure NF~1.7dB, gain S_{21} ~17dB and the *input* IP3=+3dBm.

Appendix I: 900MHz LNA circuit

Appendix II: Printlayout and list of used components & materials

Appendix III: Results of simulations and measurements

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Introduction:
With the new Philips silicon bipolar double poly BFG400W series, it is possible to design low noise amplifiers for high frequency applications with a low current and a low supply voltage. These amplifiers are well suited for the new generation low voltage high frequency wireless applications. In this note an example of such an amplifier will be given. This amplifier is designed for a working frequency of 900MHz.

Designing the circuit:
The circuit is designed to show the following performance:

transistor: BFG425W

V_{ce}=2V, I_c=10mA, V_{SUP}~3.5V
freq=900MHz
Gain~18dB
NF<=1.6dB
IP3>0dBm (input)
VSWRi<1:2
VSWRo<1:2

In the simulations the effect of extra RF-noise caused by the SMA-connectors was omitted, so in the practical situation the NF is ~0.1dB higher. This LNA is also optimised for the highest IP3. The IP3 can be optimised by:

I. an extra series C-decoupling of the base to the ground
II. increasing I_C

With the solution I. an extra component is necessary, and with solution II, the Noise Figure of the LNA increases and the optimum source impedance also.

The in- and output matching is realised with a LC-combination. Also extra emitter-inductance on both emitter-leads (µ-strips) are used to improve the matching and the Noise Figure.

Designing the layout:
A lay-out has been designed with HP-MDS. Appendix II contains the printlayout.

Measurements:
Simulations (with realistic RF-models of al used parts) and measurements of the total circuit (epoxy PCB) are done (Appendix III).

Appendix I: Schematic of the circuit

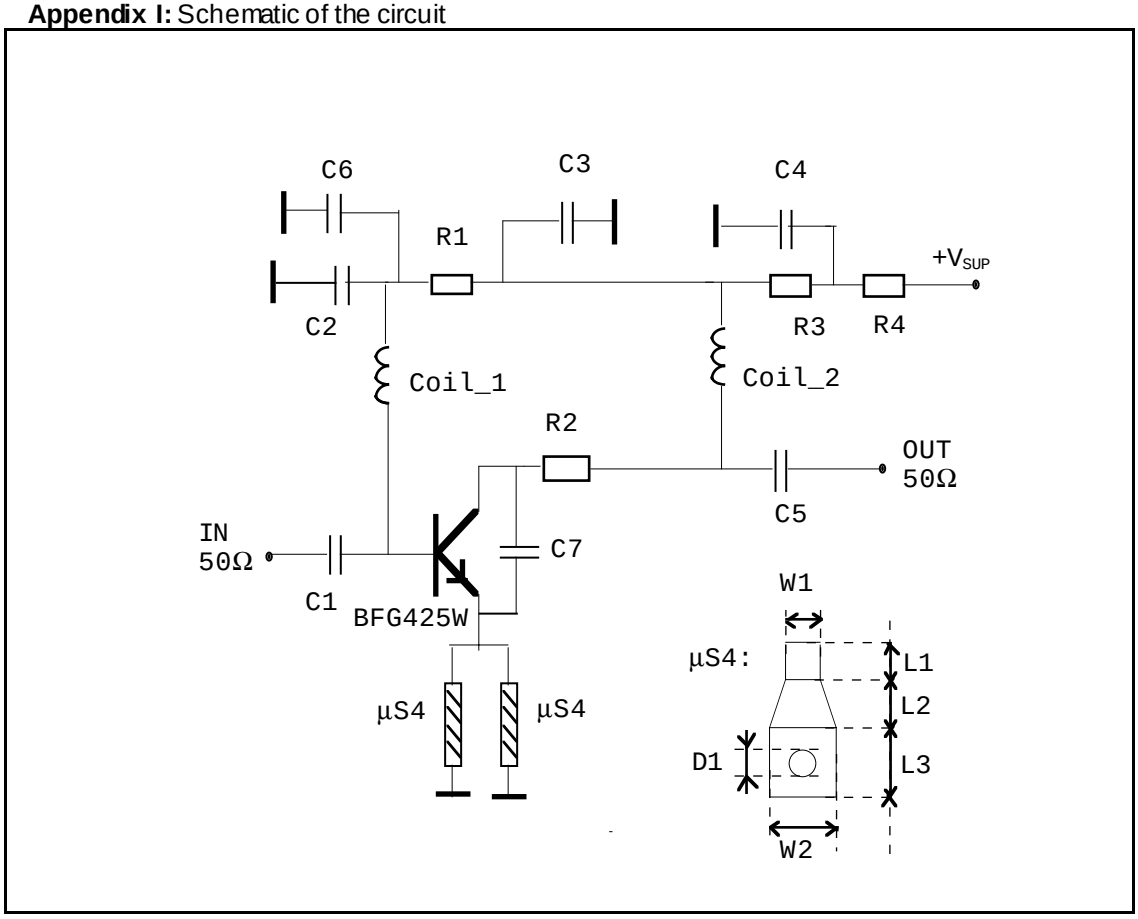

Figure 1: LNA circuit

900MHz LNA Component list: 900MHz LNA Component list:

Component	Value	Purpose, comment
R1	8.2 kΩ	Bias (coll.-base)
R2	10 Ω	in series with coll. for better S22, stability and reducing gain.
R3	22 Ω	RF blocking
R4	150 Ω	Bias, series with coll., cancelling hFE spread
C1	8.2 pF	Input match (input to base)
C2	27 pF	900 MHz short (L1 to ground)
C3	27 pF	900 MHz short (L2 to ground)
C4	100 nF	RF decoupling collector bias
C5	22 pF	Output match (collector to output)
C6	100 nF	To improve IP3 (by decoupling LF IP3 products)
C7	3.3 pF	Output match, stability (collector to emitter)
Coil_1	22 nH	Input match (base-bias)
Coil_2	12 nH	Output match (collector-bias)
µs4	(see next table)	µ-stripline Emitter-induction

µS4 Emitter inductance of µ-stripline and via-hole (see on former page: Schematic of the circuit):

Name	Dimension	Description
L1	2.5mm	length µ-stripline; Z_0~48Ω (PCB: ε_r ~4.6, H=0.5mm)
L2	1.0mm	length interconnect stripline and via-hole area
L3	1.0mm	length via-hole area
W1	0.5mm	width µ-stripline
W2	1.0mm	width via-hole area
D1	0.4mm	diameter of via-hole

Appendix II: Printlayout and list of used components & materials

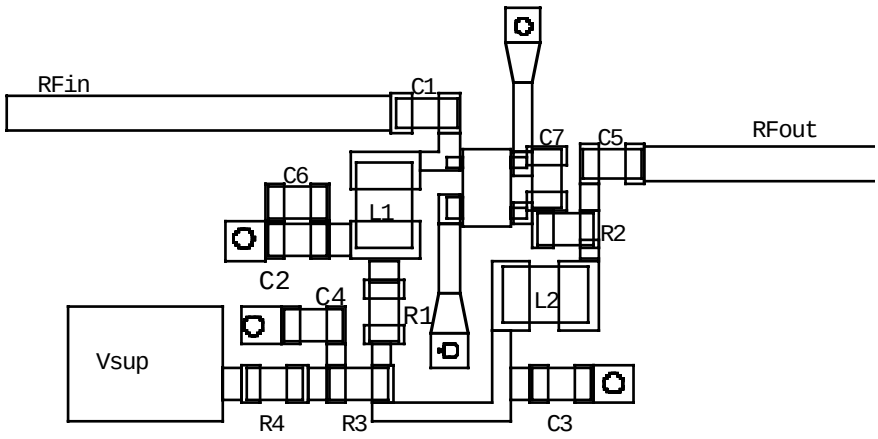

Figure 2: Printlayout

900MHz LNA Component list:

Component:	Value:	size:
PCB	FR4: ε_r ~4.6	H=0.5mm
R1	8.2 kΩ	0603 Philips
R2	10 Ω	0603 Philips
R3	22 Ω	0603 Philips
R4	150 Ω	0603 Philips
C1	8.2 pF	0603 Philips
C2	27 pF	0603 Philips
C3	27 pF	0603 Philips
C4	100 nF	0805 Philips
C5	22 pF	0603 Philips
C6	100 nF	0805 Philips
C7	3.3 pF	0603 Philips
L1	22 nH	0805CS Coilcraft
L2	12 nH	0805CS Coilcraft

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Appendix III: Results of simulations and measurements

Conditions: V_{SUP}=3.7V, I_C=10mA, f=900MHz

	Simulation (HP-MDS):	Measurements PCB:	Comment:
$\|S21\|^2$ [dB]	17.2	17.3	
$\|S12\|^2$ [dB]	-28.0	-28.3	
VSWRi	2.2	2.5	
VSWRo	1.7	1.8	
Noise Figure [dB]	1.6	1.7	note 1
IP3 [dBm] **(input)**	+1.3	+3	Δf=200KHz, note 2

note 1: The Noise Figure of the PCB is higher than the simulations (~0.1 dB). This is caused by the influence of the SMA-connectors and the microstrips on the epoxy PCB.
note 2: The IP3 of the PCB is higher than the simulations. This can be explained by the deviation of the Spice parameters, used in the IP3 simulations, from the sample transistor-parameters used in the LNA.

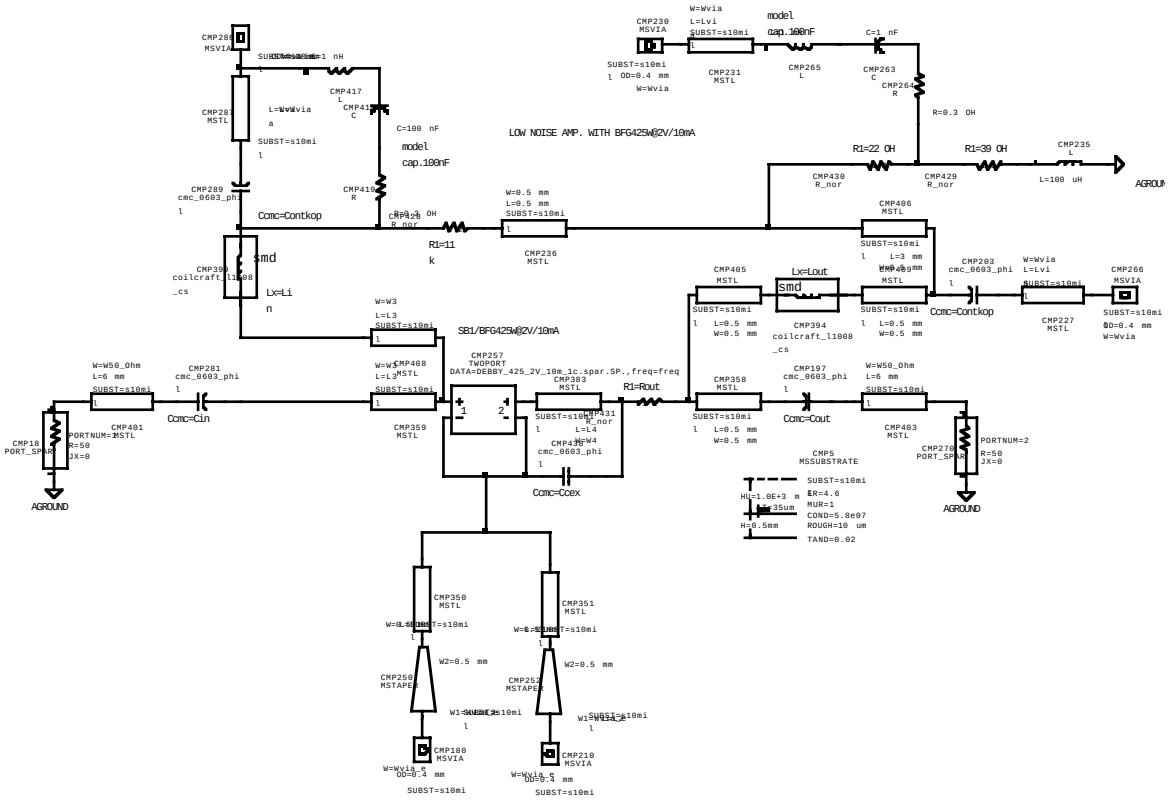

Figure 3: HP-MDS simulation circuit