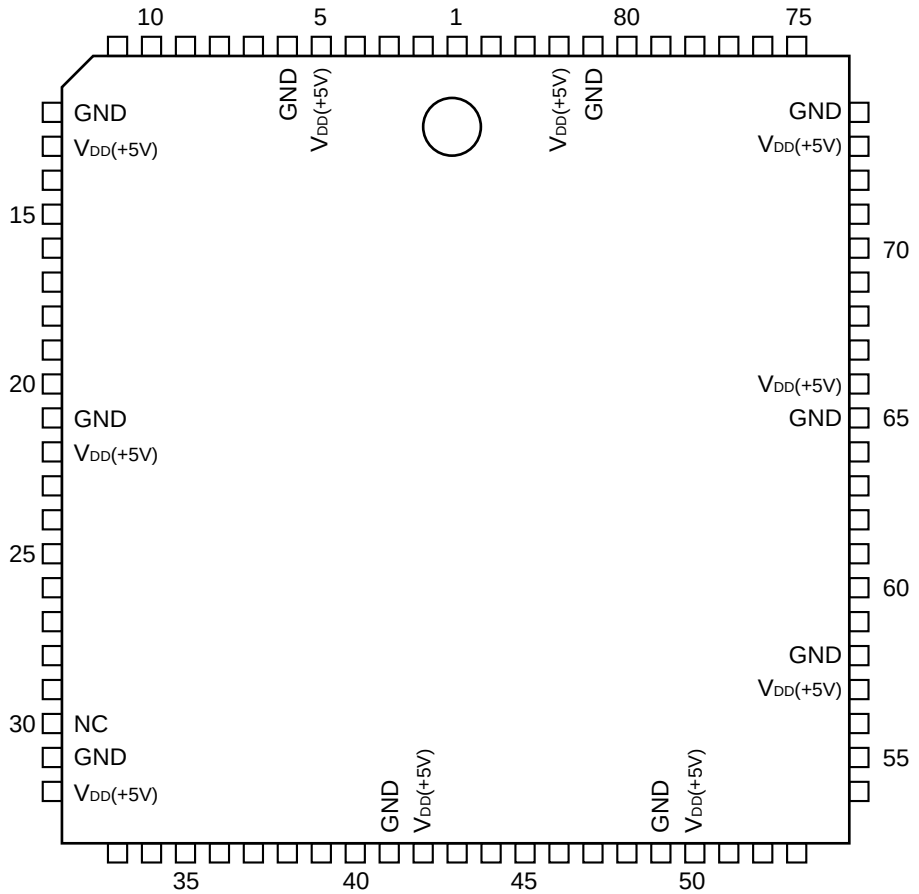
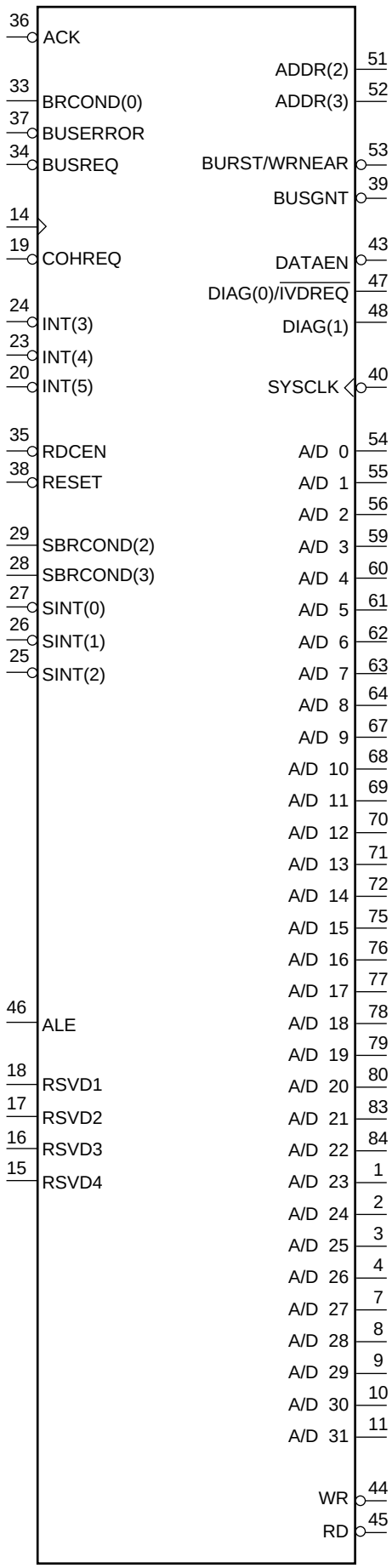
C-MOS RISC CPU

—TOP VIEW—



(VDD = +5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	A/D (23)	22	—	V_{DD}	43	O	$\overline{\text{DATAEN}}$	64	I/O	A/D (8)
2	I/O	A/D (24)	23	I	$\overline{\text{INT (4)}}$	44	I/O	$\overline{\text{WR}}$	65	—	GND
3	I/O	A/D (25)	24	I	$\overline{\text{INT (3)}}$	45	O	$\overline{\text{RD}}$	66	—	V_{DD}
4	I/O	A/D (26)	25	I	$\overline{\text{SINT (2)}}$	46	I/O	ALE	67	I/O	A/D (9)
5	—	V_{DD}	26	I	$\overline{\text{SINT (1)}}$	47	I/O	DIAG(0) / $\overline{\text{IVDREQ}}$	68	I/O	A/D (10)
6	—	GND	27	I	$\overline{\text{SINT (0)}}$	48	O	DIAG (1)	69	I/O	A/D (11)
7	I/O	A/D (27)	28	I	SBR COND (3)	49	—	GND	70	I/O	A/D (12)
8	I/O	A/D (28)	29	I	SBR COND (2)	50	—	V_{DD}	71	I/O	A/D (13)
9	I/O	A/D (29)	30	—	NC	51	O	ADDR (2)	72	I/O	A/D (14)
10	I/O	A/D (30)	31	—	GND	52	O	ADDR (3)	73	—	V_{DD}
11	I/O	A/D (31)	32	—	V_{DD}	53	O	$\overline{\text{BURST}}$ / $\overline{\text{WRNEAR}}$	74	—	GND
12	—	GND	33	I	BR COND (0)	54	I/O	A/D (0)	75	I/O	A/D (15)
13	—	V_{DD}	34	I	$\overline{\text{BUSREQ}}$	55	I/O	A/D (1)	76	I/O	A/D (16)
14	I	CLK	35	I	$\overline{\text{RDCEN}}$	56	I/O	A/D (2)	77	I/O	A/D (17)
15	I/O	RSVD (4)	36	I	$\overline{\text{ACK}}$	57	—	V_{DD}	78	I/O	A/D (18)
16	I/O	RSVD (3)	37	I	$\overline{\text{BUSERROR}}$	58	—	GND	79	I/O	A/D (19)
17	I/O	RSVD (2)	38	I	$\overline{\text{RESET}}$	59	I/O	A/D (3)	80	I/O	A/D (20)
18	I/O	RSVD (1)	39	O	$\overline{\text{BUSGNT}}$	60	I/O	A/D (4)	81	—	GND
19	I	$\overline{\text{COHREQ}}$	40	O	$\overline{\text{SYSCLK}}$	61	I/O	A/D (5)	82	—	V_{DD}
20	I	$\overline{\text{INT (5)}}$	41	—	GND	62	I/O	A/D (6)	83	I/O	A/D (21)
21	—	GND	42	—	V_{DD}	63	I/O	A/D (7)	84	I/O	A/D (22)



INPUT

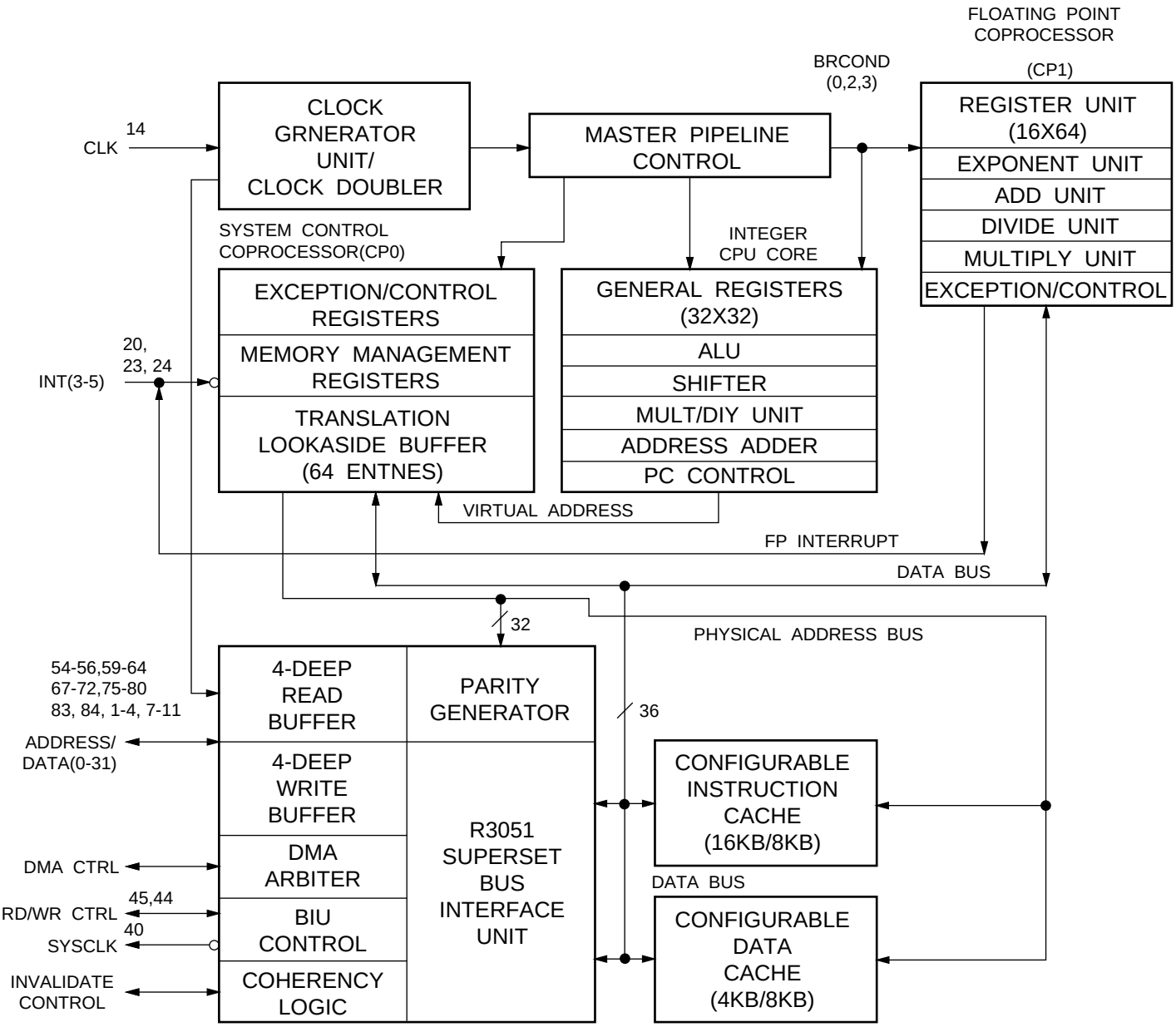
$\overline{ACK}$	;	ACKNOWLEDGE
BRCOND(0)	;	BRANCH CONDITION PORT (0)
$\overline{BUSERROR}$	;	BUS ERROR
$\overline{BUSREQ}$	;	DMA ARBITER BUS REQUEST
CLK	;	MASTER CLOCK
$\overline{COHREQ}$	;	COHERENT DMA REQUEST
$\overline{INT}$(3-5)	;	PROCESSOR INTERRUPT (3-5)
$\overline{IVDREQ}$	;	INVALIDATE REQUEST
$\overline{RDCEN}$	;	READ BUFFER CLOCK ENABLE
$\overline{RESET}$	;	MASTER PROCESSOR RESET
SBRCOND(2, 3)	;	BRANCH CONDITION PORT (2, 3)
$\overline{SINT}$(0-2)	;	PROCESSOR INTERRUPT (0-2)

OUTPUT

ADDR(2, 3)	;	LOW ADDRESS (2, 3)
$\overline{BURST}$ / WRNEAR	;	BURST TRANSFER WRITE NEAR
$\overline{BUSGNT}$	;	DMA ARBITER BUS GRANT
DATAEN	;	EXTERNAL DATA ENABLE
DIAG(0, 1)	;	DIAGNOSTIC (0, 1)
$\overline{RD}$	;	READ
SYSCLK	;	SYSTEM REFERENCE CLOCK

INPUT/OUTPUT

A/D(0-31)	;	ADRESS DATA (0-31)
ALE	;	ADDRESS LATCH ENABLE
RSVD(1-4)	;	RESERVED (1-4)
$\overline{WR}$	;	WRITE


FLOATING POINT
COPROCESSOR
(CP1)
BRCOND
(0,2,3)
14
CLK
CLOCK
GRNERATOR
UNIT/
CLOCK DOUBLER
MASTER PIPELINE
CONTROL
REGISTER UNIT
(16X64)
EXPONENT UNIT
ADD UNIT
DIVIDE UNIT
MULTIPLY UNIT
EXCEPTION/CONTROL
SYSTEM CONTROL
COPROCESSOR(CP0)
INTEGER
CPU CORE
EXCEPTION/CONTROL
REGISTERS
MEMORY MANAGEMENT
REGISTERS
TRANSLATION
LOOKASIDE BUFFER
(64 ENTNES)
GENERAL REGISTERS
(32X32)
ALU
SHIFTER
MULT/DIY UNIT
ADDRESS ADDER
PC CONTROL
20,
23, 24
INT(3-5)
VIRTUAL ADDRESS
FP INTERRUPT
DATA BUS
32
PHYSICAL ADDRESS BUS
54-56,59-64
67-72,75-80
83, 84, 1-4, 7-11
4-DEEP
READ
BUFFER
PARITY
GENERATOR
36
ADDRESS/
DATA(0-31)
4-DEEP
WRITE
BUFFER
CONFIGURABLE
INSTRUCTION
CACHE
(16KB/8KB)
DMA CTRL
DMA
ARBITER
DATA BUS
45,44
RD/WR CTRL
40
SYSCLK
BIU
CONTROL
R3051
SUPERSET
BUS
INTERFACE
UNIT
CONFIGURABLE
DATA
CACHE
(4KB/8KB)
INVALIDATE
CONTROL
COHERENCY
LOGIC