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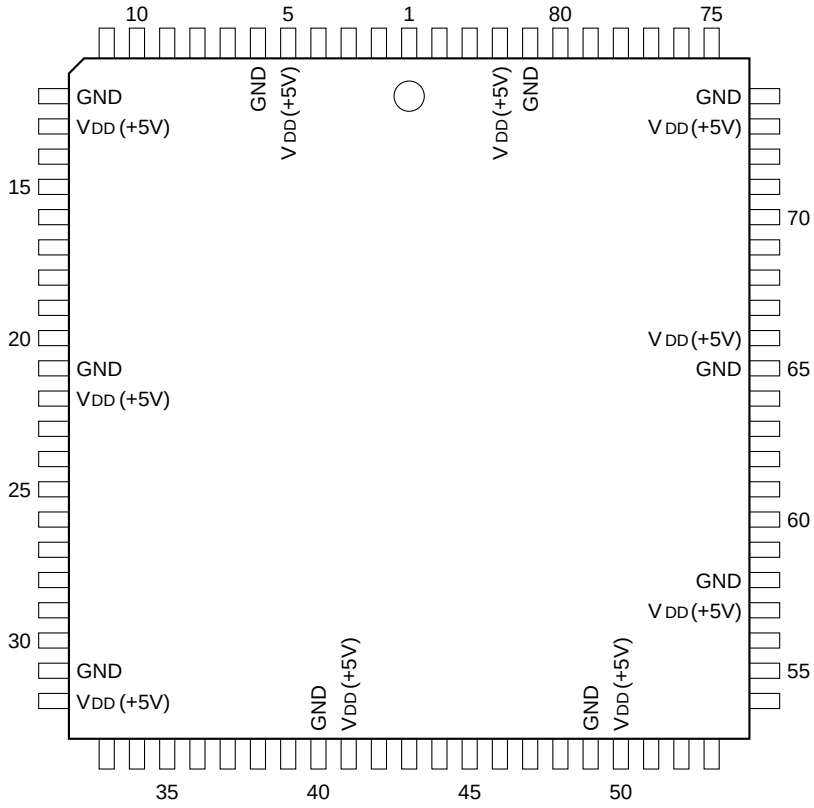
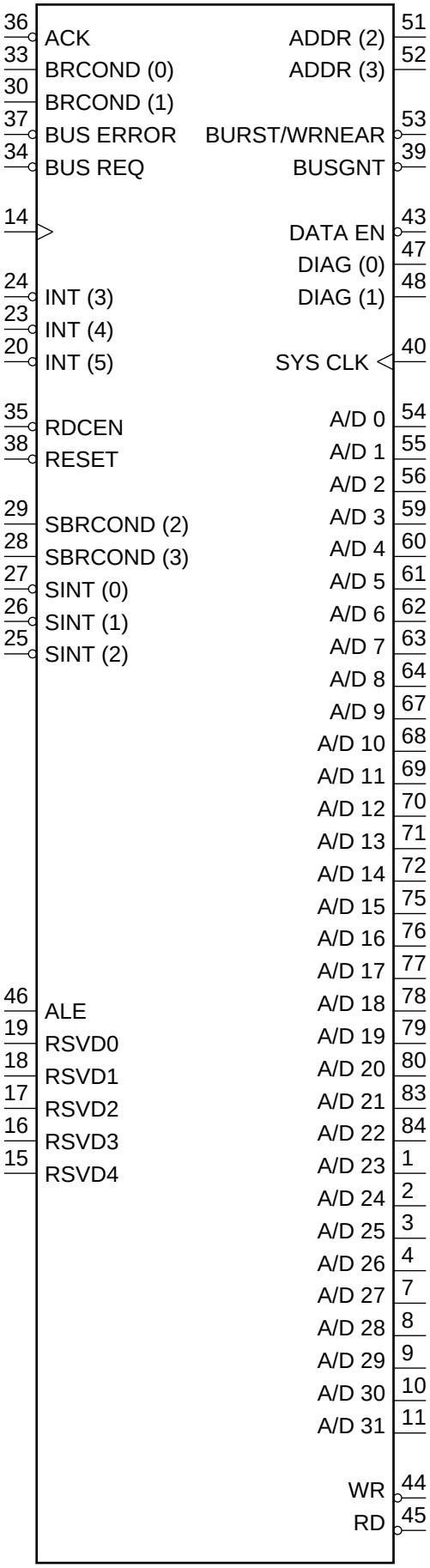
C-MOS RISC CPU

- TOP VIEW -



(V_{DD} =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	A/D (23)	22	–	V_{DD}	43	O	$\overline{DATAEN}$	64	I/O	A/D (8)
2	I/O	A/D (24)	23	I	$\overline{INT (4)}$	44	O	$\overline{WR}$	65	–	GND
3	I/O	A/D (25)	24	I	$\overline{INT (3)}$	45	O	$\overline{RD}$	66	–	V_{DD}
4	I/O	A/D (26)	25	I	$\overline{SINT (2)}$	46	O	ALE	67	I/O	A/D (9)
5	–	V_{DD}	26	I	$\overline{SINT (1)}$	47	O	DIAG (0)	68	I/O	A/D (10)
6	–	GND	27	I	$\overline{SINT (0)}$	48	O	DIAG (1)	69	I/O	A/D (11)
7	I/O	A/D (27)	28	I	SBR COND (3)	49	–	GND	70	I/O	A/D (12)
8	I/O	A/D (28)	29	I	SBR COND (2)	50	–	V_{DD}	71	I/O	A/D (13)
9	I/O	A/D (29)	30	O	BR COND (1)	51	O	ADDR (2)	72	I/O	A/D (14)
10	I/O	A/D (30)	31	–	GND	52	O	ADDR (3)	73	–	V_{DD}
11	I/O	A/D (31)	32	–	V_{DD}	53	O	$\overline{BURST/WRNEAR}$	74	–	GND
12	–	GND	33	I	BR COND (0)	54	I/O	A/D (0)	75	I/O	A/D (15)
13	–	V_{DD}	34	I	$\overline{BUSREQ}$	55	I/O	A/D (1)	76	I/O	A/D (16)
14	I	CLK 2X	35	I	$\overline{RDCEN}$	56	I/O	A/D (2)	77	I/O	A/D (17)
15	I/O	RSVD (4)	36	I	$\overline{ACK}$	57	–	V_{DD}	78	I/O	A/D (18)
16	I/O	RSVD (3)	37	I	$\overline{BUSERROR}$	58	–	GND	79	I/O	A/D (19)
17	I/O	RSVD (2)	38	I	$\overline{RESET}$	59	I/O	A/D (3)	80	I/O	A/D (20)
18	I/O	RSVD (1)	39	O	$\overline{BUSGNT}$	60	I/O	A/D (4)	81	–	GND
19	I	RSVD (0)	40	O	$\overline{SYSCLK}$	61	I/O	A/D (5)	82	–	V_{DD}
20	I	$\overline{INT (5)}$	41	–	GND	62	I/O	A/D (6)	83	I/O	A/D (21)
21	–	GND	42	–	V_{DD}	63	I/O	A/D (7)	84	I/O	A/D (22)



INPUT

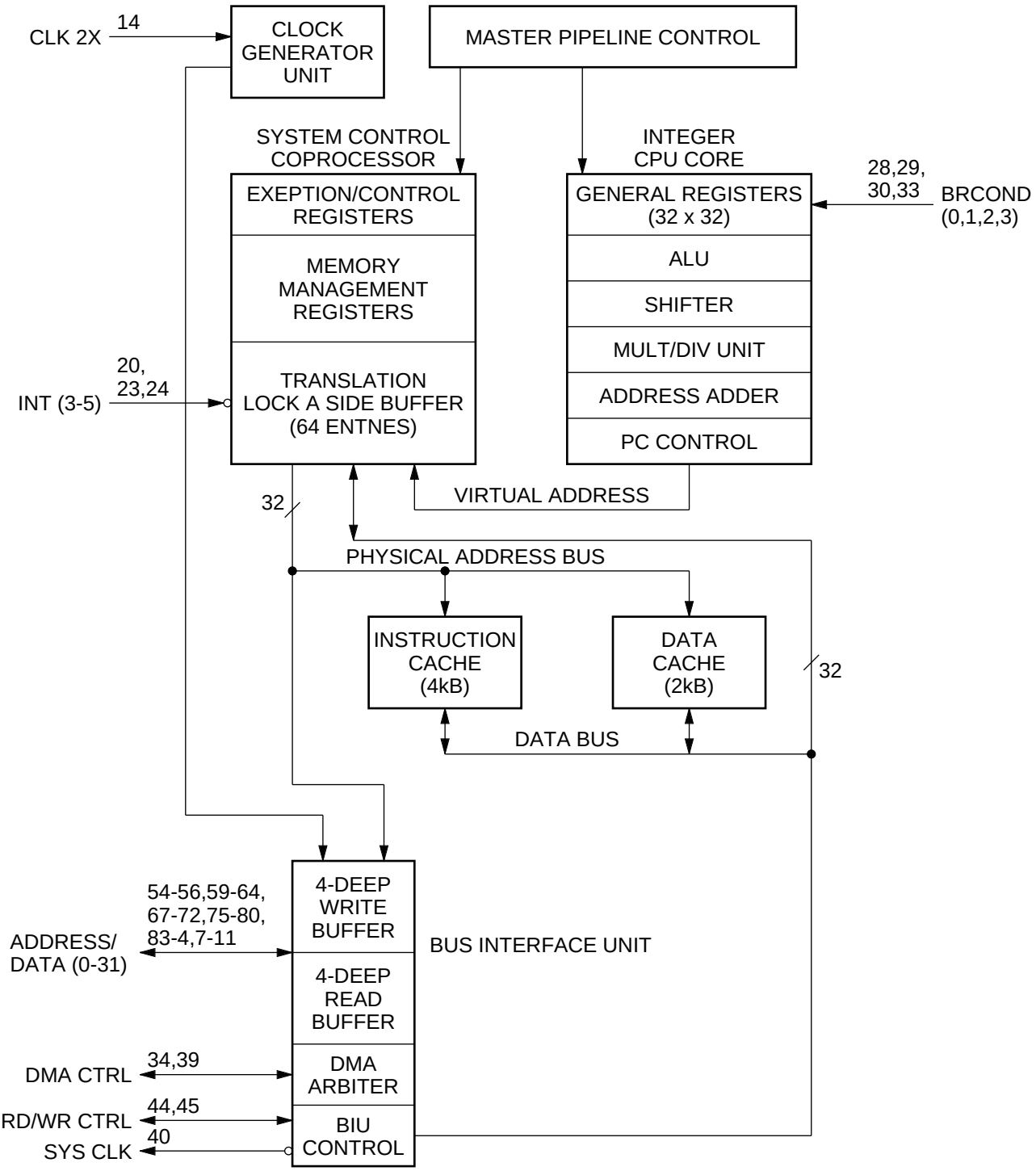
$\overline{\text{ACK}}$	; ACKNOWLEDGE
BRCOND (0,1)	; BRANCH CONDITION PORT (0,1)
$\overline{\text{BUSERROR}}$	; BUS ERROR
$\overline{\text{BUSREQ}}$	; DMA ARBITER BUS REQUEST
CLK 2X	; MASTER CLOCK
$\overline{\text{COHREQ}}$	; COHERENT DMA REQUEST
$\overline{\text{INT}}$ (3-5)	; PROCESSOR INTERRUPT (3-5)
$\overline{\text{IVDREQ}}$	; INVALIDATE REQUEST
$\overline{\text{RDCEN}}$	; READ BUFFER CLOCK ENABLE
$\overline{\text{RESET}}$	; MASTER PROCESSOR RESET
SBRCOND (2,3)	; BRANCH CONDITION PORT (2,3)
$\overline{\text{SINT}}$ (0-2)	; PROCESSOR INTERRUPT (0-2)

OUTPUT

ADDR (2,3)	; LOW ADDRESS (2,3)
$\overline{\text{BURST/WRNEAR}}$	; BURST TRANSFER WRITE NEAR
$\overline{\text{BUSGNT}}$	; DMA ARBITER BUS GRANT
$\overline{\text{DATA EN}}$	; EXTERNAL DATA ENABLE
DIAG (0,1)	; DIAGNOSTIC (0,1)
$\overline{\text{RD}}$	; READ
$\overline{\text{SYSCLK}}$	; SYSTEM REFERENCE CLOCK
$\overline{\text{WR}}$	; WRITE

INPUT/OUTPUT

A/D (0-31)	; ADDRESS DATA (0-31)
ALE	; ADDRESS LATCH ENABLE
RSVD (1-4)	; RESERVED (1-4)


CLK 2X
14
CLOCK GENERATOR UNIT
MASTER PIPELINE CONTROL
SYSTEM CONTROL COPROCESSOR
INTEGER CPU CORE
EXEPTION/CONTROL REGISTERS
MEMORY MANAGEMENT REGISTERS
TRANSLATION LOCK A SIDE BUFFER (64 ENTNES)
GENERAL REGISTERS (32 x 32)
ALU
SHIFTER
MULT/DIV UNIT
ADDRESS ADDER
PC CONTROL
28,29, 30,33
BRCOND (0,1,2,3)
INT (3-5)
20, 23,24
32
VIRTUAL ADDRESS
PHYSICAL ADDRESS BUS
INSTRUCTION CACHE (4kB)
DATA CACHE (2kB)
32
DATA BUS
4-DEEP WRITE BUFFER
4-DEEP READ BUFFER
DMA ARBITER
BIU CONTROL
BUS INTERFACE UNIT
ADDRESS/ DATA (0-31)
54-56,59-64, 67-72,75-80, 83-4,7-11
DMA CTRL
34,39
RD/WR CTRL
44,45
SYS CLK
40