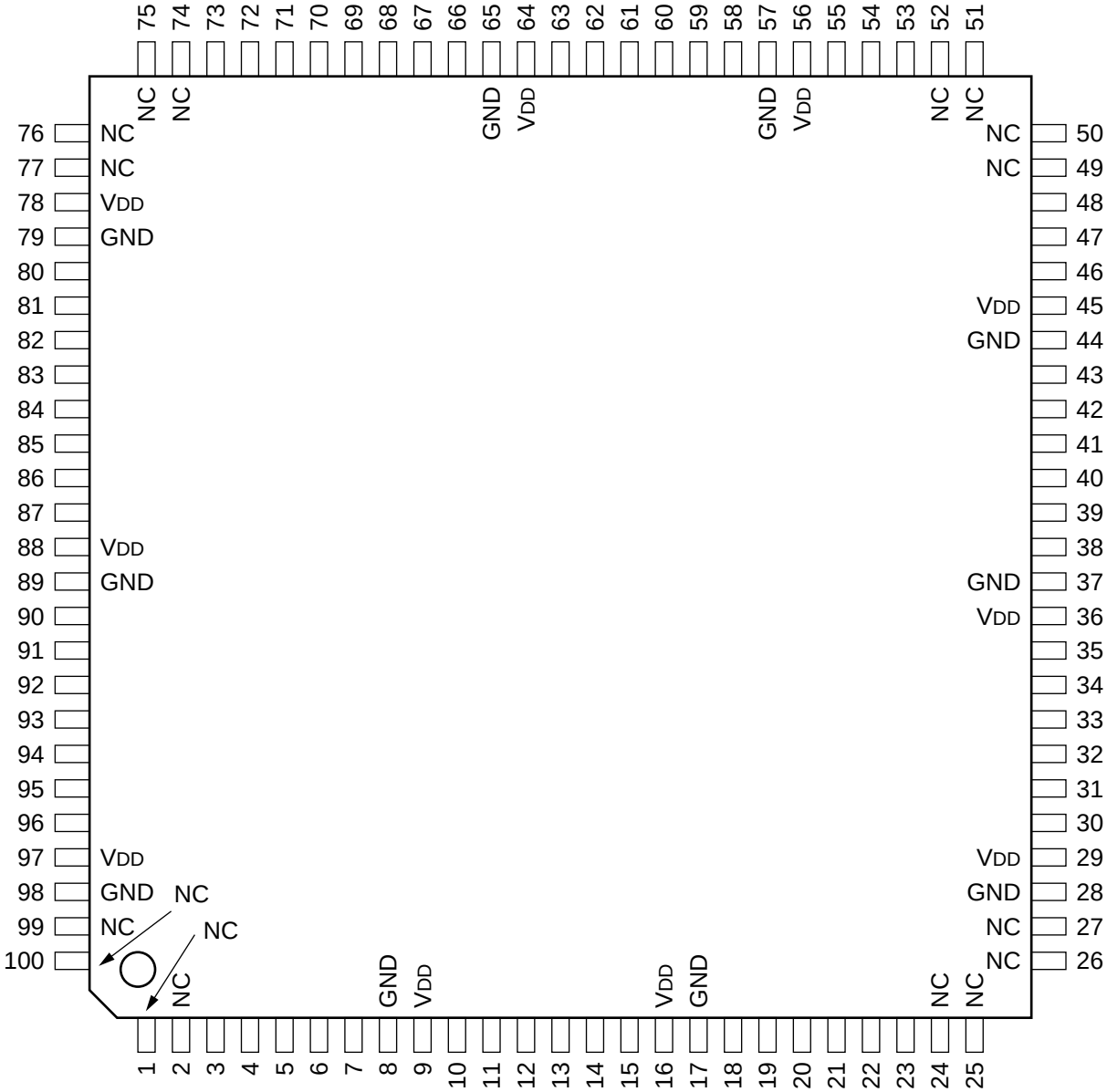
C-MOS RISC CPU

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	26	—	NC	51	—	NC	76	—	NC
2	—	NC	27	—	NC	52	—	NC	77	—	NC
3	I/O	A/D (31)	28	—	GND	53	O	$\overline{\text{BURST/WRNEAR}}$	78	—	V_{CC}
4	I/O	A/D (30)	29	—	V_{DD}	54	O	ADDR (3)	79	—	GND
5	I/O	A/D (29)	30	I/O	A/D (14)	55	O	ADDR (2)	80	O	$\overline{\text{TC}}$
6	I/O	A/D (28)	31	I/O	A/D (13)	56	—	V_{DD}	81	I/O	∗2/$\overline{\text{EXTDATAEN}}$
7	I/O	A/D (27)	32	I/O	A/D (12)	57	—	GND	82	I/O	∗1/$\overline{\text{IOSTROBE}}$
8	—	GND	33	I/O	A/D (11)	58	O	DIAG	83	I	$\overline{\text{SINT (0)}}$
9	—	V_{DD}	34	I/O	A/D (10)	59	O	$\overline{\text{LAST}}$	84	I	$\overline{\text{SINT (1)}}$
10	I/O	A/D (26)	35	I/O	A/D (9)	60	O	ALE	85	I	$\overline{\text{SINT (2)}}$
11	I/O	A/D (25)	36	—	V_{DD}	61	O	$\overline{\text{RD}}$	86	I	$\overline{\text{INT (3)}}$
12	I/O	A/D (24)	37	—	GND	62	O	$\overline{\text{WR}}$	87	I	$\overline{\text{INT (4)}}$
13	I/O	A/D (23)	38	I/O	A/D (8)	63	O	$\overline{\text{DATAEN}}$	88	—	V_{DD}
14	I/O	A/D (22)	39	I/O	A/D (7)	64	—	V_{DD}	89	—	GND
15	I/O	A/D (21)	40	I/O	A/D (6)	65	—	GND	90	I	$\overline{\text{INT (5)}}$
16	—	V_{DD}	41	I/O	A/D (5)	66	O	$\overline{\text{SYSCLK}}$	91	O	ADDR (0)
17	—	GND	42	I/O	A/D (4)	67	O	$\overline{\text{BUSGNT}}$	92	O	ADDR (1)
18	I/O	A/D (20)	43	I/O	A/D (3)	68	I	$\overline{\text{RESET}}$	93	O	$\overline{\text{BE16 (0)}}$
19	I/O	A/D (19)	44	—	GND	69	I	$\overline{\text{BUSERROR}}$	94	O	$\overline{\text{BE16 (1)}}$
20	I/O	A/D (18)	45	—	V_{DD}	70	I	$\overline{\text{ACK}}$	95	I	$\overline{\text{TRISTATE}}$
21	I/O	A/D (17)	46	I/O	A/D (2)	71	I	$\overline{\text{RDCEN}}$	96	I	CLK IN
22	I/O	A/D (16)	47	I/O	A/D (1)	72	I	$\overline{\text{BUSREQ}}$	97	—	V_{DD}
23	I/O	A/D (15)	48	I/O	A/D (0)	73	O	$\overline{\text{MEMSTROBE}}$	98	—	GND
24	—	NC	49	—	NC	74	—	NC	99	—	NC
25	—	NC	50	—	NC	75	—	NC	100	—	NC

∗1 : SBRCOND (3)　　∗2 : SBRCOND (2)

INPUT

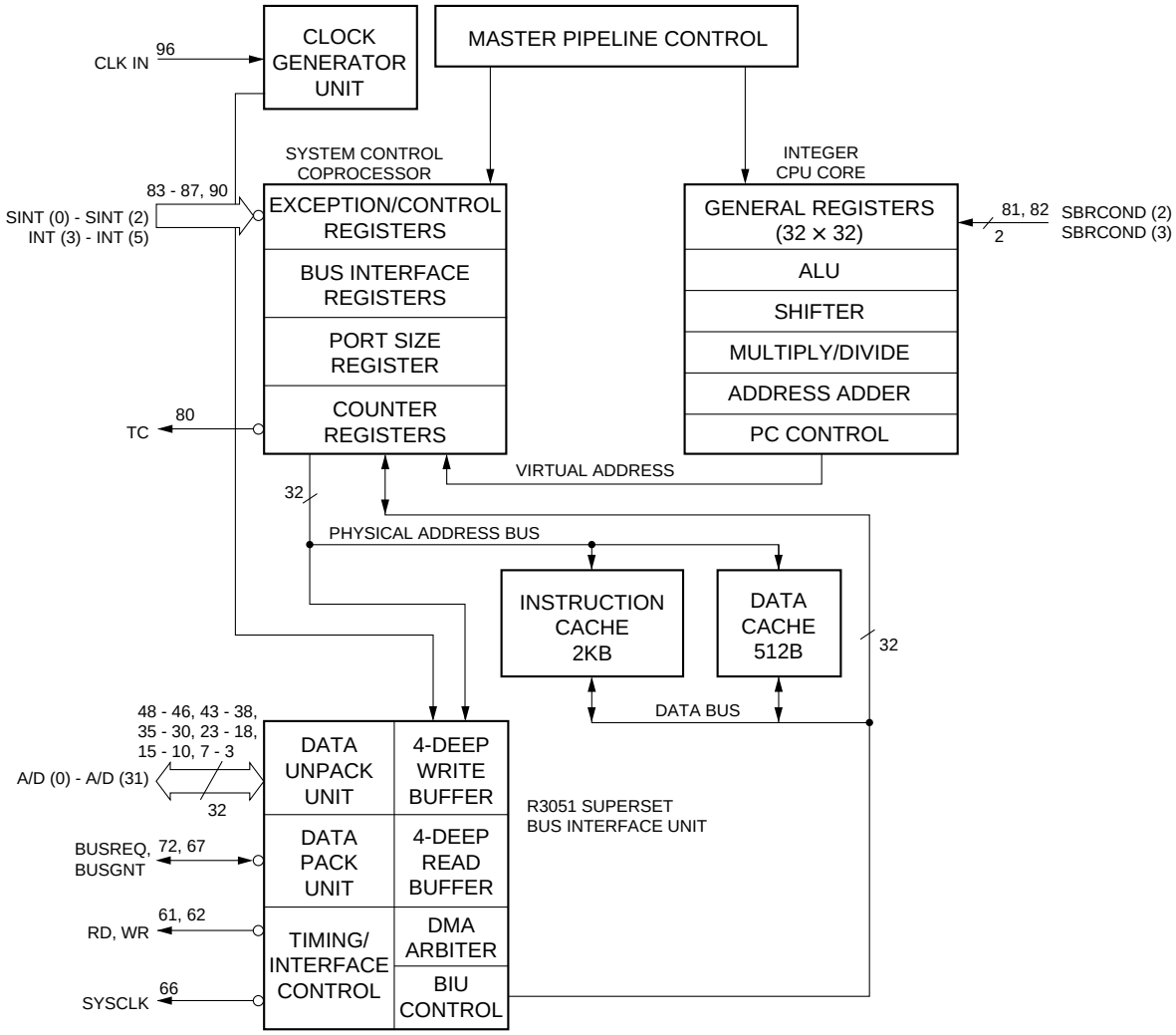
$\overline{ACK}$	:	ACKNOWLEDGE
$\overline{BUSERROR}$	:	BUS ERROR
$\overline{BUSREQ}$	:	DMA ARBITER BUS REQUEST
CLK IN	:	MASTER CLOCK
$\overline{INT}$ (3) - $\overline{INT}$ (5)	:	PROCESSOR INTERRUPT 3 - 5
$\overline{RDCEN}$	:	READ BUFFER CLOCK ENABLE
$\overline{RESET}$	:	MASTER PROCESSOR RESET
SBRCOND (2), SBRCOND (3)	:	BRANCH CONDITION PORT
$\overline{SINT}$ (0) - $\overline{SINT}$ (2)	:	PROCESSOR INTERRUPT 0 - 2
$\overline{TRISTATE}$	:	TRI-STATE

OUTPUT

ADDR (0) - ADDR (3)	:	LOW ADDRESS 0 - 3
A/D (0) - A/D (3)	:	BYTE ENABLE STROBES 0 - 3 FOR 32-BIT BUS/DATA 0 - 3
A/D (4) - A/D (31)	:	HIGH-ORDER ADDRESS 4 - 31/DATA 4 - 31
ALE	:	ADDRESS LATCH ENABLE
$\overline{BE16}$ (0), $\overline{BE16}$ (1)	:	BYTE ENABLE STROBES FOR 16-BIT MEMORY PORT 0, 1
$\overline{BURST}$	:	BURST TRANSFER
$\overline{BUSGNT}$	:	DMA ARBITER BUS GRANT
$\overline{DATAEN}$	:	DATA ENABLE
DIAG	:	DIAGNOSTIC
$\overline{EXT\ DATA\ EN}$	:	EXTENDED DATA ENABLE
$\overline{IO\ STROBE}$	:	IO STROBE
$\overline{LAST}$	:	LAST DATUM IN MINI BURST
$\overline{MEMSTROBE}$	:	MEMORY STROBE
$\overline{RD}$	:	READ
$\overline{SYSCLK}$	:	SYSTEM REFERENCE CLOCK
$\overline{TC}$	:	TERMINAL COUNT
$\overline{WR}$	:	WRITE
$\overline{WRNEAR}$	:	WRITE NEAR

INPUT/OUTPUT

A/D (0) - A/D (31)	:	ADDRESS LATCH ENABLE


CLOCK GENERATOR UNIT
MASTER PIPELINE CONTROL
CLK IN
96
SYSTEM CONTROL COPROCESSOR
INTEGER CPU CORE
83 - 87, 90
SINT (0) - SINT (2)
INT (3) - INT (5)
EXCEPTION/CONTROL REGISTERS
BUS INTERFACE REGISTERS
PORT SIZE REGISTER
COUNTER REGISTERS
GENERAL REGISTERS (32 × 32)
ALU
SHIFTER
MULTIPLY/DIVIDE
ADDRESS ADDER
PC CONTROL
81, 82
2
SBRCOND (2)
SBRCOND (3)
TC
80
VIRTUAL ADDRESS
32
PHYSICAL ADDRESS BUS
INSTRUCTION CACHE 2KB
DATA CACHE 512B
32
DATA BUS
48 - 46, 43 - 38,
35 - 30, 23 - 18,
15 - 10, 7 - 3
A/D (0) - A/D (31)
32
DATA UNPACK UNIT
4-DEEP WRITE BUFFER
DATA PACK UNIT
4-DEEP READ BUFFER
TIMING/ INTERFACE CONTROL
DMA ARBITER
BIU CONTROL
R3051 SUPERSET BUS INTERFACE UNIT
BUSREQ, BUSGNT
72, 67
RD, WR
61, 62
SYSCLK
66