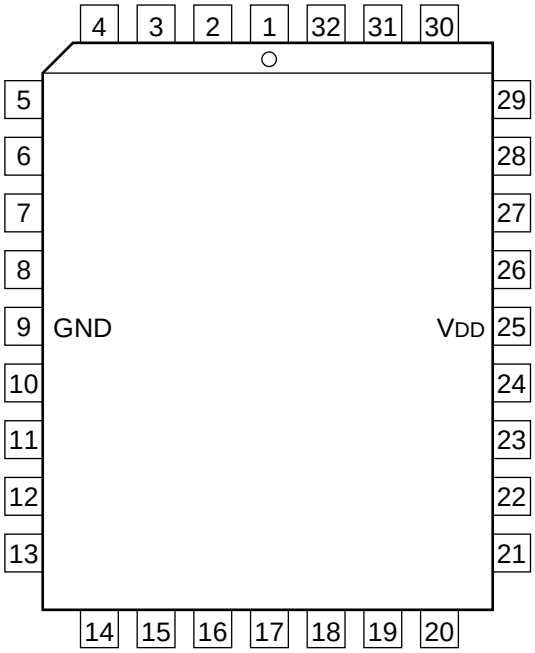
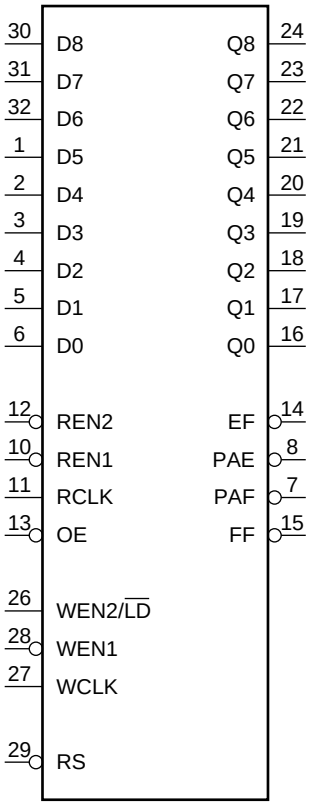
C-MOS (4,096 × 9)-BIT SYNCHRONOUS FIFO

—TOP VIEW—





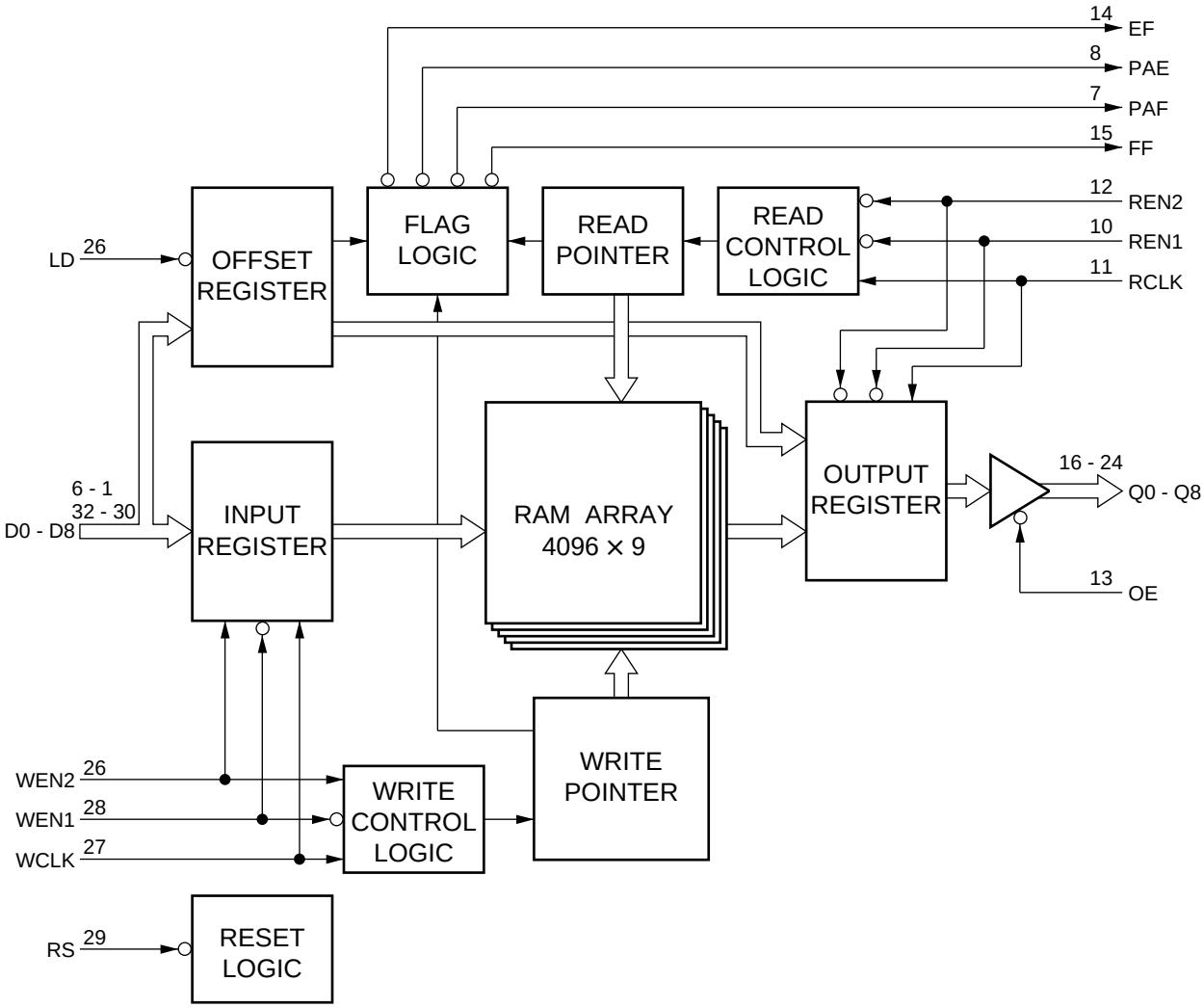
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	D5	12	I	$\overline{REN2}$	23	O	Q7
2	I	D4	13	I	$\overline{OE}$	24	O	Q8
3	I	D3	14	O	$\overline{EF}$	25	—	V_{DD}
4	I	D2	15	O	$\overline{FF}$	26	I	WEN2/$\overline{LD}$
5	I	D1	16	O	Q0	27	I	WCLK
6	I	D0	17	O	Q1	28	I	$\overline{WEN1}$
7	O	$\overline{PAF}$	18	O	Q2	29	I	$\overline{RS}$
8	O	$\overline{PAE}$	19	O	Q3	30	I	D8
9	—	GND	20	O	Q4	31	I	D7
10	I	$\overline{REN1}$	21	O	Q5	32	I	D6
11	I	RCLK	22	O	Q6			

INPUT

D0 - D8 ; DATA INPUTS
$\overline{OE}$; OUTPUT ENABLE
RCLK ; READ CLOCK
$\overline{REN1}$, $\overline{REN2}$; READ ENABLE 1, 2
$\overline{RS}$; RESET
WCLK ; WRITE CLOCK
$\overline{WEN1}$; WRITE ENABLE 1
WEN2/$\overline{LD}$; WRITE ENABLE 2/LOAD

OUTPUT

$\overline{EF}$; EMPTY FLAG
$\overline{FF}$; FULL FLAG
$\overline{PAE}$; PROGRAMMABLE ALMOST-EMPTY FLAG
$\overline{PAF}$; PROGRAMMABLE ALMOST-FULL FLAG
Q0 - Q8 ; DATA OUTPUTS


14
EF
8
PAE
7
PAF
15
FF
12
REN2
10
REN1
11
RCLK
LD
26
OFFSET REGISTER
FLAG LOGIC
READ POINTER
READ CONTROL LOGIC
6 - 1
32 - 30
D0 - D8
INPUT REGISTER
RAM ARRAY 4096 × 9
OUTPUT REGISTER
16 - 24
Q0 - Q8
13
OE
WEN2
26
WEN1
28
WCLK
27
WRITE CONTROL LOGIC
WRITE POINTER
RS
29
RESET LOGIC