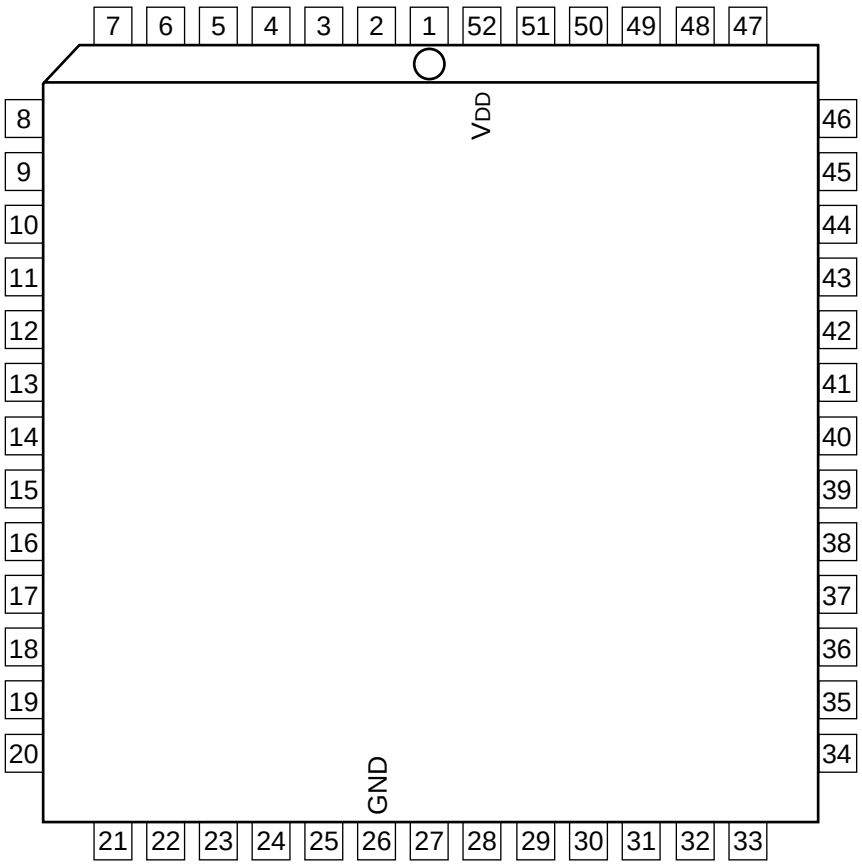
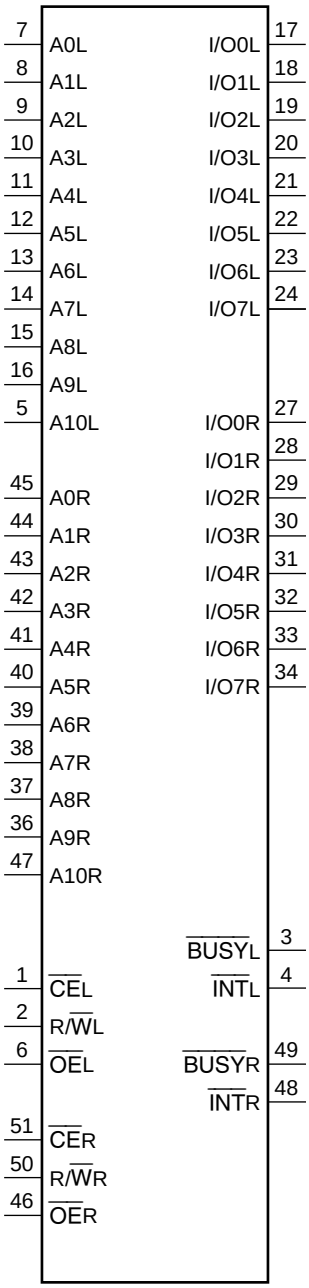
# C-MOS 16 K (2 K × 8)-BIT DUAL-PORT SRAM WITH INTERRUPT

—TOP VIEW—




| PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL | PIN NO. | I/O | SIGNAL |
|---|---|---|---|---|---|---|---|---|
| 1 | I | $\overline{CE}$L | 19 | I/O | I/O2L | 37 | I | A8R |
| 2 | I | R/$\overline{W}$L | 20 | I/O | I/O3L | 38 | I | A7R |
| 3 | O | $\overline{BUSY}$L | 21 | I/O | I/O4L | 39 | I | A6R |
| 4 | O | $\overline{INT}$L | 22 | I/O | I/O5L | 40 | I | A5R |
| 5 | I | A10L | 23 | I/O | I/O6L | 41 | I | A4R |
| 6 | I | $\overline{OE}$L | 24 | I/O | I/O7L | 42 | I | A3R |
| 7 | I | A0L | 25 | I/O | NC | 43 | I | A2R |
| 8 | I | A1L | 26 | — | GND | 44 | I | A1R |
| 9 | I | A2L | 27 | I/O | I/O0R | 45 | I | A0R |
| 10 | I | A3L | 28 | I/O | I/O1R | 46 | I | $\overline{OE}$R |
| 11 | I | A4L | 29 | I/O | I/O2R | 47 | I | A10R |
| 12 | I | A5L | 30 | I/O | I/O3R | 48 | O | $\overline{INT}$R |
| 13 | I | A6L | 31 | I/O | I/O4R | 49 | O | $\overline{BUSY}$R |
| 14 | I | A7L | 32 | I/O | I/O5R | 50 | I | R/$\overline{W}$R |
| 15 | I | A8L | 33 | I/O | I/O6R | 51 | I | $\overline{CE}$R |
| 16 | I | A9L | 34 | I/O | I/O7R | 52 | — | VDD |
| 17 | I/O | I/O0L | 35 | I/O | NC | | | |
| 18 | I/O | I/O1L | 36 | I | A9R | | | |

**INPUT**

| | | |
|---|---|---|
| A0L - A10L | : | ADDRESS LEFT |
| A0R - A10R | : | ADDRESS RIGHT |
| $\overline{BUSY}$L, $\overline{BUSY}$R | : | BUSY |
| $\overline{CE}$L, $\overline{CE}$R | : | CHIP ENBLE |
| $\overline{OE}$L, $\overline{OE}$R | : | OUTPUT ENABLE |
| R/$\overline{W}$L, R/$\overline{W}$R | : | READ/WITE ENABL |

**OUTPUT**

| | | |
|---|---|---|
| $\overline{INT}$L, $\overline{INT}$R | : | INTERRUPT |

**INPUT/OUTPUT**

| | | |
|---|---|---|
| I/O0L - I/O7L | : | DATA LEFT |
| I/O0R - I/O7R | : | DATA RIGHT |