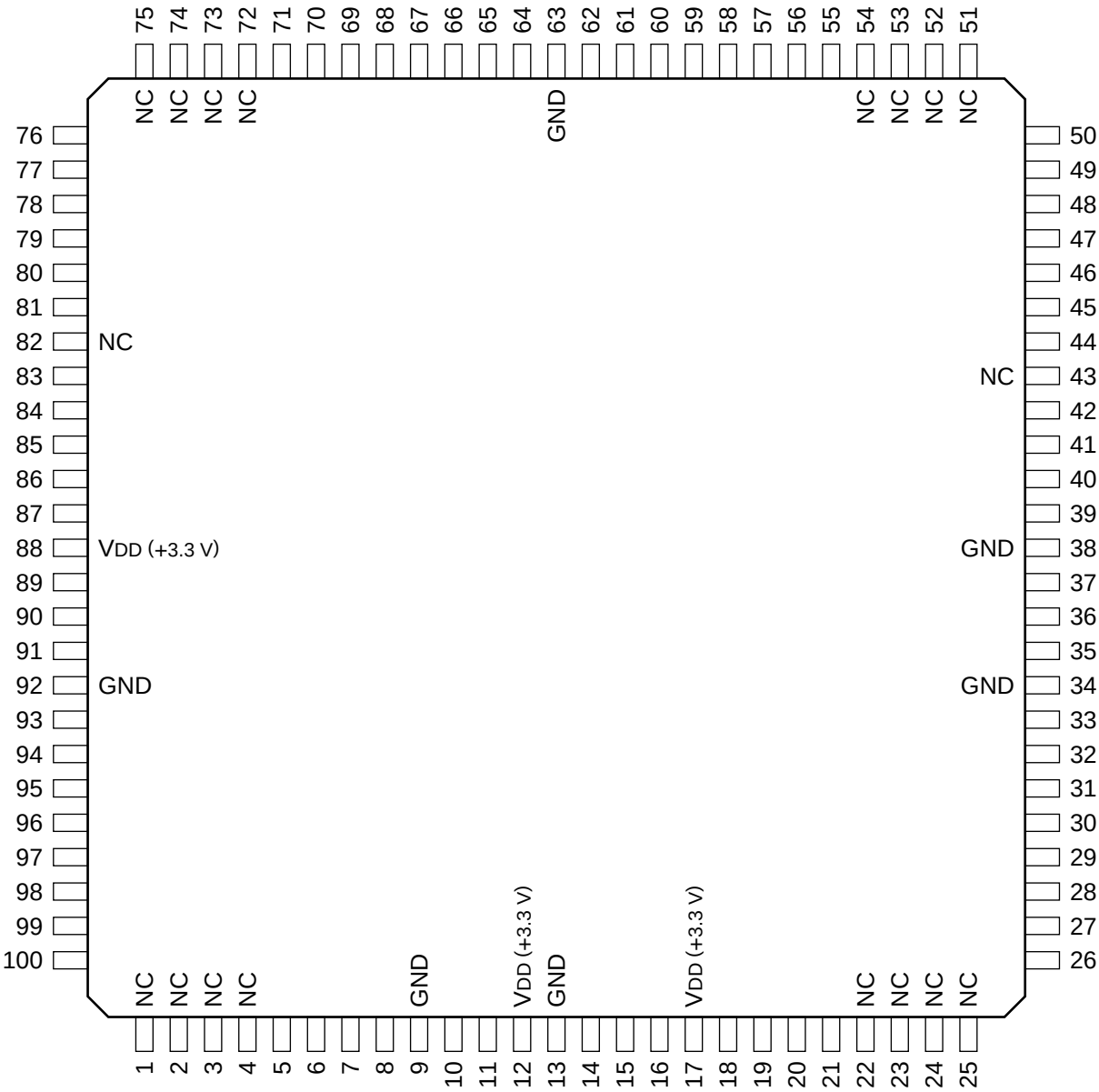
C-MOS 4 K × 16 DUAL-PORT STATIC RAM

—TOP VIEW—



(V_{DD} = +3.3 V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	26	I/O	$I/O7_R$	51	—	NC	76	I	$A6_L$
2	—	NC	27	I/O	$I/O8_R$	52	—	NC	77	I	$A7_L$
3	—	NC	28	I/O	$I/O9_R$	53	—	NC	78	I	$A8_L$
4	—	NC	29	I/O	$I/O10_R$	54	—	NC	79	I	$A9_L$
5	I/O	$I/O10_L$	30	I/O	$I/O11_R$	55	I	$A4_R$	80	I	$A10_L$
6	I/O	$I/O11_L$	31	I/O	$I/O12_R$	56	I	$A3_R$	81	I	$A11_L$
7	I/O	$I/O12_L$	32	I/O	$I/O13_R$	57	I	$A2_R$	82	—	NC
8	I/O	$I/O13_L$	33	I/O	$I/O14_R$	58	I	$A1_R$	83	I	$\overline{LB}_L$
9	—	GND	34	—	GND	59	I	$A0_R$	84	I	$\overline{UB}_L$
10	I/O	$I/O14_L$	35	I/O	$I/O15_R$	60	O	$\overline{INT}_R$	85	I	$\overline{CE}_L$
11	I/O	$I/O15_L$	36	I	$\overline{OE}_R$	61	O	$\overline{BUSY}_R$	86	I	$\overline{SEM}_L$
12	—	V_{DD}	37	I	$R/\overline{W}_R$	62	I	$M/\overline{S}$	87	I	$R/\overline{W}_L$
13	—	GND	38	—	GND	63	—	GND	88	—	V_{DD}
14	I/O	$I/O0_R$	39	I	$\overline{SEM}_R$	64	O	$\overline{BUSY}_L$	89	I	$\overline{OE}_L$
15	I/O	$I/O1_R$	40	I	$\overline{CE}_R$	65	O	$\overline{INT}_L$	90	I/O	$I/O0_L$
16	I/O	$I/O2_R$	41	I	$\overline{UB}_R$	66	I	$A0_L$	91	I/O	$I/O1_L$
17	—	V_{DD}	42	I	$\overline{LB}_R$	67	I	$A1_L$	92	—	GND
18	I/O	$I/O3_R$	43	—	NC	68	I	$A2_L$	93	I/O	$I/O2_L$
19	I/O	$I/O4_R$	44	I	$A11_R$	69	I	$A3_L$	94	I/O	$I/O3_L$
20	I/O	$I/O5_R$	45	I	$A10_R$	70	I	$A4_L$	95	I/O	$I/O4_L$
21	I/O	$I/O6_R$	46	I	$A9_R$	71	I	$A5_L$	96	I/O	$I/O5_L$
22	—	NC	47	I	$A8_R$	72	—	NC	97	I/O	$I/O6_L$
23	—	NC	48	I	$A7_R$	73	—	NC	98	I/O	$I/O7_L$
24	—	NC	49	I	$A6_R$	74	—	NC	99	I/O	$I/O8_L$
25	—	NC	50	I	$A5_R$	75	—	NC	100	I/O	$I/O9_L$

INPUT

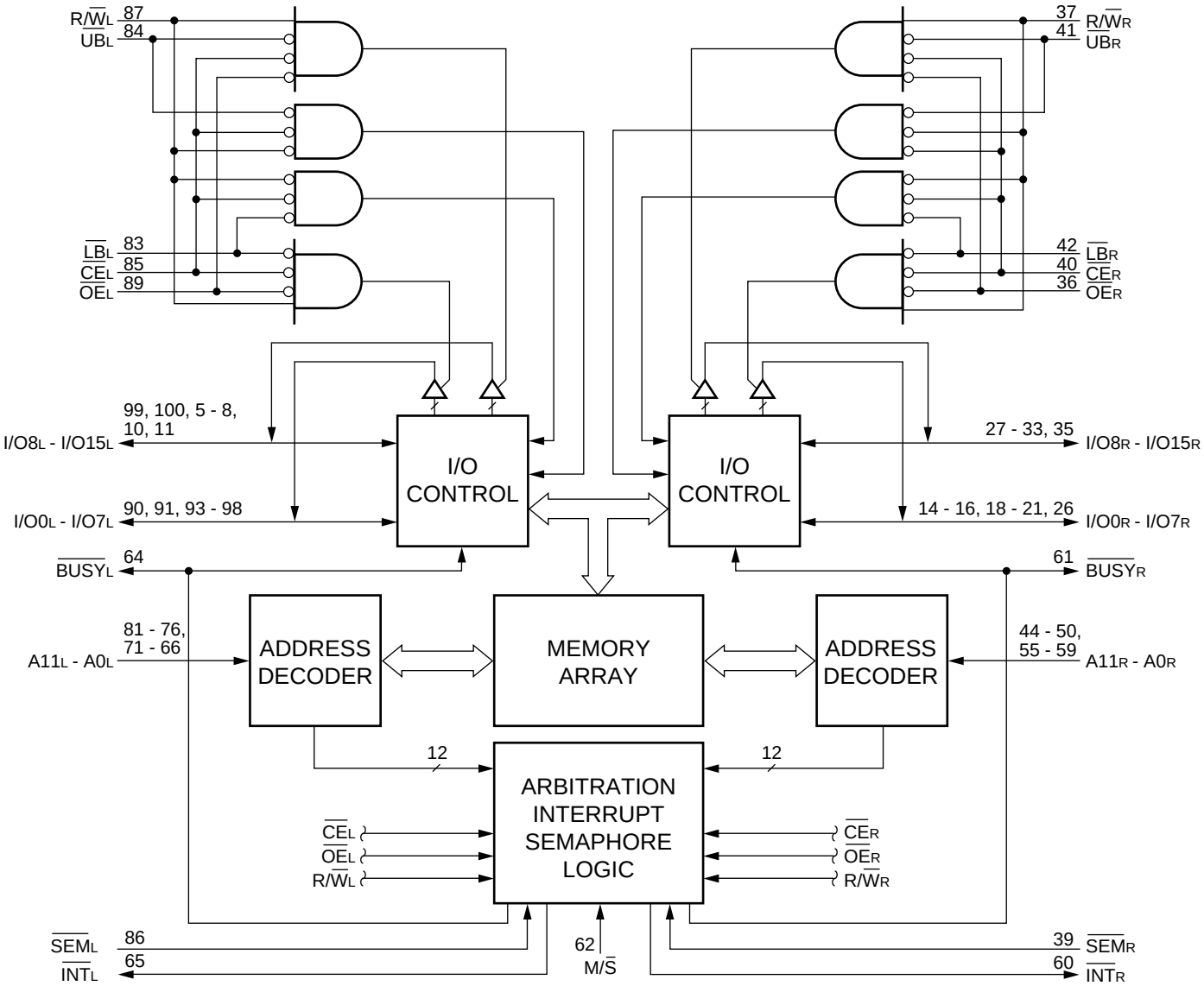
A0 - A11	:	ADDRESS
CE	:	CHIP ENABLE
LB	:	LOWER BYTE SELECT
M/S	:	MASTER/SLAVE SELECT
OE	:	OUTPUT ENABLE
R/W	:	READ/WRITE ENABLE
SEM	:	SEMAPHORE ENABLE
UB	:	UPPER BYTE SELECT

OUTPUT

BUSY	:	BUSY FLAG
INT	:	INTERRUPT FLAG

INPUT/OUTPUT

I/O0 - I/O15	:	DATA


R/W_L
87
UB_L
84
LB_L
83
CE_L
85
OE_L
89
37
R/W_R
41
UB_R
42
LB_R
40
CE_R
36
OE_R
99, 100, 5 - 8, 10, 11
I/O8_L - I/O15_L
I/O CONTROL
I/O CONTROL
27 - 33, 35
I/O8_R - I/O15_R
I/O0_L - I/O7_L
90, 91, 93 - 98
14 - 16, 18 - 21, 26
I/O0_R - I/O7_R
BUSY_L
64
61
BUSY_R
81 - 76, 71 - 66
A11_L - A0_L
ADDRESS DECODER
MEMORY ARRAY
ADDRESS DECODER
44 - 50, 55 - 59
A11_R - A0_R
12
12
ARBITRATION INTERRUPT SEMAPHORE LOGIC
CE_L
OE_L
R/W_L
CE_R
OE_R
R/W_R
SEM_L
86
INT_L
65
62
M/S
39
SEM_R
60
INT_R