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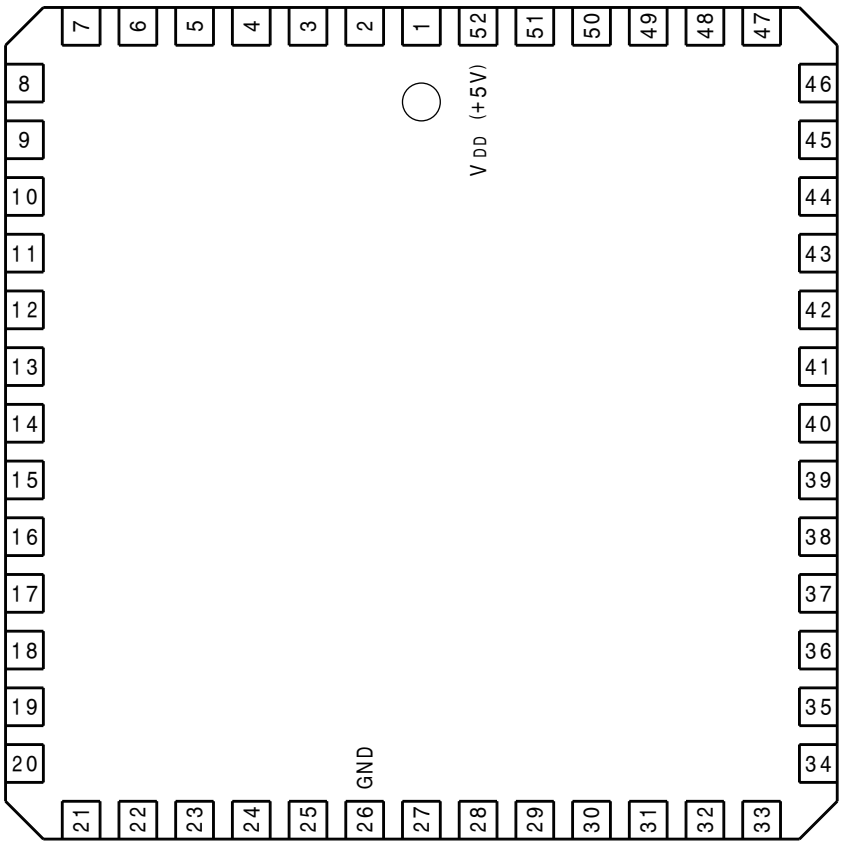
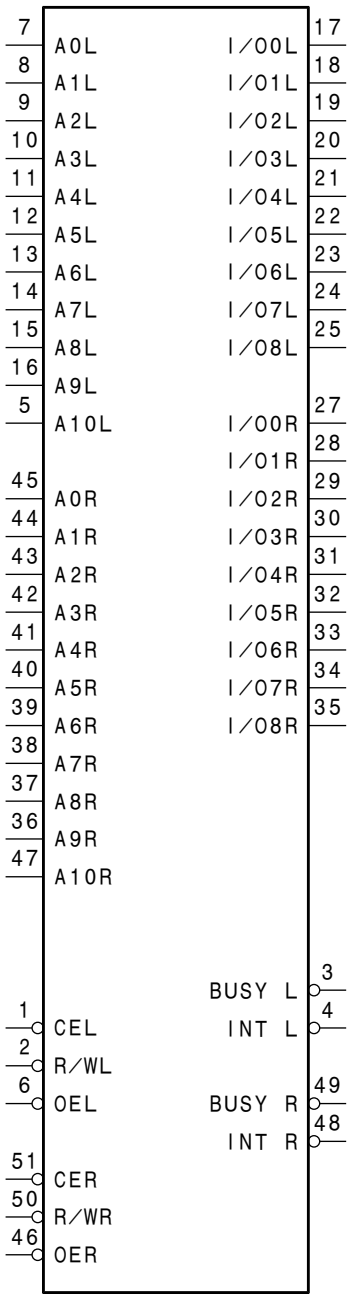
C-MOS 2Kx9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

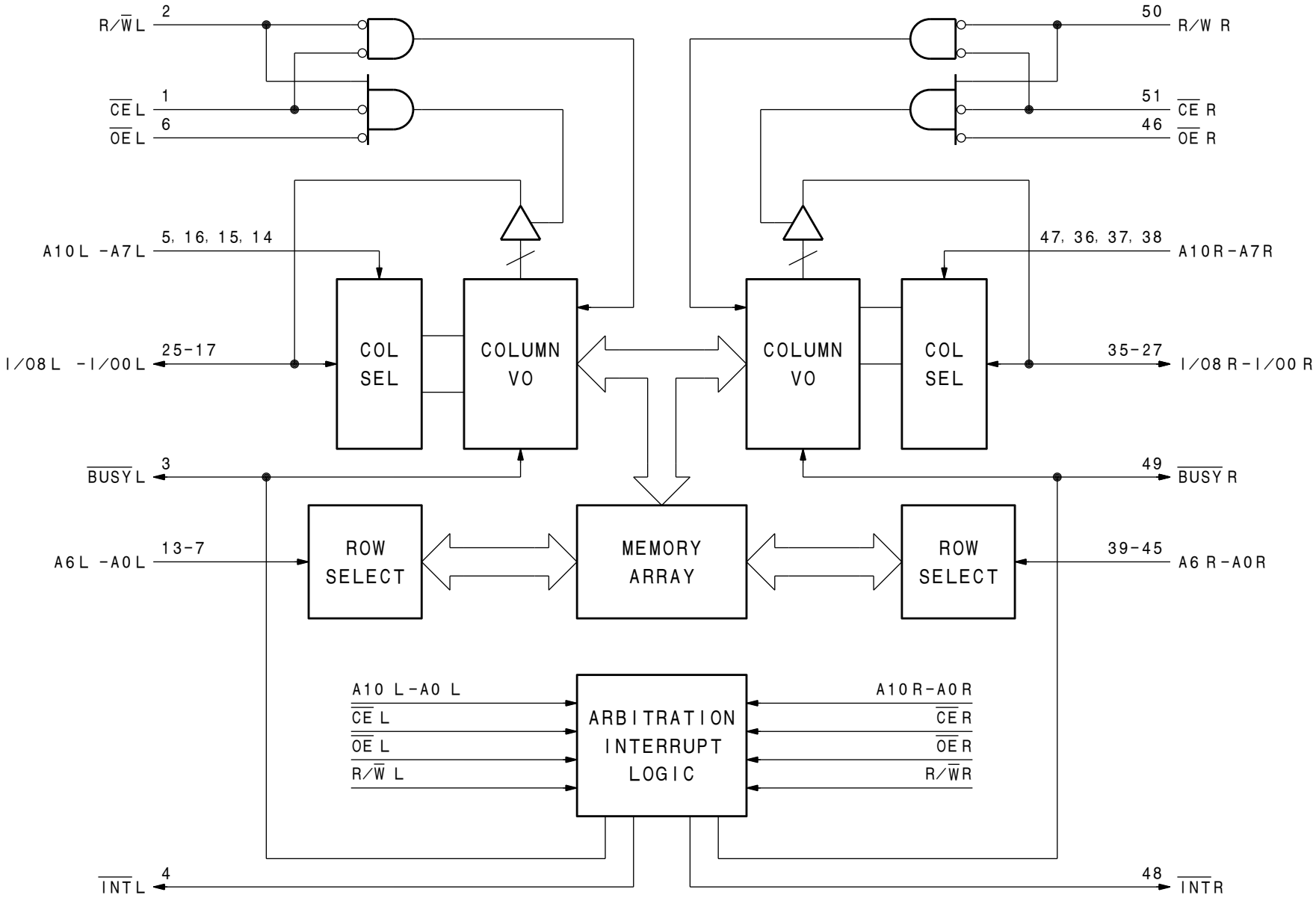
-TOP VIEW-



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	$\overline{CE}$ L	19	I/O	I/O 2L	37	I	A8R
2	I	R/$\overline{W}$ L	20	I/O	I/O 3L	38	I	A7R
3	O	$\overline{BUSY}$ L	21	I/O	I/O 4L	39	I	A6R
4	O	$\overline{INT}$ L	22	I/O	I/O 5L	40	I	A5R
5	I	A10L	23	I/O	I/O 6L	41	I	A4R
6	I	$\overline{OE}$L	24	I/O	I/O 7L	42	I	A3R
7	I	A0L	25	I/O	I/O 8L	43	I	A2R
8	I	A1L	26	-	GND	44	I	A1R
9	I	A2L	27	I/O	I/O 0R	45	I	A0R
10	I	A3L	28	I/O	I/O 1R	46	I	$\overline{OE}$ R
11	I	A4L	29	I/O	I/O 2R	47	I	A10R
12	I	A5L	30	I/O	I/O 3R	48	O	$\overline{INT}$R
13	I	A6L	31	I/O	I/O 4R	49	O	$\overline{BUSY}$R
14	I	A7L	32	I/O	I/O 5R	50	I	R/$\overline{W}$R
15	I	A8L	33	I/O	I/O 6R	51	I	$\overline{CE}$R
16	I	A9L	34	I/O	I/O 7R	52	-	Vcc (+5V)
17	I/O	I/O 0L	35	I/O	I/O 8R			
18	I/O	I/O 1L	36	I	A9R			



A0L-A10L,
A0R-A10R ; ADDRESS INPUTS
BUSYL, BUSYR ; BUSY INPUTS
CEL, CER ; CHIP ENBLE INPUTS
I/O0L-I/O10L,
I/O0R-I/O10R ; DATA INPUTS/OUTPUTS
INTL, INTR ; INTERRUPT OUTPUTS
OEL, OER ; OUTPUT ENABLE INPUTS
R/$\overline{W}$L, R/$\overline{W}$R ; READ/WITE ENABLE INPUTS


R/W L
2
CE L
1
OE L
6
A10L -A7L
5, 16, 15, 14
I/O8L -I/O0L
25-17
BUSY L
3
A6L -A0L
13-7
INT L
4
COL SEL
COLUMN VO
ROW SELECT
MEMORY ARRAY
ROW SELECT
COLUMN VO
COL SEL
A10 L-A0 L
CE L
OE L
R/W L
ARBITRATION INTERRUPT LOGIC
A10R-A0R
CE R
OE R
R/W R
50
R/W R
51
CE R
46
OE R
47, 36, 37, 38
A10R-A7R
35-27
I/O8 R-I/O0 R
49
BUSY R
39-45
A6 R-A0R
48
INT R