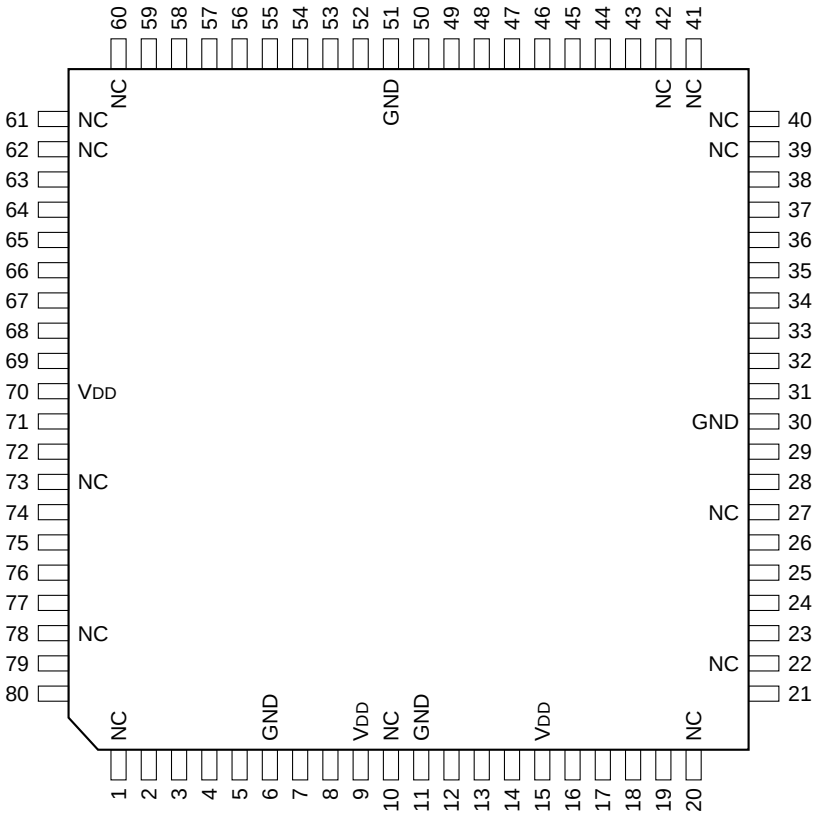
C-MOS 256 K (32,768 × 8)-BIT DUAL-PORT SRAM

—TOP VIEW—



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	NC	21	I/O	I/O7R	41	—	NC	61	—	NC
2	I/O	I/O2L	22	—	NC	42	—	NC	62	—	NC
3	I/O	I/O3L	23	I	$\overline{OE}$R	43	I	A4R	63	I	A6L
4	I/O	I/O4L	24	I	R/$\overline{W}$R	44	I	A3R	64	I	A7L
5	I/O	I/O5L	25	I	$\overline{SEM}$R	45	I	A2R	65	I	A8L
6	—	GND	26	I	$\overline{CE}$R	46	I	A1R	66	I	A9L
7	I/O	I/O6L	27	—	NC	47	I	A0R	67	I	A10L
8	I/O	I/O7L	28	I	A14R	48	O	$\overline{INT}$R	68	I	A11L
9	—	VDD	29	I	A13R	49	O	$\overline{BUSY}$R	69	I	A12L
10	—	NC	30	—	GND	50	I	M/$\overline{S}$	70	—	VDD
11	—	GND	31	I	A12R	51	—	GND	71	I	A13L
12	I/O	I/O0R	32	I	A11R	52	O	$\overline{BUSY}$L	72	I	A14L
13	I/O	I/O1R	33	I	A10R	53	O	$\overline{INT}$L	73	—	NC
14	I/O	I/O2R	34	I	A9R	54	I	A0L	74	I	$\overline{CE}$L
15	—	VDD	35	I	A8R	55	I	A1L	75	I	$\overline{SEM}$L
16	I/O	I/O3R	36	I	A7R	56	I	A2L	76	I	R/$\overline{W}$L
17	I/O	I/O4R	37	I	A6R	57	I	A3L	77	I	$\overline{OE}$L
18	I/O	I/O5R	38	I	A5R	58	I	A4L	78	—	NC
19	I/O	I/O6R	39	—	NC	59	I	A5L	79	I/O	I/O0L
20	—	NC	40	—	NC	60	—	NC	80	I/O	I/O1L

INPUT

$A0_R$ - $A14_R$, $A0_L$ - $A14_L$	:	ADDRESS
$\overline{CE}_R$, $\overline{CE}_L$	:	CHIP ENABLE
M/$\overline{S}$	:	CONTROL/CONTROLLED SELECT
$\overline{OE}_R$, $\overline{OE}_L$	:	OUTPUT ENABLE
R/$\overline{W}_R$, R/$\overline{W}_L$	:	READ/WRITE ENABLE
$\overline{SEM}_R$, $\overline{SEM}_L$	:	SEMAPHORE ENABLE

OUTPUT

$\overline{BUSY}_R$, $\overline{BUSY}_L$	:	BUSY FLAG
$\overline{INT}_R$, $\overline{INT}_L$	:	INTERRUPT FLAG

INPUT/OUTPUT

$I/O0_R$ - $I/O7_R$, $I/O0_L$ - $I/O7_L$	:	DATA