FLASH MEMORY CARD

ID242 Series

2MB, 4MB, 8MB

PRODUCT OVERVIEW

SHARP

CPS0002-000@Aug.1997

Contents

1. Introduction

This datasheet is for SHARP's ID242 series flash memory card. This datasheet provides all AC and DC characteristics (including timing waveforms) and a convenient reference for the device command set and the card's integrated registers(including the LH28F008SC's status registers). This datasheet provides description of the methods which are very helpful for customer to use the card.

2. Features

2.1 Type Flash Memory Card

2.2 Overview

	ID242Dxx	ID242Exx	ID242Gxx
Common Memory Capacity	2M words × 8bits 1Mwords × 16bits	4M words × 8bits 2M words × 16bits	8M words × 8bits 4M words × 16bits
Attribute Memory Capasity	2KBytes		
Supply Voltage	Smart Voltage		
Access time	150ns(@Vcc=5v) 250ns(@Vcc=3.3v)		
Erase Unit	64K word blocks		
Program/Erase Cycles	100,000cycles/Block		
External Dimensions	54.0 × 85.6 × 3.3mm PCMCIA Type 1		

2.3 Interface Parallel I/O Interface

2.4 Function Table See Function Table in page. 9

2.5 Pin Connections See Pin Connections in page. 6

2.6 Type of Connector Conforms to PCMCIA PC Card Standard 95 Card Use Connector
(Card connector: JC20-J68S-NB3 JAE or FCN-568J068-G/0 Fujitsu)

2.7 Operating Temperature 0 to 60°C

2.8 Storage Temperature -20 to 65°C

2.9 Not designed for rated radiation hardened.

3. Block Diagram (For example: 8MB)

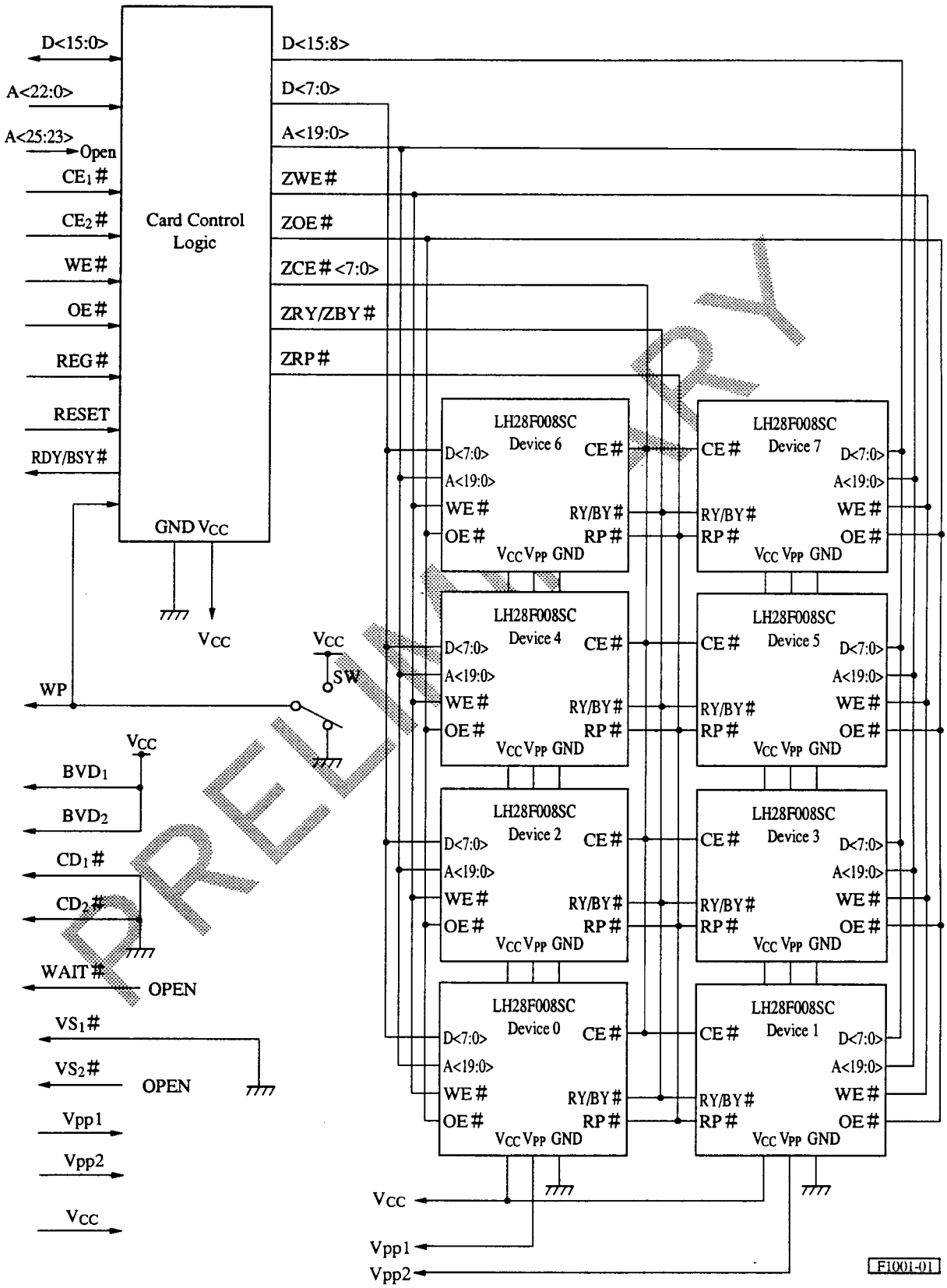


Figure 1. Block Giagram for ID242-8MB

4. Pin Connections

Table 1. Pin Connections

PIN No.	SIGNAL	I/O	FUNCTION	ACTIVE
1	GND		Ground	
2	D_3	I/O	Data Bit 3	
3	D_4	I/O	Data Bit 4	
4	D_5	I/O	Data Bit 5	
5	D_6	I/O	Data Bit 6	
6	D_7	I/O	Data Bit 7	
7	CE_1#	I	Card Enable 1	LOW
8	A_{10}	I	Address Bit 10	
9	OE#	I	Output Enable	LOW
10	A_{11}	I	Address Bit 11	
11	A_9	I	Address Bit 9	
12	A_8	I	Address Bit 8	
13	A_{13}	I	Address Bit 13	
14	A_{14}	I	Address Bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready Busy	LOW
17	V_{CC}		Supply Voltage	
18	V_{PP1}		Program Voltage	
19	A_{16}	I	Address Bit 16	
20	A_{15}	I	Address Bit 15	
21	A_{12}	I	Address Bit 12	
22	A_7	I	Address Bit 7	
23	A_6	I	Address Bit 6	
24	A_5	I	Address Bit 5	
25	A_4	I	Address Bit 4	
26	A_3	I	Address Bit 3	
27	A_2	I	Address Bit 2	
28	A_1	I	Address Bit 1	
29	A_0	I	Address Bit 0	
30	D_0	I/O	Data Bit 0	
31	D_1	I/O	Data Bit 1	
32	D_2	I/O	Data Bit 2	
33	WP	O	Write Protect	HIGH
34	GND		Ground	

PIN No.	SIGNAL	I/O	FUNCTION	ACTIVE
35	GND		Ground	
36	CD_1#	O	Card Detect 1	LOW
37	D_{11}	I/O	Data Bit 11	
38	D_{12}	I/O	Data Bit 12	
39	D_{13}	I/O	Data Bit 13	
40	D_{14}	I/O	Data Bit 14	
41	D_{15}	I/O	Data Bit 15	
42	CE_2#	I	Card Enable 2	LOW
43	VS_1#	O	Voltage Sense 1	LOW
44	RFU		Reserved	
45	RFU		Reserved	
46	A_{17}	I	Address Bit 17	
47	A_{18}	I	Address Bit 18	
48	A_{19}	I	Address Bit 19	
49	A_{20}	I	Address Bit 20	
50	A_{21}	I	Address Bit 21	
51	V_{CC}		Supply Voltage	
52	V_{PP2}		Program Voltage	
53	A_{22}	I	Address Bit 22	
54	A_{23}	I	Address Bit 23	
55	A_{24}	I	Address Bit 24	
56	A_{25}	I	Address Bit 25	
57	VS_2#	O	Voltage Sense 2	N.C.
58	RESET	I	Reset	HIGH
59	RFU		Reserved	
60	RFU		Reserved	
61	REG#	I	Atribute Memory Select	
62	BVD_2	O	Battery Boltage Detect 2	
63	BVD_1	O	Battery Boltage Detect 1	
64	D_8	I/O	Data Bit 8	
65	D_9	I/O	Data Bit 9	
66	D_{10}	I/O	Data Bit 10	
67	CD_2#	O	Card Detect 2	LOW
68	GND		Ground	

5. Signal Description

Table 2. Signal Description

Symbol	I/O	Electrical Interface	Function
A_0-A_{25}	I	Pull-down (250kΩ @Vcc=5v)	ADDRESS INPUTS: Address A0 through A22 are address bus lines which enable direct addressing of up to 8MB of memory on the card. Signal A0 is not used in word access mode. A23 through A25 are open. The system should NOT try to access memory beyond the card's density, because the upper addresses are not decoded.
D_0-D_{15}	I/O	Pull-down (250kΩ @Vcc=5v)	DATA INPUT/OUTPUT: D0 through D15 constitute the bi-directional data bus. D15 is the most significant bit.
CE_1#,CE_2#	I	Pull-up (250kΩ @Vcc=5v)	CARD ENABLE 1 & 2: CE1# enables even byte, CE2# enables odd byte.
OE#	I	Pull-up (250kΩ @Vcc=5v)	OUTPUT ENABLE: Active low signal gating read data from the memory card.
WE#	I	Pull-up (250kΩ @Vcc=5v)	WRITE ENABLE: Active low signal gating write data to the memory card.
RDY/BSY#	O		READY/BUSY OUTPUT: Indicates status of internally timed erase or write activities. ID242 series has two types of Ready/Busy output mode; PCMCIA mode and High-Performance mode. In PCMCIA mode, a high output indicates the memory card is ready to accept accesses. A low output indicates that a device in the memory card is busy. In High-Performance mode, the card outputs low when the card is in default state. A high output indicates at least one of flash memory devices in the card comes to be ready to accept accesses.
CD_1#, CD_2#	O	Pull-down 0Ω	CARD DETECT 1 & 2: These signals provide for card insertion detection. The signals are connected to ground internally on the memory card, and will be forced low whenever a card is placed in the socket. The host socket interface circuitry shall supply 10K or larger pull-up resistors on these signal pins.
WP	O	Low:Pull-down 0Ω High:Pull-up 100kΩ	WRITE PROTECT: Write Protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected.
V_{PP1}, V_{PP2}			WRITE/ERASE POWER SUPPLY 1 & 2:
V_{CC}			CARD POWER SUPPLY:
GND			GROUND:
REG#	I	Pull-up (250kΩ@Vcc=5v)	REGISTER SELECT: Provides access to attribute memory when REG# is low.
RESET	I	Pull-up (250kΩ@Vcc=5v)	RESET: Active high signal for placing card in Power-On Default State.
BVD_1, BVD_2	O	Pull-up 100kΩ	BATTERY VOLTAGE DETECT 1 & 2: These signals are pulled high to maintain SRAM card compatibility.
VS_1#, VS_2#	O	VS_1#: Pull-down VS_2#: N.C.	VOLTAGE SENSE 1 & 2: Notifies the host socket of the card's VCC requirements. VS1# is pulled down to ground and VS2# is open indicates a 3.3V/5V card has been inserted.
RFU			RESERVED FOR FUTURE USE

6. Functions

6. 1 Common Memory

6. 1. 1 Common Memory Architecture

Figure 2 shows common memory architecture of ID242 series flash memory card. Device pair is consisted of two pieces of 8Mbit flash memory devices. Each device has 16 distinct, individually erasable and lockable blocks. All blocks are divided into odd bytes and even bytes.

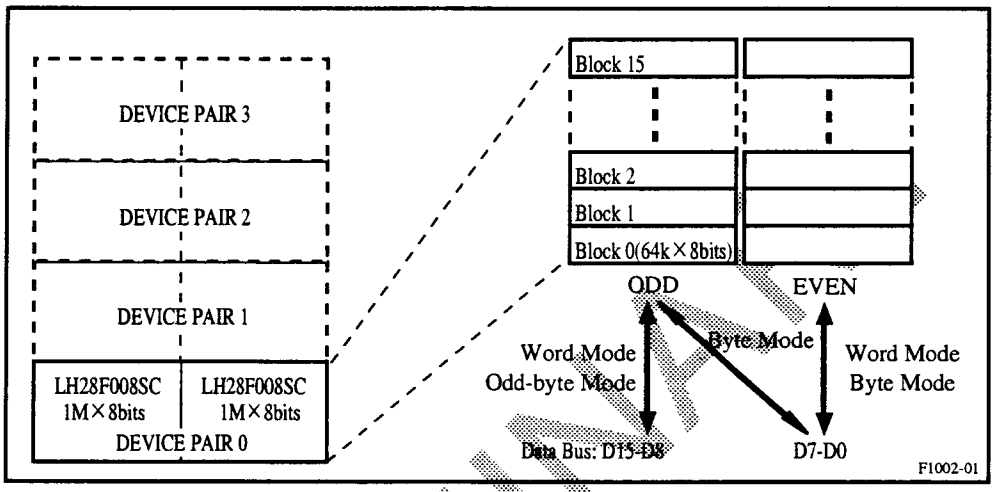


Figure 2. Common Memory Architecture

Each device pair and block is selected by address bits. Table 3 shows definitions of address bits.

Table 3. Address Difinitions

A_0	Select Even/Odd byte in the byte access mode.
A_{16}-A_1	Select address in the block.
A_{20}-A_{17}	Select a block.
A_{25}-A_{21}	Select a device pair.

6. 1. 2 Erase

Erase is executed one block at a time. Erasable block size is 64K bytes in byte access mode and 128K bytes in word access mode.

6. 1. 3 Address Decoding

The higher address area of ID242 series flash memory card which goes beyond common memory area is not decoded in common memory access. It means that the system will access to random memory address of the memory card even if system will try to access to the memory address which exceeds memory capacity of the card. Please do not access to the memory address which goes beyond memory capacity of the card.

As an enhanced function, the memory card enables to output invalid data (either of 0000h or FFFFh) when system will access to the memory address which exceeds memory capacity of the card. Please contact our sales & marketing people to find concrete way of setting.

6. 2 Attribute Memory

Figure 3 shows attribute memory architecture of ID242 series flash memory card. Attribute memory is contained within the Card Control Logic. Attribute memory contains the Card Information Structure (CIS) and Component Management Registers (CMRs). The CIS contains tuple information and is located at even byte addresses beginning with address 0000h (Please refer to section 7). The standard CIS of ID242 series flash memory card is hardwired and is for read only. As an enhanced function, the hardwired CIS area is switchable to EEPROM so that customer can program required CIS. Please contact our sales & marketing people to find concrete way of setting. The CMRs are located at even byte addresses beginning with address 4000h (Please refer to section 9).

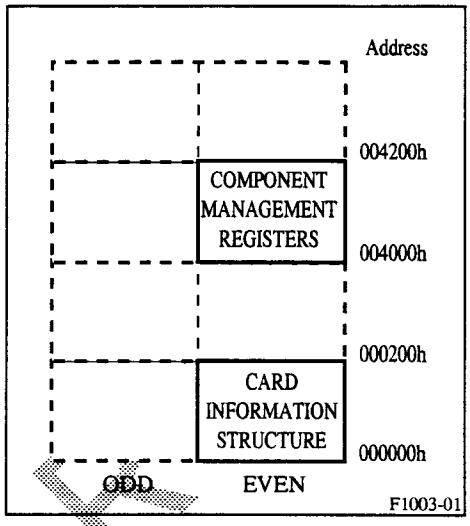


Figure 3. Attribute Memory Map

6. 3 Function Table

6. 3. 1 Common Memory Access

Table 4. Common Memory Access

Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	$D_{15\sim8}$	$D_{7\sim0}$
Stand-by	X	H	H	X	X	X	High-Z	High-Z
Byte Read	H	H	L	L	L	H	High-Z	Even
	H	H	L	H	L	H	High-Z	Odd
Word Read	H	L	L	X	L	H	Odd	Even
Odd Byte Read	H	L	H	X	L	H	Odd	High-Z
Byte Write	H	H	L	L	H	L	Don't care	Even
	H	H	L	H	H	L	Don't care	Odd
Word Write	H	L	L	X	H	L	Odd	Even
Odd Byte write	H	L	H	X	H	L	Odd	Don't care

6. 3. 2 Attribute Memory Access

Table 5. Attribute Memory Access

Mode	REG#	CE_2#	CE_1#	A_0	OE#	WE#	$D_{15\sim8}$	$D_{7\sim0}$
Stand-by	X	H	H	X	X	X	High-Z	High-Z
Byte Read	L	H	L	L	L	H	High-Z	Even
	L	H	L	H	L	H	High-Z	XXX
Word Read	L	L	L	X	L	H	XXX	Even
Odd Byte Read	L	L	H	X	L	H	XXX	High-Z
Byte Write	L	H	L	L	H	L	Don't care	Even
	L	H	L	H	H	L	Don't care	Don't care
Word Write	L	L	L	X	H	L	Don't care	Even
Odd Byte write	L	L	H	X	H	L	Don't care	Don't care

XXX: Output data is invalid.

The standard CIS is for read only. Write operation is only for CMRs and CIS on EEPROM.

6. 4 Enhancement Functions

ID242 series flash memory card contains enhanced control functions. By taking advantage of these enhancement functions, this card provides innovative capabilities, low-power operation and very high read/write performance. These enhancement functions are achieved by CMRs.(Please refer to section 9)

Table 6. Enhancement Functions

Enhancement Functions	Function Preview
Soft Reset	Initiates internal automation of the memory card by seftware reset.
Sleep Control	Puts specified device pair(s) in deep power-down mode.
Ready/Busy Monitor	Indicates the RDY/BSY# status of each flash memory device to Ready/Busy Status Register.
Ready/Busy Mask	Masks RDY/BSY# status of each flash memory device.
Ready/Busy Mode	Select RDY/BSY# output mode which PCMCIA mode or High-Performance mode.
Software Write Protect	Executes write protect by sofware control, without Write Protect Switch.
Soket and Copy Entry	If the similar cards installed in a system, the system can distinguish each card by this function.

6. 4. 1 Soft Reset

The card become the reset state by setting the SRESET bit of the Configuration Option Register to "1". It is a similar function to hardware reset by the card's RESET without the SRESET bit status. The SRESET bit must be cleared("0") to enable access to the card.

6. 4. 2 Sleep Control

Writing "1" to the PWDN bit of the Configuration Status Register puts selected device pairs by the Sleep Control Register into the deep power-down mode. It means keeping down the stand-by current.

6. 4. 3 Ready/Busy Monitor

The Ready/Busy Status Register indicates the RDY/BSY# status of each device. It means that the system can confirm the RDY/BSY# status of each device when the card's RDY/BSY# is in the High-Performance mode, the device's RDY/BSY# is masked or the card is in other mode.

6. 4. 4 Ready/Busy Mask

With setting the appropriate bits of the Ready/Busy Mask Register to "1" , the corresponding device's RDY/BSY# signals are masked for card's RDY/BSY# output.

6. 4. 5 Ready/Busy Mode

ID242 series has two types of Ready/Busy output mode; PCMCIA mode and High-Performance mode. In PCMCIA mode, a high output indicates the memory card is ready to accept accesses. A low output indicates that a device in the memory card is busy. In High-Performance mode, the card outputs low when the card is in default state. A high output indicates at least one of flash memory devices in the card comes to be ready to accept

accesses. The system must clear the RACK bit of the Rady/Busy Mode Register after receiving ready status to prepare for next device's ready transition.

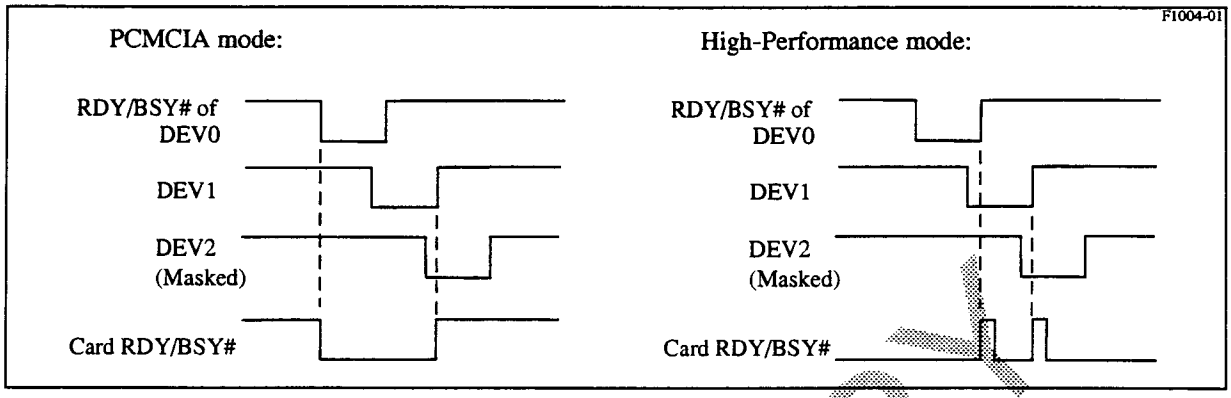


Figure 4. RDY/BSY# Output Mode

6. 4. 6 Software Write Protect

ID242 series flash memory card can provide Common Memory CIS (CMCIS) with first block (64Kwords in word access mode or 128KBytes in byte access mode) of the common memory. The Write Protection Register can protect the common memory or CMCIS by sofware. By setting the CMWP bit of Write Protection Register to "1" , the common memory without the CMCIS area is protected from write operation. And by setting the CISWP bit to "1" , the CMCIS area is protected from write operation. Software write protection is available when the write protect switch of the card is located writable position.

6. 4. 7 Socket and Copy Entry

If the similar cards installed in a system, the system can distinguish these cards by writing the Socket Number and Copy Number in the Socket and Copy Register of each card (Please refer to section 9). The Socket Number should be written in D0-D3 of Socket and Copy Register. This field indicates to the card that it is located in the n'th socket. The Copy Number should be written in D4-D6 of Socket and Copy Register. This field indicates to the card that it is n'th copy of the card installed in the system which is identically configured. PC cards which indicate in their CIS that they support more than one copy of identically configured card, should have a copy number (0 to MAX twin cards, MAX=n-1) written back to the Socket and Copy Register.

6. 5 SmartVoltage

SmartVoltage technology provides a choice of VCC and VPP combinations as shown in Table 7. VPP is converted to 12V automatically in each common memory device. For correct conversion, VPP must be provided VPP1, VPP2 or VPP3 from the system (Please refer to Section 12). Giving the higher VPP voltage provides the higher performance, for example, reduce the write/erase operation current or shorten the write/erase time.

Table 7. SmartVoltage

V_{CC}	V_{PP}
3.3V	3.3V, 5V, 12V
5V	5V, 12V

7. Card Information Structure (CIS)

The CIS is contained within attribute memory (Please refer to section 6.2). Table 8 shows standard CIS tuples, but it is for read only. As an enhanced function, the hardwired CIS area is switchable to EEPROM so that customer can program required CIS. Please contact our sales & marketing people to find concrete way of setting.

Table 8. Standard CIS

Address	Value	Description
00h	01h	Device Info (Common Memory)
02h	04h	Tuple Link
04h	57h	Flash Memory
06h	22h	Access Time 150ns
08h	06h 0Eh 1Eh	Capacity 2MB 4MB 8MB
0Ah	FFh	End of Tuple
0Ch	1Ch	Device Info (Common Memory Other Conditions)
0Eh	05h	Tuple Link
10h	02h	Conditions 3Vcc
12h	57h	Flash Memory
14h	32h	Access Time 250ns
16h	06h 0Eh 1Eh	Capacity 2MB 4MB 8MB
18h	FFh	End of Tuple
1Ah	17h	Device Info ID (Attribute Memory)
1Ch	04h	Tuple Link
1Eh	1Fh	ROM
20h	2Ah	Access Time 200ns
22h	01h	Capacity 2KB
24h	FFh	End of Tuple
26h	1Dh	Device Info ID (Attribute Memory)
28h	05h	Tuple Link
2Ah	02h	Conditions 3Vcc
2Ch	17h	ROM

Address	Value	Description
2Eh	2Ah	Access Time 200ns
30h	01h	Capacity 2KB
32h	FFh	End of Tuple
34h	18h	JEDEC Code ID
36h	02h	Tuple Link
38h	89h	Manufacture Code
3Ah	A6h	Device Code
3Ch	00h	End of Tuple
3Eh	15h	Version Info Level 1
40h	23h	Tuple Link
42h	04h	Major Version
44h	01h	Minor Version
46h	53h	S :Product Info
48h	48h	H
4Ah	41h	A
4Ch	52h	R
4Eh	50h	P
50h	00h	END TEXT
52h	49h	I
54h	44h	D
56h	32h	2
58h	34h	4
5Ah	53h	S
5Ch	52h	R
5Eh	20h	SPACE
60h	00h	END TEXT
62h	53h	S :Maker Info
64h	48h	H
66h	41h	A
68h	52h	R

Table 8. Standard CIS (Continued)

Address	Value	Description
6Ah	50h	P
6Ch	20h	SPACE
6Eh	43h	C
70h	4Fh	O
72h	52h	R
74h	50h	P
76h	4Fh	O
78h	52h	R
7Ah	41h	A
7Ch	54h	T
7Eh	49h	I
80h	4Fh	O
82h	4Eh	N
84h	00h	END TEXT
86h	FFh	End of Tuple
88h	1Ah	Configuration Info
8Ah	05h	Tuple Link
8Ch	01h	2 Bytes Field
8Eh	06h	Last Index of Configuration Table
90h	00h	CMRs Base Adress
92h	40h	CMRs Base Adress
94h	0Bh	CMR Mask
96h	00h	Null
98h	1Bh	Configuration Table Entry 1
9Ah	0Fh	Tuple Link
9Ch	01h	Index
9Eh	02h	Vcc & Vpp
A0h	79h	Parameter Selection
A2h	55h	Vcc Voltage 5V
A4h	0Ch	Icc Static 1.2mA
A6h	06h	Icc Average 100mA
A8h	06h	Icc Peak 100mA
AAh	23h	Icc Powerdown 50μ A
ACh	79h	Parameter Selection
AEh	D5h	Vpp Voltage 5V
B0h	7Dh	NC OK
B2h	1Bh	Ipp Static 150μ A
B4h	75h	Ipp Average 80mA
B6h	75h	Ipp Peak 80mA
B8h	52h	Ipp Powerdown 50μ A
BAh	1Bh	Configuration Table Entry 2
BCh	0Fh	Tuple Link

Address	Value	Description
BEh	02h	Index
C0h	02h	Vcc & Vpp
C2h	79h	Parameter Selection
C4h	55h	Vcc Voltage 5V
C6h	0Ch	Icc Static 1.2mA
C8h	06h	Icc Average 100mA
CAh	06h	Icc Peak 100mA
CCh	23h	Icc Powerdown 50μ A
CEh	79h	Parameter Selection
D0h	8Eh	Vpp Voltage 12V
D2h	7Dh	NC OK
D4h	1Bh	Ipp Static 150μ A
D6h	35h	Ipp Average 30mA
D8h	35h	Ipp Peak 30mA
DAh	52h	Ipp Powerdown 50μ A
DCh	1Bh	Configuration Table Entry 3
DEh	11h	Tuple Link
E0h	03h	Index
E2h	02h	Vcc & Vpp
E4h	79h	Parameter Selection
E6h	B5h	Vcc Voltage 3.3V
E8h	1Eh	
EAh	0Ch	Icc Static 1.2mA
ECh	7Dh	Icc Average 90mA
EEh	7Dh	Icc Peak 90mA
F0h	1Bh	Icc Powerdown 150μ A
F2h	79h	Parameter Selection
F4h	B5h	Vpp Voltage 3.3V
F6h	9Eh	
F8h	7Dh	NC OK
FAh	1Bh	Ipp Static 150μ A
FCh	75h	Ipp Average 80mA
FEh	75h	Ipp Peak 80mA
100h	52h	Ipp Powerdown 50μ A
102h	1Bh	Configuration Table Entry 4
104h	10h	Tuple Link
106h	04h	Index
108h	02h	Vcc & Vpp
10Ah	79h	Parameter Selection
10Ch	B5h	Vcc Voltage 3.3V
10Eh	1Eh	
110h	0Ch	Icc Static 1.2mA

Table 8. Standard CIS (Continued)

Address	Value	Description
112h	7Dh	Icc Average 90mA
114h	7Dh	Icc Peak 90mA
116h	1Bh	Icc Powerdown 150μ A
118h	79h	Parameter Selection
11Ah	8Eh	Vpp Voltage 12V
11Ch	7Dh	NC OK
11Eh	1Bh	Ipp Static 150μ A
120h	35h	Ipp Average 30mA
122h	35h	Ipp Peak 30mA
124h	52h	Ipp Powerdown 50μ A
126h	00h	Null
128h	00h	Null
12Ah	1Eh	Device Geometry
12Ch	06h	Tuple Link
12Eh	02h	Bus: 2bytes
130h	11h	Erase Block: 64Kbytes
132h	01h	Read size: 1byte
134h	01h	Write size: 1byte
136h	01h	Partation: 1block
138h	01h	Non-interleaved

Address	Value	Description
13Ah	20h	Manufacturer ID
13Ch	04h	Tuple Link
13Eh	B0h	Manufacturer Code
140h	00h	
142h	06h 07h 09h	Manufacturer Info: 2MB 4MB 8MB
144h	33h	Manufacturer Info: DVO
146h	21h	Function Identification
148h	02h	Tuple Link
14Ah	01h	Function: MEMORY
14Ch	00h	System Init: None
14Eh	FFh	End of CIS

8. Card Control

8. 1 Bus Operations

The host executes read, write and erase operations by issuing the appropriate command to the flash device's Command User Interface (CUI). The CUI serves as the interface between the host processor and internal operation of the flash device. These commands can be issued to the CUI using standard microprocessor bus cycles.

8. 1. 1 Read Array

The host enables reads from the card by writing the appropriate read command to the CUI. The Common Memory devices automatically resets to read array mode upon initial device power-up, or after reset. CE1#, CE2#, and OE# must be logically active to obtain 16 data bits at the outputs. The Card Enables (CE1# and CE2#) are used to select the addressed devices. Output Enable (OE#) is the data input/output (D0–D15) direction control, and when active, drives data from the selected memory onto the data bus. WE# must be driven to V_{IH} during a read access.

8. 1. 2 Output Disable

With OE# at a logic-high level (V_{IH}), the device outputs are disabled. Outputs (D0–D15) are placed in a high-impedance state.

8. 2 Standby

CE1# and CE2# at a logic-high level (V_{IH}) places the card in standby mode. Standby operation disables much of the card's circuitry and substantially reduces device power consumption. The outputs (D0–D15) are placed in a high-impedance state independent of the status of OE#. If the host deselects the card during a write or erase, the card continues to function and consume normal active power until the operation completes.

8. 3 Deep Power-Down

RESET at V_{IH} initiates the deep power-down mode. RESET pin is connected to Vcc with resister 250K (@Vcc=5V). When accesses the card, the system must input low level to RESET.

During reads, an active RESET deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. RESET must be held high for a minimum of 100 ns. After returning from deep power-down, the host must wait before initial memory access outputs are valid, as determined by t_{PHQV}. After this wake-up interval, the host can resume normal operations to the card. Card reset forces the CUI to reset to read array mode and sets the status register to 80H.

8. 4 Reset

The card is in initial state directly after power-up. But we recommend to do reset operation after power-up to make sure to initialize the card.

During block erase, byte write, or lock-bit configuration modes, an active RESET will abort the operation. RDY/BSY# remains low until the reset operation completes. Memory contents being altered are no longer valid; the data may be partially erased or written. The host must wait after RESET goes to logic-Low (V_{IL}) before it can write another command, as determined by t_{PHWL}.

It is important to assert RESET to the card during a system reset. If a CPU reset occurs without a card reset, the host will not be able to read from the card if that card is in a different mode when the system reset occurs.

For example, if an end-user initiates a host reset when the card is in read status register mode, the host will attempt to read code from the card, but will actually read status register data. Sharp's ID242 Series Flash Memory Card allows proper card reset following a system reset through the use of the RESET input.

8. 5 Read Identifier Codes Operation

Manufacture Code and Device Code are contained within each flash memory device in the memory card. The identifier code operation is initiated by writing the Read Identifier Codes command (90h, 9090h) into the CUI of each memory device. The specific address of each device is necessary to be selected to read these codes (Table 9).

Tables 9. Identifier Codes

Code	Address	Data
Manufacture Code	000000h	89h (8989h)
Device Code	000002h	A6h (A6A6h)

(): In word access mode.

Table 8. Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SR.7	SR.6	SR.5	SR.4	SR.3	SR.2	SR.1	SR.0
WSMS	ESS	ECLBS	BWSLBS	VPPS	BWSS	DPS	RFU

SR.7 =WRITE STATE MACHINE STATUS
1 = Ready
0 = Busy

SR.6 =ERASE-SUSPEND STATUS
1 = Erase Suspended
0 = Erase in Progress/Completed

SR.5 =ERASE AND CLEAR LOCK-BITS STATUS
1 = Error In Block Erasure or Clear Lock-Bits
0 = Successful Block Erase or Clear Lock-Bits

SR.4 =BYTE WRITE AND SET LOCK-BIT STATUS
1 = Error in Byte Write or
Set Block/Master Lock-Bit
0 = Successful Byte Write or
Set Block/Master Lock-Bit

SR.3 =VPP STATUS
1 = VPP Low Detect, Operation Abort
0 = VPP OK

SR.2 =BYTE WRITE SUSPEND STATUS
1 = Byte Write Suspended
0 = Byte Write in Progress/Completed

SR.1 =DEVICE PROTECT STATUS
1 = Master Lock-bit,Block Lock-bit and/or
RP# Lock Detected, Operation Abort
0 = Unlock

SR.0 =Reserved for Future Enhancements

Notes:

Chech RDY/BSY# or SR.7 to determine block erase, word/byte write, or lock-bit configuration completion. SR.6-0 are invalid while SR.7="0".

If both SR.5 and SR.4 are "1"s after a block erase or lock-bit configuration attempt, an improper command sequence was entred.

SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Word/Byte Write, Set Block/Master Lock-bit, or Clear Lock-bits command sequences. SR.3 is not guaranteed to reports accurate feedback only when $V_{PP}=V_{PPH1/2/3}$.

SR.1 does not provide a continuous indication of master and block lock-bit values. The WSM interrogates the master lock-bit, block lock-bit, and RP# only after Block Erase, Word/Byte Write, or Lock-bit configuration command sequences. If informs the system, depending on the attempted operation, if the block lock-bit is set, master lock-bit is set, and/or RP# is not 12V. Reading the block lock and master lock configuration codes after writing the Read Identifier Codes commnad indicates master and block lock-bit status.

SR.0 is reserved for future use and should be masked out when polling the status register.

8. 6 Status Register

Each flash memory device in the card has status register. The status register may be read to determine when a write, block erase, or lock-bits configuration is complete, and whether that operation completed successfully (Please refer to Table 10). It may be read at any time by writing the Read Status Register command (70h, 7070h) into the CUI. In word access mode, the status register data of even byte devices are output to D7~0, and the status register data of odd byte devices are output to D15~8.

8. 7 CUI Writes

Flash memory device operations are selected by writing specific commands (Please refer to Section 10) into the Command User Interface (CUI). The contents of the interface register serves as input to the internal state machine on each component.

The CUI itself does not occupy an addressable memory location. The interface register is a latch used to store the command, address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Write Setup command requires both appropriate command data and the address of the location to be written, while the Write command consists of the data to be written and the address of the location to be written.

The CUI is written by bringing WE# to a logic-low level (V_{IL}) while CE# is low. Addresses and data are latched on the rising edge of WE#. Standard microprocessor write timings are used.

When a write or erase command has been issued to the CUI, the internal Write State Machine (WSM) becomes busy and will not be ready until it has completed the operation.

8. 8 Write Protect Switch

The ID242 Series Flash Memory Card has a write protect switch on the back of the card. When the switch is in the write protect position, the card blocks all writes to the common and attribute memory without Card Management Registers region (see Figure 5).

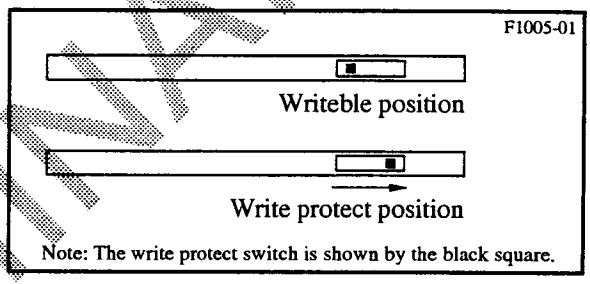


Figure 5. Write Protect Switch

9. Component Management Registers (CMR)

Component Management Registers (CMR) are mapped at even byte locations beginning at address 4000h in attribute memory.

9. 1 Configuration Option Register (Address:4000h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4000h	SRESET	Reserved						
SRESET: 1=Reset State 0=End Reset Cycle								

9. 2 Card Configuration Register (Address:4002h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4002h	Reserved					PWDN	Reserved	
PWDN: 1=Power-Down Device pairs that apointed by Sleep Control Register(4118h-411Ah) are in Power-Down. 0=Power-Up								

9. 3 Socket and Copy Register (Address:4006h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4006h	Reserved	Copy No.			Soket No.			

Soket No.: Socket Number
Copy No.: Copy Number

The card may use to distinguish between similar cards installed in a system.

9. 4 Card Status Register (Address:4100h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4100h	ADM	ADS	SRESET	CMWP	PWDN	CISWP	WP	RDY/BSY

ADM: ORed value of the Ready/Busy Mask Register.
1 = Any device is masked. 0 = All Devices are not Masked.
ADS: ORed value of the Sleep Control Register.
1 = Any device-pair is Controled power-down by bit.2 of the Card Configuration Register.
SRESET: Reflects the bit.7 of the Configuration Option Register.
CMWP: Reflects the bit.1 of the Write Protection Register.
PWDN: Reflects the bit.2 of the Card Configuration Register.
CISWP: Reflects the bit.0 of the Write Protection Register.
WP: Indicates the Write Protect Switch status.
1 = Write Protect Switch: ON 1 = Write Protect Switch: OFF
RDY/BSY: Reflects the Ready/Busy Status Register.
1 = All devices are READY. 0 = Any device is BUSY.

9. 5 Write Protection Register (Address:4104h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4104h	Reserved					BLKEN	CMWP	CISWP

BLKEN: Block Locking Enable
1 = Enable Block Locking 0 = All Blocks Unlocked
CMWP: Common Memory Write Protect
1 = Common Memory without CIS region in Write Protect Status
CISWP: Common Memory CIS Write Protect
1 = Common Memory CIS in Write Protect Status

NOTE: ID242 series ignores BLKEN bit. Block Locking is always enable.

9. 6 Sleep Control Register (Address:4118h~411Ah)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
411Ah	Reserved							
4118h	Reserved		DEV10/11	DEV8/9	DEV6/7	DEV4/5	DEV2/3	DEV0/1

1= Select sleep mode device-pair
If set to "1", the corresponding device-pairs are putted into deep power-down mode by PWDN bit of Configuration Status Register.
Available bits are DEV0/1~DEV6/7 for 8MB, DEV0/1~DEV2/3 for 4MB, DEV0/1 for 2MB.

9. 7 Ready/Busy Mask Register (Address:4120h~4122h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4122h	Reserved				DEV11	DEV10	DEV9	DEV8
4120h	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0

1 =Mask the Rdy/Bsy#
The corresponding device's Rdy/Bsy# signals to set bit are ignored for card's RDY/BSY# output.
Available bits are DEV0~ DEV7 for 8MB, DEV0~ DEV3 for 4MB, DEV0~ DEV1 for 2MB.

9. 8 Ready/Busy Status Register (Address:4130h~4132h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4132h	Reserved				DEV11	DEV10	DEV9	DEV8
4130h	DEV7	DEV6	DEV5	DEV4	DEV3	DEV2	DEV1	DEV0

1=READY 0=BUSY
Each bit indicates the corresponding device's Rdy/Bsy# signal.
Available bits are DEV0~ DEV7 for 8MB, DEV0~ DEV3 for 4MB, DEV0~ DEV1 for 2MB.

9. 9 Ready/Busy Mode Register (Address:4140h)

Address	Bit.7	Bit.6	Bit.5	Bit.4	Bit.3	Bit.2	Bit.1	Bit.0
4140h	Reserved						RACK	MODE

RACK: Ready Acknowledge Bit
Must clear this bit after receiving ready status to prepare for next device's ready transition.
MODE: RDY/BSY# Mode
1 = High-Performance Mode 0 = PCMCIA Mode

10. Command Definitions

Device operations are selected by writing specific commands into the Command User Interface. Table 11 defines the commands.

Table 11. Command Definitions

Command	Note	First Bus Cycle			Second Bus Cycle		
		Operation	Address	Data	Operation	Address	Data
Read Array / Reset		Write	DA	FFh (FFFFh)	-	-	-
Read Identifier Codes	1	Write	DA	90h (9090h)	Read	IA	ID
Read Status Register	2	Write	DA	70h (7070h)	Read	DA	SRD
Clear Status Register		Write	DA	50h (5050h)	-	-	-
Word/Byte Write	3	Write	WA	40h (4040h) or 10h (1010h)	Read	WA	WD
Block Erase	3	Write	BA	20h (2020h)	Write	BA	D0h (D0D0h)
Block Erase and Word/Byte Write Suspend	3	Write	DA	B0h (B0B0h)	-	-	-
Block Erase and Word/Byte Write Resume	3	Write	DA	D0h (D0D0h)	-	-	-
Set Block Lock-Bit		Write	BA	60h (6060h)	Write	BA	01h (0101h)
Set Master Lock-Bit	4	Write	DA	60h (6060h)	Write	DA	F1h (F1F1h)
Clear Block Lock-Bit		Write	DA	60h (6060h)	Write	DA	D0h (D0D0h)

Address

IA =Identifier code Address

WA =Write Address

BA =Block Address

DA =Device Address

Data

ID =Identifier Codes

WD =Write Data

SRD =Data from Status Register

Note:

1. Following the Read Identifier Codes command, read operations access manufacture, device, block lock, and master lock codes.
2. Status Register may be read to determine when a write, block erase, or lock bit configuration is complete, and whether that operation completed successfully.
3. If the block is locked, block erase or write operations are desabled.
4. This command is not available for ID242 series, because the card does not possess the feature suppling 12V to RP# of common memory devices.

10. 1 Read Array Command

Upon initial device power-up and after exit from deep power-down mode, the card defaults to read array mode. The host can also read by writing the Read Array command. The device remains enabled for reads until the host writes another valid command. Once the internal WSM has started a block erase, byte write or lock-bit configuration, the device will not recognize the Read Array command until the WSM completes its operation. However, the host can suspend the WSM using an Erase Suspend or Byte Write Suspend command.

10. 2 Read Identifier Codes Command

The host initiates the identifier code operation by writing the Read Identifier Codes command. Following the command write, read cycles from addresses shown in Table 12 retrieve the manufacturer, device, block lock configuration and master lock configuration codes. To terminate the operation, write another valid command.

Table 12. Identifier Codes

	Select Dvice-pair A25-A21	Address in Device A20-A1	Even/Odd A0	Data Output D7-D0
Manufacture Identifier Code	DPA	00000h	0:Even 1:Odd	89h
Device Identifier Code	DPA	00001h	0:Even 1:Odd	A6h
Block Lock Configuration	DPA	X0002h (X: Select Block)	0:Even 1:Odd	BLKD D0: 0=Unlock 1=Lock D7-D1: Reserved
Master Lock Configuration	DPA	00003h	0:Even 1:Odd	MLKD D0: 0=Unlock 1=Lock D7-D1: Reserved

NOTE: A0 is ignored in word access mode, and D15-D8 outputs the Odd byte data.

DPA: Address as select device pair
BLKD: Block Lock Configuration Data
MLKD: Master Lock Configuration Data

10. 3 Read Status Register Command

The common memory components on this Flash Memory Card each contain a Status Register which may be read to determine when a write, block erase, or lock bit configuration is complete, and whether that operation completed successfully (see Table 8). The host may read the Status Register at any time by writing the Read Status Register command to the CUI. After writing this command, all subsequent read operations output data from the Status Register, until the host writes another valid command to the CUI. The flash components latch the contents of the Status Register on the falling edge of OE# or CE#, whichever occurs first. OE# or CE# must be toggled to V_{IH} before further reads to update the Status Register latch.

NOTE:

Both status registers need to be checked when determining the status of a × 16 erase/write operation.

10. 4 Clear Status Register Command

The WSM sets the Erase Status and Write Status bits to "1"s and they can only be reset by the Clear Status Register command. The WSM sets these bits to "1" when a write or erase operation has failed. The host can issue additional write and erase commands to the CUI without clearing the status register. This allows a system to write a sequence of bytes before checking the write status bit. However, if an error has occurred the system will not know which write in the sequence has failed. To clear the Status Register, the Clear Status Register command (5050H) is written to the CUI.

10. 5 Block Erase Command

The host executes an erase command one block at a time using a two-cycle command. The host writes a block erase setup command first, followed by a block erase confirm command. These two commands require appropriate sequencing and an address within the block to complete (erase changes all block data to FFH). The WSM handles block preconditioning, erase, and verify internally (invisible to the system). After the host writes the two-cycle block erase sequence, the device automatically outputs status register data when read. The CPU can detect block erase completion by analyzing the output data of the RDY/BSY# signal or status register bit SR.7.

When the block erase completes, status register bit SR.5 should be checked. If a block erase error is detected, the host should clear the status register before system software attempts corrective actions. The CUI remains in read status register mode until the host issues a new command.

This two-step command sequence of setup followed by execution ensures that block contents are not accidentally erased. An invalid Block Erase command sequence will result in the WSM setting status register bits SR.4 and SR.5 to "1". Successful block erase requires that the corresponding block lock-bits is not set. If the host attempts a block erase when the corresponding block lock-bit is set, the WSM will set SR.1 and SR.5 to "1".

10. 6 Word/Byte Write Command

The host executes a word write by a two-cycle command sequence. The host writes word write setup (standard 4040H or alternate 1010H) first, followed by a second write that specifies the address and data (latched on the rising edge of WE#). The WSM then takes over, controlling the word write and write verify algorithms internally. After the host writes the word write sequence, the device automatically output status register data when read. The CPU can detect the completion of the byte write event by analyzing the RDY/BSY# pin or status register bit SR.7. When the WSM completes the word writes, the host should check status register bit SR.4. If the host detects a write error, it should clear the status register. The internal WSM verify only detects errors for "1"s that do not successfully writes to "0"s. The CUI remains in read status register mode until it receives another command.

Successful word writes requires that the corresponding block lock-bit is not set. If the host attempts a write when the corresponding block lock-bit is set, the WSM will set SR.1 and SR.4 "1".

10. 7 Block Erase Suspend Command

The Block Erase Suspend command allows block-erase interruption to read or write data in another block of memory. Once the block erase process starts, writing the Block Erase Suspend command requests that the WSM suspend the block erase sequence at a predetermined point in the algorithm. After the host writes the Block Erase

Suspend command, the host should then write the Read Status Register command. Polling status register bits SR.7 and SR.6 can determine when the WSM suspends the block erase operation (both will be set to "1"). RDY/BSY# will also transition to V_{OH} Specification t_{WHRH2} defines the block erase suspend latency. It is also possible that the block erase completes before the device has an opportunity to suspend. The host should also check for this condition.

After the block erase has been suspended, the host can issue a read array command or a word write command to any block except the one that has been suspended. Using the Word Write Suspend command (see Section 8.8), a word write operation can also be suspended. During a word write operation with block erase suspended, status register bit SR.7 will return to "0" and the RDY/BSY# output will transition to V_{OL}. However, SR.6 will remain "1" to indicate block erase suspend status. The only other valid commands while block erase is suspended are Read Status Register and Block Erase Resume. After the host writes a Block Erase Resume command to the flash memory, the WSM will continue the block erase process. Status register bits SR.6 and SR.7 will automatically clear and RDY/BSY# will return to V_{OL}. After the host writes the Erase Resume command, the device automatically outputs status register data when read. Block erase cannot resume until word write operation initiated during block erase suspend have completed.

10. 8 Word/Byte Write Suspend Command

The Word Write Suspend command allows word write interruption to read data in other flash memory locations. Once the word write process starts, writing the Word Write Suspend command requests that the WSM suspend the word write sequence at a predetermined point in the algorithm. After the host writes the Word Write Suspend command, it should write the Read Status Register command. Polling status register bits SR.7 and SR.2 can determine when the WSM suspends the byte write operation (both will be set to "1"). RDY/BSY# will also transition to V_{OH}. Specification t_{WHRH1} defines the word write suspend latency. It is also possible that the word write completes before the device has an opportunity to suspend. The host should also check for this condition.

After the word write has been suspended, the host can write the Read Array command to read data from any location except the suspended location. The only other valid commands while word write is suspended are Read Status Register and Word Write Resume. After the host writes a Word Write Resume to the CUI, the WSM will continue the word write process. Status register bits SR.2 and SR.7 will automatically clear and RDY/BSY# will return to V_{OL}. After the host writes the Word Write Resume command, the device automatically outputs status register data when read.

10. 9 Set Block Lock-Bit Command

The host can enable a flexible block locking and unlocking scheme using the Set Block Lock-Bit command. This command enables the host to lock individual blocks within the flash array. The block lock-bits gate program and erase operations.

The host sets the block lock-bit using a two-cycle command sequence. The host writes the set block lock-bit setup command along with the appropriate block or device address. This command is followed by the set block lock-bit confirm command (and an address within the block to be locked). The WSM controls the set lock-bit algorithm. After the host completes the command sequence, the card automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing the RDY/BSY# pin output or status

register bit SR.7.

When the WSM completes the set lock-bit operation, the host should check status register bit SR.4. If the host detects an error it should clear the status register. The CUI will remain in read status register mode until the host issues a new command.

This two-step sequence of setup followed by execution ensures that the host does not accidentally set the lock-bits. An invalid Set Block Lock-Bit command will result in the WSM setting status register bits SR.4 and SR.5 to "1".

10. 10 Set Master Lock-Bit Command

A successful set block lock-bit operation of the memory card requires that the master lock-bit be cleared or, if the master lock-bit is set, that RP# of common memory device is Vcc. RP# of common memory device can only accept Vcc or be connected to GND. The RP# will not accept 12V. If it is attempted with the master lock-bit set and RP#=12V, SR.1 and SR.4 will be set to "1" and operation will fail.

10. 11 Clear Block Lock-Bits Command

The host clears all set block lock-bits in parallel using the Clear Block Lock-Bits command. The host is free to clear block lock-bits using the Clear Block Lock-Bits command.

The host executes the clear block lock-bits operation using a two-cycle command sequence. The host must first issue a Clear Block Lock-Bits setup command. This command is followed by a confirm command. After the host completes the two-cycle command sequence, the device automatically outputs status register data when read. The CPU can detect completion of the clear block lock-bits event by analyzing the RDY/BSY# pin output or status register bit SR.7.

When the WSM completes the operation, the host should check status register bit SR.5. If the host detects a clear block lock-bit error, the host should clear the status register. The CUI will remain in read status register mode until the host issues another command.

This two-step sequence of setup followed by execution ensures that the host does not accidentally clear block lock-bits. An invalid Clear Block Lock-Bits command sequence will result in the WSM setting status register bits SR.4 and SR.5 to "1".

If a clear block lock-bits operation is aborted due to V_{CC} transitioning out of valid range or RESET active transition, block lock-bit values are left in an undetermined state. The host must repeat the clear block lock-bits command to initialize block lock-bit contents to known values.

10. 12Automated Word Write Flowchart

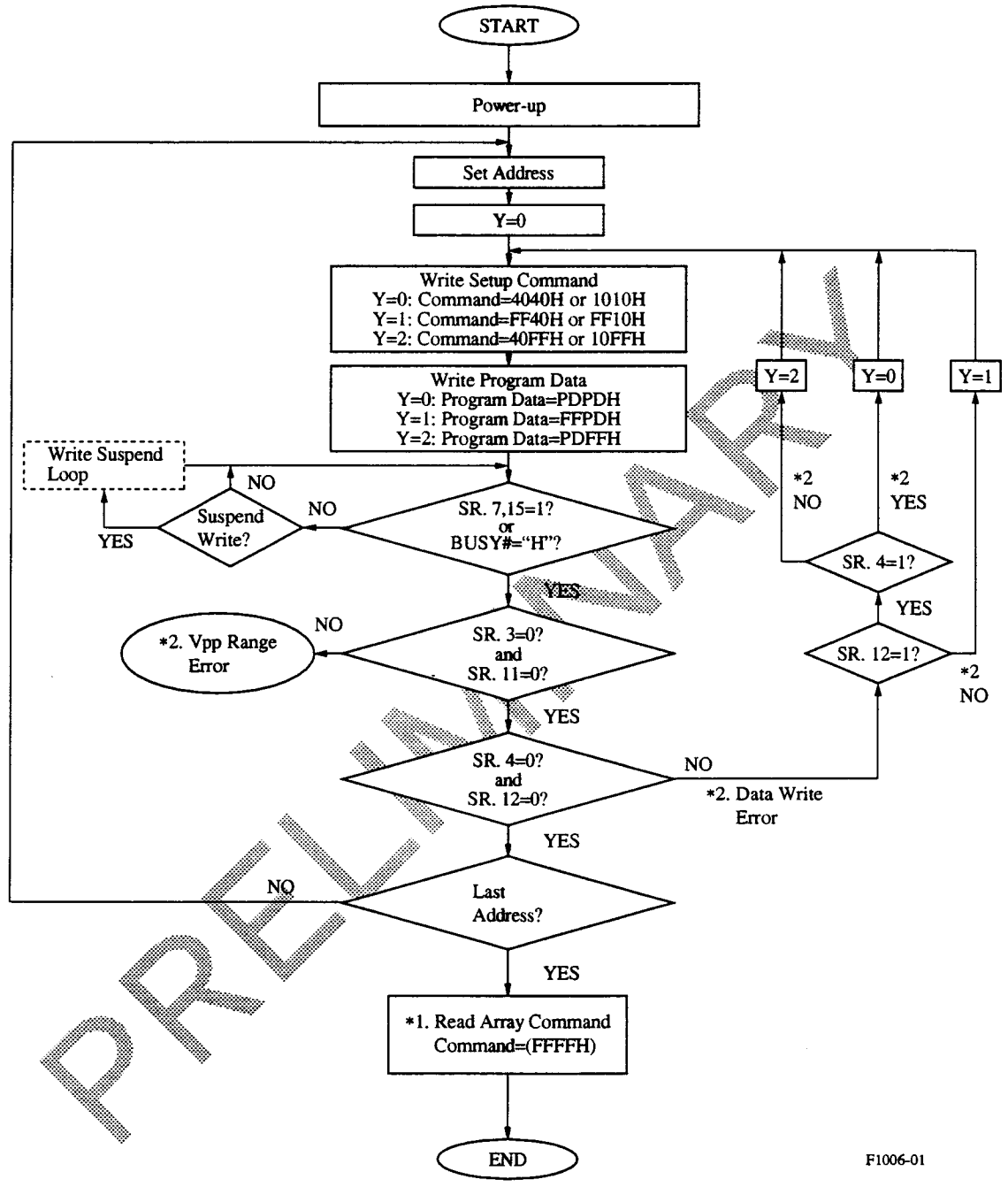


Figure 6. Automated Word Write Flowchart

Note) *1. Write FFFFH after the last word write operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

10. 13Automated Block Erase Flowchart

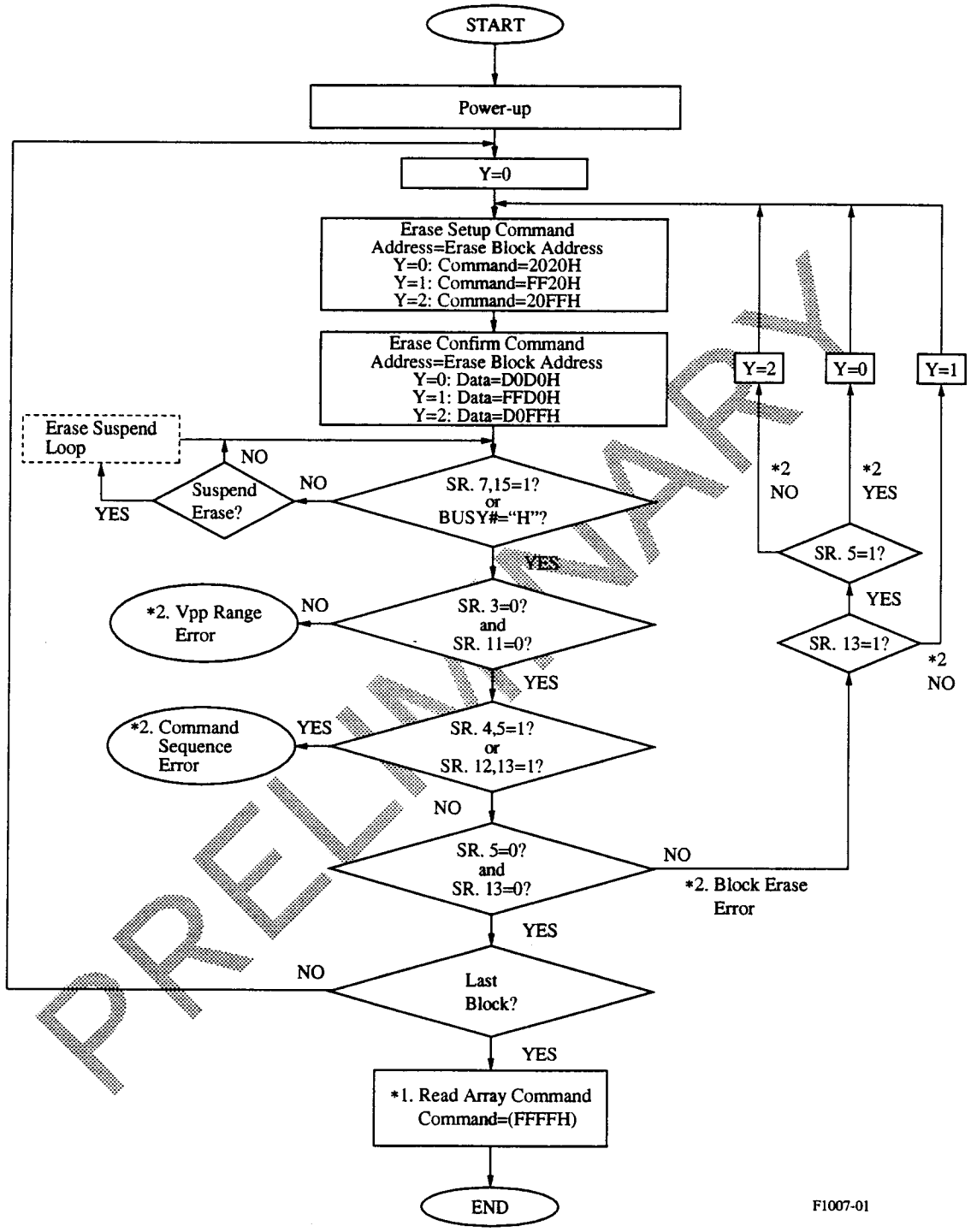


Figure 7. Automated Block Erase Flowchart

Note) *1. Write FFFFH after the last block erase operation to reset the device to Read Array Mode.

*2. If error is detected, clear the Status Register before attempting retry or other error recovery.

11. Electrical Specifications

11. 1 Absolute Maximum Ratings

PARAMETER	NOTE	SYMBOL	RATING	UNIT
Supply Voltage	2	V_{CC}	-0.3 to 6.0	V
Program Voltage	2	V_{PP}	-2.0 to 14.0	V
Input Voltage	2	V_{IN}	-0.3 to Vcc+0.3(Max:6.0)	V
Operating Temperature	1	T_{OPR}	0 to 60	℃
Storage Temperature		T_{STG}	-20 to 65	℃

NOTES:
1. Operating temperature is for commercial product defined by this specification.
2. All specified voltages are with respect to GND. During transitions, this level may undershoot to -2.0v for periods <20ns or overshoot to Vcc+2.0v for periods <20ns.

11. 2 Recommended Operating Conditions

PARAMETER	NOTE	SYMBOL	MIN	MAX	UNIT
Supply Voltage		V_{CC1}	3.0	3.6	V
		V_{CC2}	4.75	5.25	V
		V_{CC3}	4.5	5.5	V
Program Voltage		V_{PP1}	3.0	3.6	V
		V_{PP2}	4.5	5.5	V
		V_{PP3}	11.4	12.6	V
Operating Temperature		T_{OPR}	0	60	℃

11. 3 Capacitance

Ta=25℃, f=1MHz

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Capacitance	C_{IN}	-	15	-	pF	V_{IN}=0.0V
Input/Output Capacitance	C_{IO}	-	25	-	pF	V_{OUT}=0.0V

11. 4 AC Input/Output Test Conditions

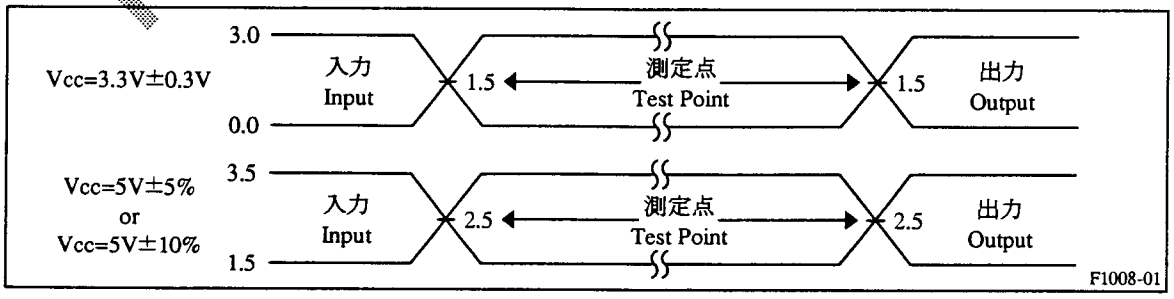


Figure 8. Transient Input/Output Reference Waveform

Figure 8 shows Input/Output level and test level for AC test. Input rise and fall times (10% to 90%) < 10ns.

12. DC Characteristics

(Ta = 0 to 60℃)

PARAMETER	SYM-BOL	NO-TE	Densi-ty	Vcc=3.3V±0.3V		Vcc=5V±5% Vcc=5V±10%		UNIT	TEST CONDITION
				MIN	MAX	MIN	MAX		
Input Low Voltage	V_{IL}	1			0.3Vcc		1.5	V	
Input High Voltage	V_{IH}	1		0.7Vcc		3.5		V	
Input Low Current	$-I_{IL1}$	2			± 2.0		± 2.0	μA	V_I = 0V
	$-I_{IL2}$	3		2.0	30.0	8.0	60.0	μA	V_I = 0V
Input High Current	I_{IH1}	3			± 2.0		± 2.0	μA	V_I = Vcc
	I_{IH2}	2		2.0	30.0	8.0	60.0	μA	V_I = Vcc
Output Low Voltage	V_{OL1}	4,5			-		0.4	V	I_{OL} = 6mA
					0.4		-	V	I_{OL} = 3mA
Output High Voltage	V_{OH1}	4		-		4.0		V	I_{OH} = -3mA
				Vcc-0.5		-		V	I_{OH} = -1.5mA
	V_{OH2}	5		-		4.0		V	I_{OH} = -6mA
				Vcc-0.5		-		V	I_{OH} = -3mA
Vcc Stand-by Current	I_{CCS}	6	2MB		240		240	μA	CE_1#,CE_2#=Vcc A_0~A_{25}=GND I_{OUT}=0mA
			4MB		450		450	μA	
			8MB		850		850	μA	
Vcc Deep Power-Down Current	I_{CCD}	6	2MB		45		75	μA	RESET=Vcc CE_1#,CE_2#=Vcc A_0~A_{25}=GND I_{OUT}=0mA
			4MB		70		110	μA	
			8MB		150		200	μA	
Vcc Read Current	I_{CCR}	6,8			90		100	mA	CE_1#,CE_2#=GND I_{OUT}=0mA
Vcc Word Write or Set Lock-Bit Current	I_{CCW}	6,9			35		-	mA	V_{PP}=3.3V± 0.3V
					35		75	mA	V_{PP}=5.0V± 10%
					25		65	mA	V_{PP}=12.0V± 5%
Vcc Block Erase or Clear Lock-Bit Current	I_{CCE}	6,9			35		-	mA	V_{PP}=3.3V± 0.3V
					35		65	mA	V_{PP}=5.0V± 10%
					25		55	mA	V_{PP}=12.0V± 5%
VccWord Write or Block Erase Suspend Current	I_{CCWS} I_{CCES}	6			13		21	mA	
Vcc Lockout Voltage	V_{LKO}			2.0		2.0		V	

(Continue to next page)

DC Characteristics (Continued) (Ta = 0 to 60℃)

PARAMETER	SYM-BOL	NO-TE	Densi-ty	Vcc=3.3V±0.3V		Vcc=5V±5% Vcc=5V±10%		UNIT	TEST CONDITION
				MIN	MAX	MIN	MAX		
V_{PP} Stand-by or Read Current	I_{PPS} I_{PPR}	6	2MB		± 30		± 30	μ A	$V_{PP} \leqq$ Vcc
			4MB		± 60		± 60	μ A	
			8MB		± 150		± 150	μ A	
			2MB		0.4		0.4	mA	V_{PP}>Vcc
			4MB		0.8		0.8	mA	
			8MB		1.6		1.6	mA	
V_{PP} Deep Power-Down Current	I_{PPD}	6	2MB		10		10	μ A	
			4MB		20		20	μ A	
			8MB		50		50	μ A	
V_{PP} Word Write or Set Lock-Bit Current	I_{PPW}	6,9			80		-	mA	V_{PP}=3.3V± 0.3V
					80		80	mA	V_{PP}=5.0V± 10%
					32		32	mA	V_{PP}=12.0V± 5%
V_{PP} Block Erase or Clear Lock-Bit Current	I_{PPE}	6,9			40		-	mA	V_{PP}=3.3V± 0.3V
					40		40	mA	V_{PP}=5.0V± 10%
					32		32	mA	V_{PP}=12.0V± 5%
V_{PP} Word Write or Block Erase Suspend Current	I_{PPWS} I_{PPES}	6	2MB		400		400	μ A	$V_{PP} \leqq$ Vcc
			4MB		430		430	μ A	
			8MB		500		500	μ A	
			2MB		0.4		0.4	mA	V_{PP}>Vcc
			4MB		0.8		0.8	mA	
			8MB		1.6		1.6	mA	
V_{PP} Lockout Voltage	V_{PPLK}	7,9			1.5		1.5	V	

NOTE:

1. These parameters are applied to all input pins and all i/put/output pins in input mode.
2. These parameters are applied to A_0~A_{25} and D_0~D_{15} in input mode.
3. These parameters are applied to CE_1#,CE_2#,WE#,OE#,REG# and RESET.
4. These parameters are applied to RDY/BSY#.
5. These parameters are applied to D_0~D_{15} in output mode.
6. All currents are in RMS unless otherwise notes.
7. Block erase, word/byte write, and lock-bit configurations are inhibited when $V_{PP} \leqq V_{PPLK}$, and guaranteed in the V_{PP} Voltage is V_{PP1}, V_{PP2} or V_{PP3}.
8. Automatic Power Savings(APS) reduces typical I_{CCR} to 30mA at Vcc=5V and 20mA at Vcc=3.3V in static operation.
9. Sampled.

13. AC Characteristics

Testing Conditions :

1) Input Pulse Level : 1.5 to 3.5V (@Vcc=5V±5%,Vcc=5V±10%)
   0 to 3.0V (@Vcc=3.3±0.3V)
2) Input Rise/Fall Time : 10ns
3) Input/Output Timing Reference Level : 2.5V (@Vcc=5V±5%,Vcc=5V±10%)
   1.5V (@Vcc=3.3V±0.3V)
4) Output Load : 1TTL+100pF (@Vcc=5V±5%,Vcc=5V±10%)
   (including scope and jig capacitance) 1TTL+50pF (@Vcc=3.3V±0.3V)

13. 1 Common and Attribute Memory Read Operations

(Ta = 0 to 60℃)

PARAMETER	SYMBOL		Vcc=3.3V±0.3V		Vcc=5V±5%		Vcc=5V±10%		Unit
	IEEE	JEIDA/ PCMCIA	MIN	MAX	MIN	MAX	MIN	MAX	
Read Cycle Time	t_{AVAV}	t_{cR}	250	-	150	-	160	-	ns
Address Access Time	t_{AVQV}	t_a(A)	-	250	-	150	-	160	
CE# Access Time	t_{ELQV}	t_a(CE)	-	250	-	150	-	160	
OE# Access Time	t_{GLQV}	t_a(OE)	-	125	-	75	-	80	
Output Disable Time from CE1#,CE2# *	t_{EHQZ}	t_{dis}(CE)	-	100	-	75	-	80	
Output Disable Time from OE# *	t_{GHQZ}	t_{dis}(OE)	-	100	-	75	-	80	
Output Enable Time from CE1#,CE2#	t_{ELQNZ}	t_{en}(CE)	5	-	5	-	5	-	
Output Enable Time from OE#	t_{GLQNZ}	t_{en}(OE)	5	-	5	-	5	-	
Data Valid Time from Address Change		t_v(A)	0	-	0	-	0	-	
RESET Recovery Time to Output Delay	t_{PHQV}		-	700	-	450	-	450	

*:Time until output becomes floating. (The output voltage is not defined.)

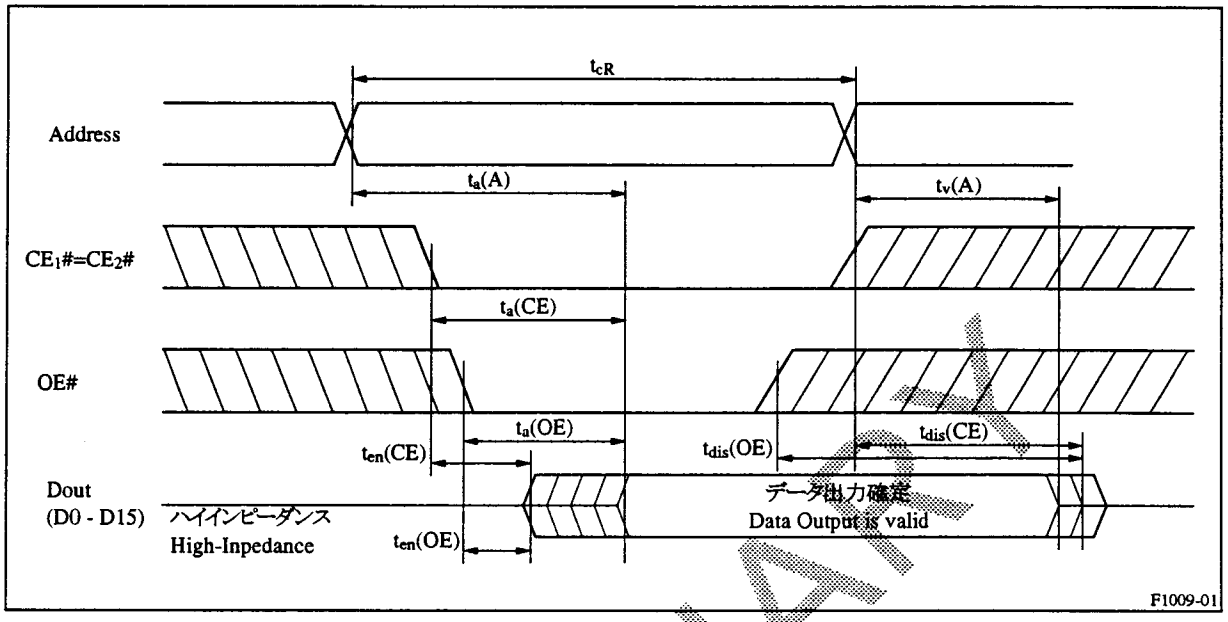


Figure 9. AC Waveforms for Read Operations

Note) 1. WE# = "HIGH", during a read cycle.

2. Either "HIGH" or "LOW" in diagonal areas.

3. The output data becomes valid when last interval, ta (A), ta (CE) or ta (OE) have concluded.

13. 2 Command Write Operations : Common Memory

13. 2. 1 WE# Controlled Write Operations

(Vcc=3.3V±0.3V, Ta=0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=3.3V±0.3V		Unit
	IEEE	PCMCIA		MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		250	-	ns
Address Setup Time	t_{AVWL}	t_{su}(A)		30	-	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)		30	-	ns
Data Setup Time for WE#	t_{DVWH}	t_{su}(D-WEH)		80	-	ns
Data Hold Time	t_{WHDX}	t_h(D)		30	-	ns
OE# Hold Time from WE#	t_{WHGL}	t_h(OE-WE)		120	-	ns
CE# Setup Time for WE#	t_{ELWH}	t_{su}(CE-WEH)		180	-	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)		180	-	ns
Write Pulse Width	t_{WLWH}	t_w(WE)		150	-	ns
WE# High to RDY/BSY# going Low	t_{WHRL}			-	140	ns
RESET Recovery Time	t_{PHWL}			1	—	μs
V_{PP} Setup Time	t_{VPWH}			180	—	ns
V_{PP} Hold Time	t_{QVVL}			0	—	ns
Word/Byte Write Time	t_{WHQV1}		V_{PP}=3.3V±0.3V	15	—	μs
			V_{PP}=5V±10%	8.2	—	μs
			V_{PP}=12V±5%	6.7	—	μs
Block Erase Time	t_{WHQV2}		V_{PP}=3.3V±0.3V	1.5	—	s
			V_{PP}=5V±10%	1.0	—	s
			V_{PP}=12V±5%	0.8	—	s
Set Lock-Bit Time	t_{WHQV3}		V_{PP}=3.3V±0.3V	18	—	μs
			V_{PP}=5V±10%	11.2	—	μs
			V_{PP}=12V±5%	9.7	—	μs
Clear Block Lock-Bits Time	t_{WHQV4}		V_{PP}=3.3V±0.3V	1.5	—	s
			V_{PP}=5V±10%	1.0	—	s
			V_{PP}=12V±5%	0.8	—	s

(Vcc=5V±5%, Vcc=5V±10%,, Ta = 0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=5V±5%		Vcc=5V±10%		Unit
	IEEE	PCMCIA		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		150	-	150	-	ns
Address Setup Time	t_{AVWL}	t_{su}(A)		20	-	20	-	ns
Write Recovery Time	t_{WHAX}	t_{rec}(WE)		20	-	20	-	ns
Data Setup Time for WE#	t_{DVWH}	t_{su}(D-WEH)		50	-	50	-	ns
Data Hold Time	t_{WHDX}	t_h(D)		20	-	20	-	ns
OE# Hold Time from WE#	t_{WHGL}	t_h(OE-WE)		80	-	80	-	ns
CE# Setup Time for WE#	t_{ELWH}	t_{su}(CE-WEH)		100	-	100	-	ns
Address Setup Time for WE#	t_{AVWH}	t_{su}(A-WEH)		100	-	100	-	ns
Write Pulse Width	t_{WLWH}	t_w(WE)		80	-	80	-	ns
WE# High to RDY/BSY# going Low	t_{WHRL}			-	140	-	140	ns
RESET Recovery Time	t_{PHWL}			1	-	1	-	μs
V_{PP} Setup Time	t_{VPWH}			100	-	100	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	0	-	ns
Word/Byte Write Time	t_{WHQV1}		V_{PP}=5V±10%	6.5	-	6.5	-	μs
			V_{PP}=12V±5%	4.8	-	4.8	-	μs
Block Erase Time	t_{WHQV2}		V_{PP}=5V±10%	0.9	-	0.9	-	s
			V_{PP}=12V±5%	0.3	-	0.3	-	s
Set Lock-Bit Time	t_{WHQV3}		V_{PP}=5V±10%	9.5	-	9.5	-	μs
			V_{PP}=12V±5%	7.8	-	7.8	-	μs
Clear Block Lock-Bits Time	t_{WHQV4}		V_{PP}=5V±10%	0.9	-	0.9	-	s
			V_{PP}=12V±5%	0.3	-	0.3	-	s

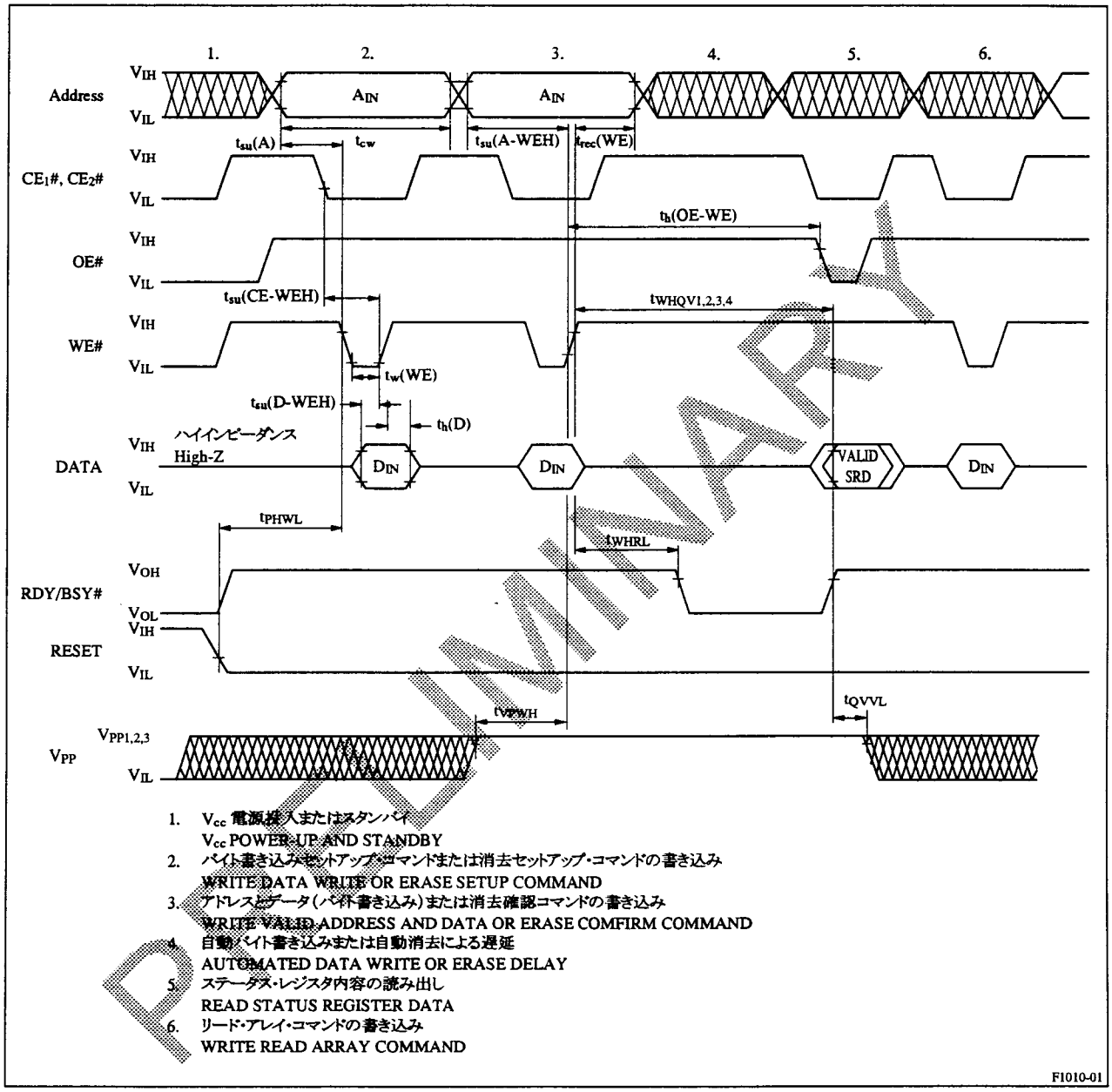


Figure 10. AC Waveforms for Write Operations (WE# Controlled)

Note) While the data signal is in output mode, do not apply an opposite phase input signal.

13. 2. 2 CE# Controlled Write Operations

(Vcc=3.3V±0.3V, Ta = 0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=3.3V±0.3V		Unit
	IEEE	PCMCIA		MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		250	-	ns
Address Setup Time	t_{AVEL}	t_{su}(A)		30	-	ns
Write Recovery Time	t_{EHAX}	t_{rec}(CE)		30	-	ns
Data Setup Time for CE#	t_{DVEH}	t_{su}(D-CEH)		60	-	ns
Data Hold Time	t_{EHDX}	t_{h}(D)		30	-	ns
OE# Hold Time from CE#	t_{EHGL}	t_{h}(OE-CE)		120	-	ns
WE# Setup Time for CE#	t_{WLEH}	t_{su}(WE-CEH)		180	-	ns
Address Setup Time for CE#	t_{AVEH}	t_{su}(A-CEH)		180	-	ns
Write Pulse Width	t_{ELEH}	t_{w}(CE)		150	-	ns
CE# High to RDY/BSY# going Low	t_{EHRL}			-	140	ns
RESET Recovery Time	t_{PHEL}			1	-	μs
V_{PP} Setup Time	t_{VPEH}			180	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	ns
Word/Byte Write Time	t_{EHQV1}		V_{PP}=3.3V±0.3V	15	-	μs
			V_{PP}=5V±10%	8.2	-	μs
			V_{PP}=12V±5%	6.7	-	μs
Block Erase Time	t_{EHQV2}		V_{PP}=3.3V±0.3V	1.5	-	s
			V_{PP}=5V±10%	1.0	-	s
			V_{PP}=12V±5%	0.8	-	s
Set Lock-Bit Time	t_{EHQV3}		V_{PP}=3.3V±0.3V	18	-	μs
			V_{PP}=5V±10%	11.2	-	μs
			V_{PP}=12V±5%	9.7	-	μs
Clear Block Lock-Bits Time	t_{EHQV4}		V_{PP}=3.3V±0.3V	1.5	-	s
			V_{PP}=5V±10%	1.0	-	s
			V_{PP}=12V±5%	0.8	-	s

(Vcc=5V±5%, Vcc=5V±10%, Ta=0 to 60℃)

PARAMETER	SYMBOL		CONDITION	Vcc=5V±5%		Vcc=5V±10%		Unit
	IEEE	PCMCIA		MIN	MAX	MIN	MAX	
Write Cycle Time	t_{AVAV}	t_{cW}		150	-	150	-	ns
Address Setup Time	t_{AVEL}	t_{su}(A)		20	-	20	-	ns
Write Recovery Time	t_{EHAX}	t_{rec}(CE)		20	-	20	-	ns
Data Setup Time for CE#	t_{DVEH}	t_{su}(D-CEH)		50	-	50	-	ns
Data Hold Time	t_{EHDX}	t_{h}(D)		20	-	20	-	ns
OE# Hold Time from CE#	t_{EHGL}	t_{h}(OE-CE)		80	-	80	-	ns
WE# Setup Time for CE#	t_{WLEH}	t_{su}(WE-CEH)		100	-	100	-	ns
Address Setup Time for CE#	t_{AVEH}	t_{su}(A-CEH)		100	-	100	-	ns
Write Pulse Width	t_{ELEH}	t_{w}(CE)		80	-	80	-	ns
CE# High to RDY/BSY# going Low	t_{EHRL}			-	140	-	140	ns
RESET Recovery Time	t_{PHEL}			1	-	1	-	μs
V_{PP} Setup Time	t_{VPEH}			100	-	100	-	ns
V_{PP} Hold Time	t_{QVVL}			0	-	0	-	ns
Word/Byte Write Time	t_{EHQV1}		V_{PP}=5V±10%	6.5	-	6.5	-	μs
			V_{PP}=12V±5%	4.8	-	4.8	-	μs
Block Erase Time	t_{EHQV2}		V_{PP}=5V±10%	0.9	-	0.9	-	s
			V_{PP}=12V±5%	0.3	-	0.3	-	s
Set Lock-Bit Time	t_{EHQV3}		V_{PP}=5V±10%	9.5	-	9.5	-	μs
			V_{PP}=12V±5%	7.8	-	7.8	-	μs
Clear Block Lock-Bits Time	t_{EHQV4}		V_{PP}=5V±10%	0.9	-	0.9	-	s
			V_{PP}=12V±5%	0.3	-	0.3	-	s

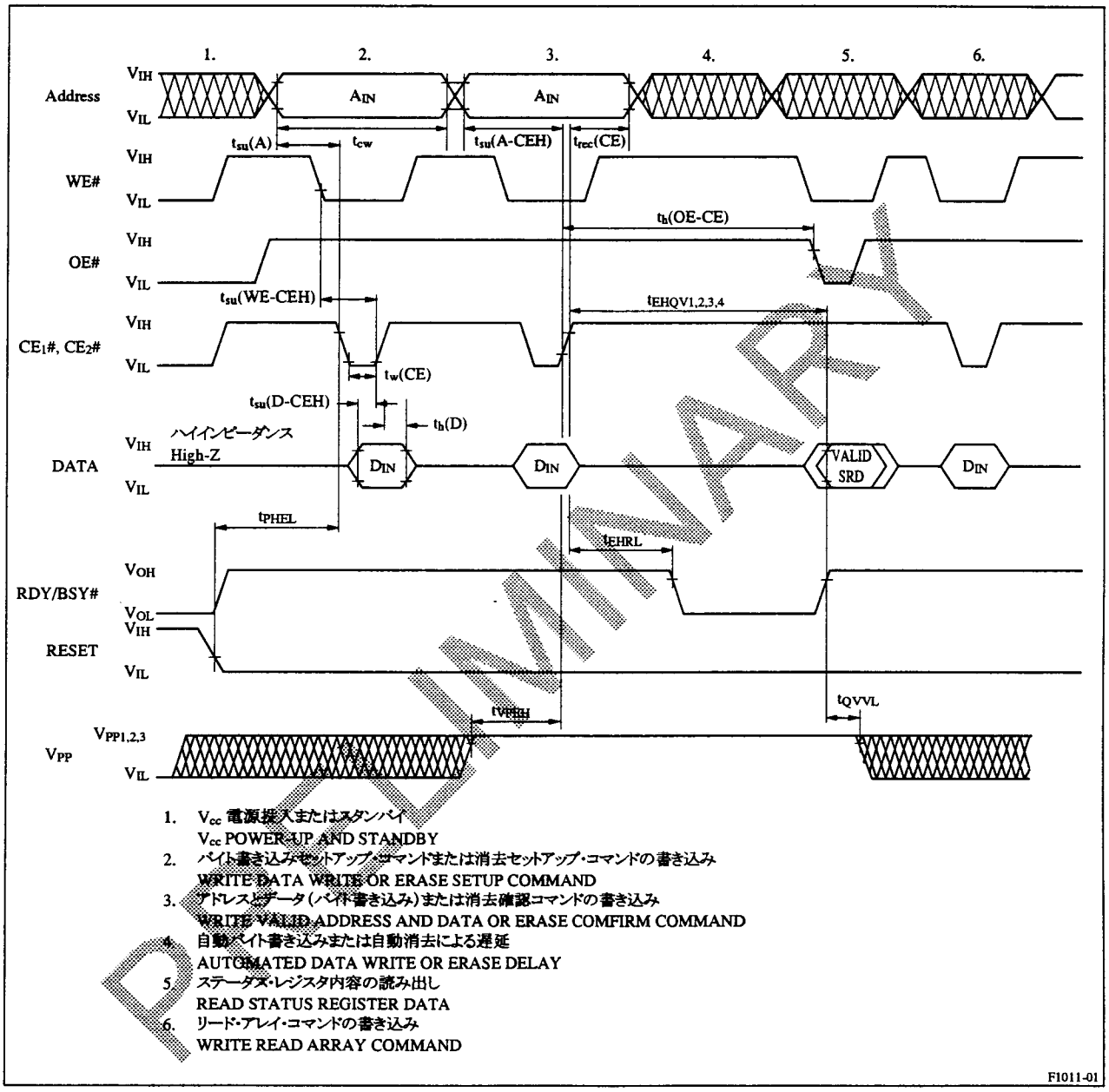


Figure 11. AC Waveforms for Write Operations (CE# Controlled)

Note) While the data signal is in output mode, do not apply an opposite phase input signal.

13. 3 Power-Up/Power Down

PARAMETER	SYMBOL PCMCIA	NOTES	MIN	MAX	UNITS
CE# Signal Level (0.0V < V_{CC} < 2.0V)	V_i (CE)	1	0	V_{iMAX}	V
CE# Signal Level (2.0V < V_{CC} < V_{IH})		1	V_{CC}–0.1	V_{iMAX}	V
CE# Signal Level (V_{IH} < V_{CC})		1	V_{IH}	V_{iMAX}	V
CE# Setup Time	t_{su} (V_{CC})	—	20	—	ms
RESET Setup Time	t_{su} (RESET)	—	20	—	ms
CE# Recover Time	t_{rec} (V_{CC})	—	1.0	—	µs
V_{CC} Rising Time	t_{pr}	2	0.1	300	ms
V_{CC} Falling Time	t_{pf}	2	3.0	300	ms
RESET Width	t_w (RESET)	—	10	—	µs
RESET Width	t_h (Hi–Z RESET)	—	1	—	ms
RESET Width	t_s (Hi–Z RESET)	—	0	—	ms

NOTES:

1. V_{iMAX} means Absolute Maximum Voltage for input in the period of 0.0V < V_{CC} < 2.0 V, Vi (CE#) is only 0.00V-V_{iMAX}
2. The t_{pr} and t_{pf} are defined as "linear waveforms" in the period of 10% to 90%, or vice-versa. Even if the waveform is not a "liner waveform," its rising and falling time must meet this specification.

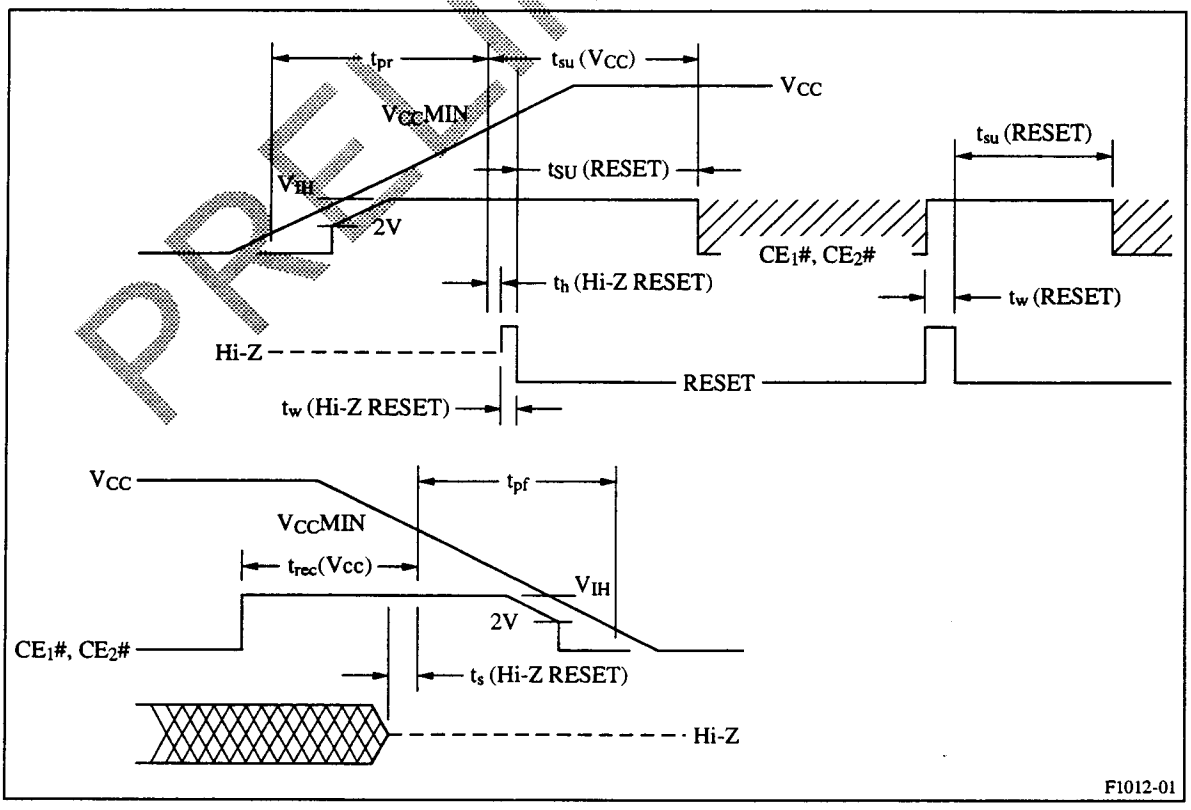


Figure 12. Power-Up/Down Timing

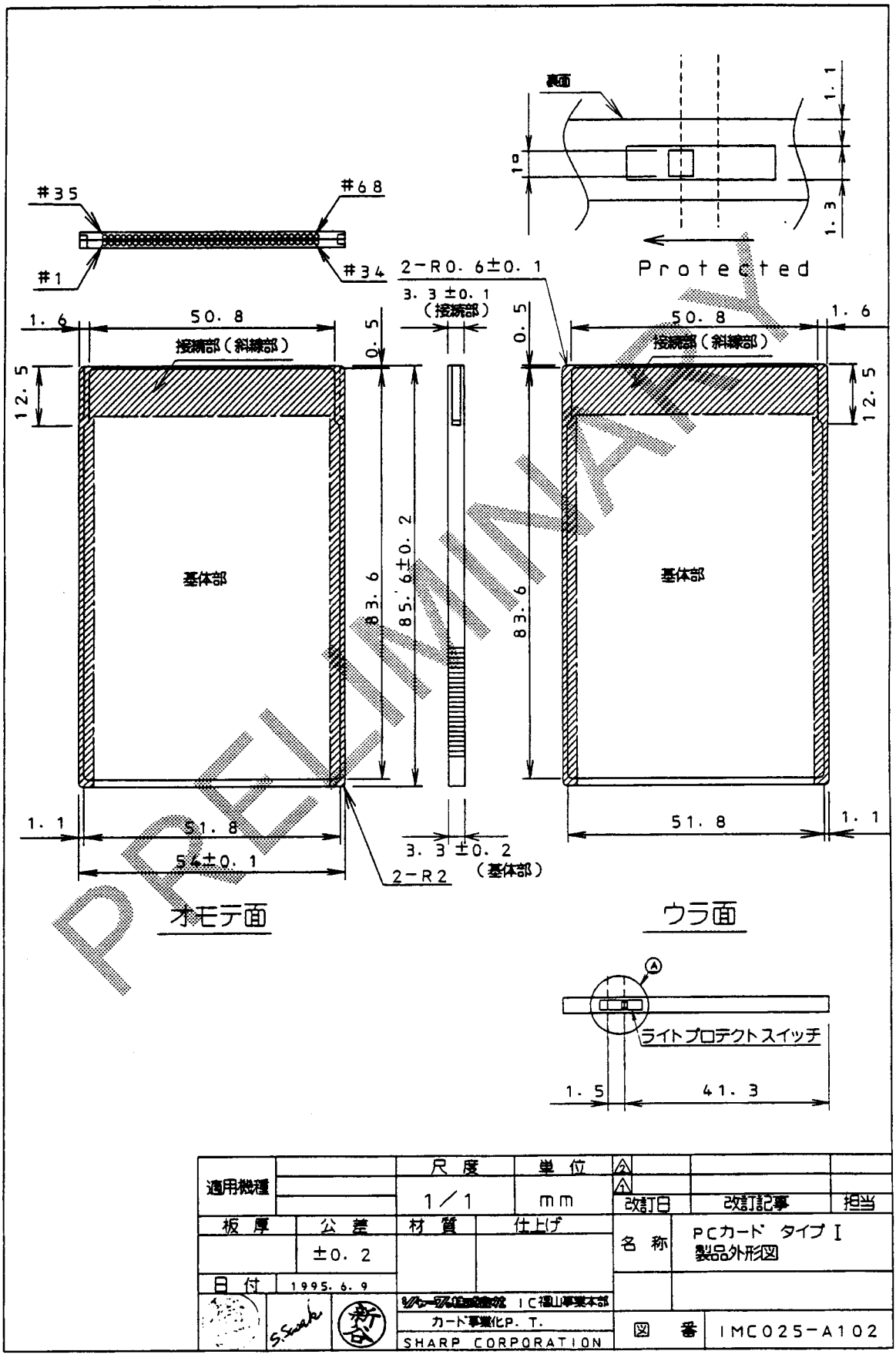
14. Specification Changes

This datasheet is for ID242 series product overview, and final specifications will be submitted for qualification of the memory card. Please note that contents of this datasheet may be revised without announcement beforehand. Please do NOT finalize a system design with this information.

15. Other Precautions

- Permanent damage occurs if the memory card is stressed beyond Absolute Maximum Ratings. Operation beyond the Recommended Operating Conditions is not recommended and extended exposure beyond the Recommended Operating Conditions may affect device reliability.
- Writing to the memory card can be prevented by switching on the write protect switch on the end of the memory card.
- Avoid allowing the memory card connectors to come in contact with metals and avoid touching the connectors, as the internal circuits can be damaged by static electricity.
- Avoid storing in direct sunlight, high temperatures (do not place near heaters or radiators), high humidity and dusty areas.
- Avoid subjecting the memory card to strong physical abuse. Dropping, bending, smashing or throwing the card can result in loss of function.
- When the memory card is not being used, return it to its protective case.
- Do not allow the memory card to come in contact with fire.

16. External Diagrams



適用機種		尺度	単位	△			
		1／1	mm	△	改訂日	改訂記事	担当
板厚	公差	材質	仕上げ	名称	PCカード タイプI 製品外形図		
	±0.2						
日付	1995.6.9						
S.Suzuki	新合	シャープ株式会社 IC福山事業本部 カード事業化P.T. SHARP CORPORATION		図番	IMC025-A102		

Flash Card, Series 2, Intel Compatible, Linear PCMCIA Memory