SIEMENS

HYB 514171BJ/BJL -50/-60/-70
256k x 16 - Bit Dynamic RAM

INFORMATION NOTE

256kx16 BYTEWIDE DYNAMIC MEMORIES
(Hypershrink Version)

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6.95
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This information note is intended to provide technical information on the SIEMENS 256kx16 DYNAMIC ACCESS MEMORY HYB51471BJ/BJL.

GENERAL INFORMATION

The SIEMENS HYB 514171BJ/BJL is a fourth generation 4 megabit dynamic RAM organised 262144 words by 16 bit assembled in 400 mil wide industry standard SOJ 40 packages. The word-wide chip design features fast page mode, two addressing schemes , a symmetrical addressing with 512 refresh cycles and an asymmetrical addressing with 1024 refresh cycles and the possibility to individually select the upper or lower byte either by two CAS or two WE input lines. A low power version with extended & self refresh option is also available. Additional hyper page mode versions (EDO) will be introduced later this year.

The HYB 514171BJ/BJL utilised the SIEMENS submicron twin-well CMOS silicon gate 4M-process technology with depletion type trench capacitors and ONO dielectric as well as advanced circuit techniques to provide wide operation margins , both internally and to the system user.

Table 1 & 2 highlight the process and design related data.

JEDEC STANDARDISATION

CAS OR WRITE (WE) CONTROL

JEDEC has standardised different versions of CAS and/or WE control for 256k x 16 DRAMs to individual select the lower and upper byte of the 16 data lines.

Version 1	1 CAS	1 WE	
Version 2	2 CAS	1 WE	preferred version
Version 3	1 CAS	2 WE	
Version 4	2 CAS	2 WE	

The SIEMENS 256kx16 chip design has incorporated all different versions of CAS and WE control, standardised by JEDEC. Each version can be selected via bonding options during the assembly process.

Controllers exist that support either version so choosing one of the above versions depends on the controller which is used. Since most of the applications using 256k x 16 DRAMs are upgraded from 256kx4 DRAMs the dual CAS-Version with one write enable signal (WE) is preferred by most users. The dual CAS allows the user to do byte reads or byte writes, whereas the dual WE-version does not have the capability to perform byte reads. Therefore the 2CAS / 1WE version runs in production.

The SIEMENS partnumber for this version is HYB 514171BJ/BJL and has the following pin-out and top-side marking (fig.1) :

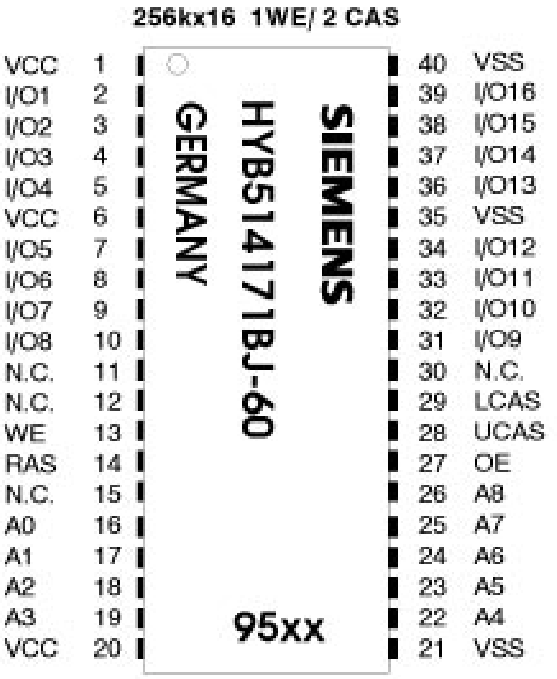


fig.1

SYMMETRICAL or ASYMMETRICAL ADDRESSING

In the past, the addressing of DRAMs has been simple. The number of row-address lines was equal to the number of column-address lines. This is known as "symmetrical addressing". For the x 16 devices, JEDEC has approved a slightly different type of addressing called "asymmetrical", in addition to the standard symmetrical version. Asymmetrical addressing has more row-address lines than column-address lines. With the increased number of row and decreased number of columns, there is a potential for power savings at the chip level (one-half the number of sense amplifiers are activated in any cycle).

A 256kx16 DRAM with symmetrical addressing has 512 rows and 512 columns, whereas the asymmetrical addressing has 1024 rows and 256 columns. The number of columns defines the "depth" of a page.

Address Scheme	Row Addresses	Refresh Addresses	Column Addresses	
Symmetrical	A0R - A8R	A0R - A8R	A0C - A8C	preferred version
Asymmetrical	A0R - A9R	A0R - A9R	A0C- A7C	

Since the asymmetrical version needs to have special DRAM controllers and therefore usage of these devices is not very widespread, SIEMENS has concentrated the production to the version with symmetrical addressing.

LOW-POWER, EXTENDED & SELF REFRESH VERSION

The HYB 514171BJL is the low-power version with extended and self refresh of the 256kx16 DRAM. This low-power version has reduced CMOS standby current limits (typically from 1mA to 200 µA) and refresh interval eight times longer (from 15 µs per row to 125 µs per row). The extended refresh offers a battery backup mode, which is a low-current, data-retention cycle. It consists of a CAS-before-RAS refresh cycle at the slowest possible cycle rate. Low-power, extended-refresh DRAMs have the same functionality as a standard 256kx16 DRAM , except they have been tested to meet the lower CMOS standby current and the extended refresh specifications.

In addition to the standard refresh modes (RAS only refresh, CAS-before-RAS refresh and hidden refresh) the HYB 514171BJL additionally offers a **SELF-REFRESH** mode. This mode provides the DRAM with the ability to refresh itself and eliminates the need for an external refresh control circuitry. Self-refresh introduces new parameters, t_{RASS}, t_{CHS} and t_{RPS}. (fig. 2)

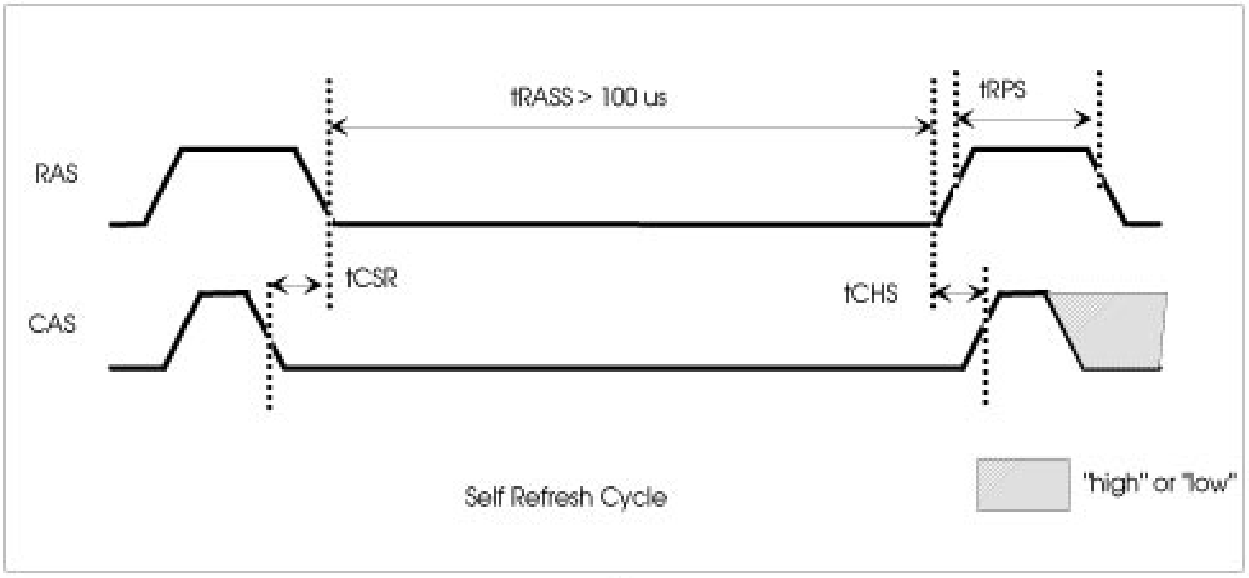


fig.2

The self-refresh mode is initiated by executing a CAS-before-RAS refresh cycle and holding both RAS and CAS low for a specified minimum period. The industry standard for this value is tRASS = 100 µs. After this time the DRAM internal timer starts and a new row is refreshed. When the refresh pulse is generated by the internal timer, the ICC current peaks but the current ICCS during the self refresh is guaranteed to be a maximum of 300 µA . The DRAM will remain in the self-refresh mode while RAS and CAS remain low. The self-refresh mode is terminated by taking RAS high for tRPS. Once the self-refresh mode has been terminated, the user can access the DRAM normally.

PACKAGE OUTLINE DRAWINGS

The SIEMENS 256k x 16 byte-wide DRAM is available in an industrial standard 400 mil wide 40 pin SOJ plastic package , appropriate for surface-mounting techniques . Package related data are shown in tab. 3 . The package outline dimensions of the SOJ 40 package can be seen in fig.3. All SIEMENS packages meet JEDEC standards.

CODES FOR MARKING

The marking on the top side of every 256k x 16 device gives information as to the device type , which access time specification is met, and the country of origin "Germany" . In addition, a weekcode indicated in which week of the year the part was tested.

A SIEMENS internal number is printed on the bottom side which represents the wafer production lot number, the date of final assembly and a code for the assembly line. Laser equipment is used for top and bottom side marking.

PACKING

Before packing, all devices are backed in metal tubes at 125 ^{o}C in ovens with circulating hot air for 12 hours. Within 24 hours the devices are seal packed. One sealed dry-pack box contains 50 tubes (each tube with 18 devices) along with a pouch of desiccant and a humidity indicator.

Deliveries in tape&reel are also available. Each dry-packed reel contains 900 devices on a 44 mm wide tape with 16mm pocket pitch.

For SOJ packaged devices SIEMENS recommends not to exceed a 72 hours time frame between unpacking and vaporphase or reflow soldering. Test have shown the increase on weight after 72 hour storage in a 27 ^{o}C , 55 % relative humidity environment is 0.1 %. After a vaporphase soldering at 215 ^{o}C of parts unpacked and stored for 72 hours no cracks could be found by optical inspection. Extended storage in a high humidity environment showed a saturation of weight increase of about 0.18 %.

256k x 16 DRAM
PROCESS RELATED DATA

PROCESS	0. 7um twin well CMOS on a p -type substrate 2 Polysilicon layer 1 Molybdenium silicide layer 1 Aluminium layer	
SIEMENS PROCESS NAME	C5DH	
TYPICAL DESIGN RULES		
LINE	0.7 µm	
SPACE	0.8 µm	
LITHOGRAPHY	G-LINE / I-LINE STEPPER	
CONTACT DIMENSIONS	0.9 µm x 1.1 µm AlSiCu / TiN-barrier metallisation	
CHANNEL LENGTH	N-channel	0.75 µm LDD
	P-channel	0.75 µm
OXIDE THICKNESS	18 nm	
JUNCTION DEPTH	N-channel	0.25 um
	P-channel	0.35 um
THRESHOLD VOLTAGE	N-channel	0.7 V
	P-channel	-1.1 V
CELL TYPE	TRENCH-CAPACITOR with fully over-lapping bitline contact (FOBIC) 13 nm eff ONO 4.5 um depth p-well depth 6um	
CELL CAPACITANCE	> 40 fF	
BITLINE TO CELL CAPACITANCE RATION	10 : 1	
ALUMINIUM		
THICKNESS	800 nm	
CONTENT	Al /Si / Cu	

tab. 1

256k x 16 DRAM
DESIGN RELATED DATA

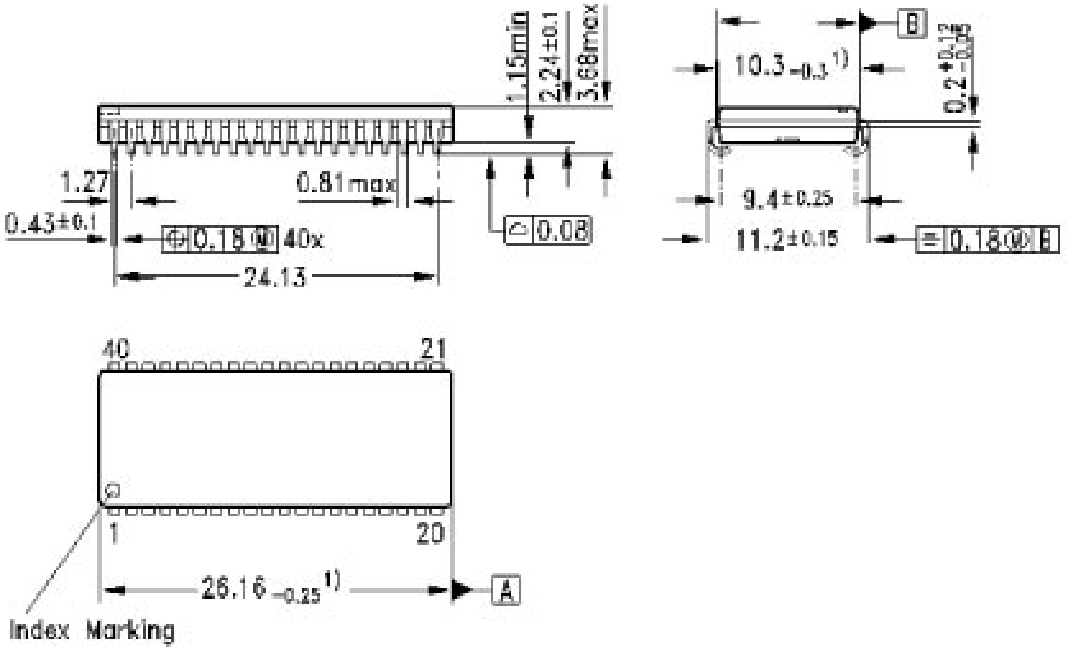
ORGANISATION	256k x 16
OPERATION MODES	FAST PAGE MODE Low-Power extended & self refresh mode
REFRESH	512 CYCLES / 16 ms (128 ms for L-version)
SPECIFICATIONS	
TRAC	50 / 60 / 70 ns
TCAC	15 / 15 / 20 ns
TAA	25 / 30 / 35 ns
CHIP SIZE	5.47 mm x 11.70 mm = 64.00 mm^2
CELL SIZE	1.73 µm x 3.46 µm = 5.98 μm^2
SENSE LINE	FOLDED BITLINE CONCEPT with 16 blocks of 256k cells
WORDLINE PITCH	1.73 µm
BITLINE PITCH	1.73 µm
REDUNDANCY	
ROWS	16
COLUMNS	64
METHOD	Laser
NUMBER OF DEVICES	
transistors	4.7 Mio.
trench capacitors	4.2 Mio.
contact holes	3.0 Mio.

tab. 2

256k x 16 DRAM
ASSEMBLY RELATED DATA

PACKAGE TYPE	Surface mount package
PACKAGE	400 mil wide SOJ 40 package JEDEC-standard
LEAD FRAME	CDA C19400-H / Ag spot
LEAD FINISH	SnPb 80/20
DIE ATTACH	Silver filled epoxy
WIRE BOND	33 um Au wires, thermosonic
CHIP PROTECTION	Polyimid layer
MOLDING COMPOUND	KCM 184 VA

tab.3



1) Does not include plastic or metal protrusions of 0.25 max per side

fig.3