SIEMENS

HYB 514400BJ/BJL -50/-60/-70
HYB 514400BT/BTL-50/-60/-70
1 048 576 x 4 - Bit Dynamic RAM

INFORMATION NOTE NO.19

Fifth Generation 1M x 4 - DRAM
(Ultrashrink-Version)

Characterisation Data

10.95
Info4m19.doc

This information note is intended to provide technical information on the SIEMENS 1M x 4 fifth generation ("Hypershrink-Version") DYNAMIC ACCESS MEMORIES HYB514400B.

CHARACTERISTICS OF DC - PARAMETERS

The SIEMENS HYB 514400B 1M x 4 DRAM device is guarantied to meet certain DC parametric limits over the temperature range 0^{o} to 70^{o}C. This information note shows the actual performance levels that can typically be expected from devices. Samples out of three different production lots have been randomly selected and characterised.

Typical values of operation and standby currents as a function of temperature, voltage and cycle time are shown in fig.1 through fig. 5.

In fig. 6 the typical behaviour of V_{IHmin} (minimum TTL-level input high voltage) , V_{ILmax} (maximum TTL-level input low voltage), V_{OH}/V_{OL} (output high and low voltage) as a function of supply voltage is shown.

CHARACTERISTICS OF AC - PARAMETERS

Supply voltage and temperature dependence of row (trac), column (tcac), address access times (taa) and output enable access time (toea) are the topics of fig. 7 and fig. 8.

All other AC - parameters measured at two voltages (VCC = 4.5 V and 5.5 V) and two temperatures (+85^{o}C and - 10^{o}C) are put together in table 1.

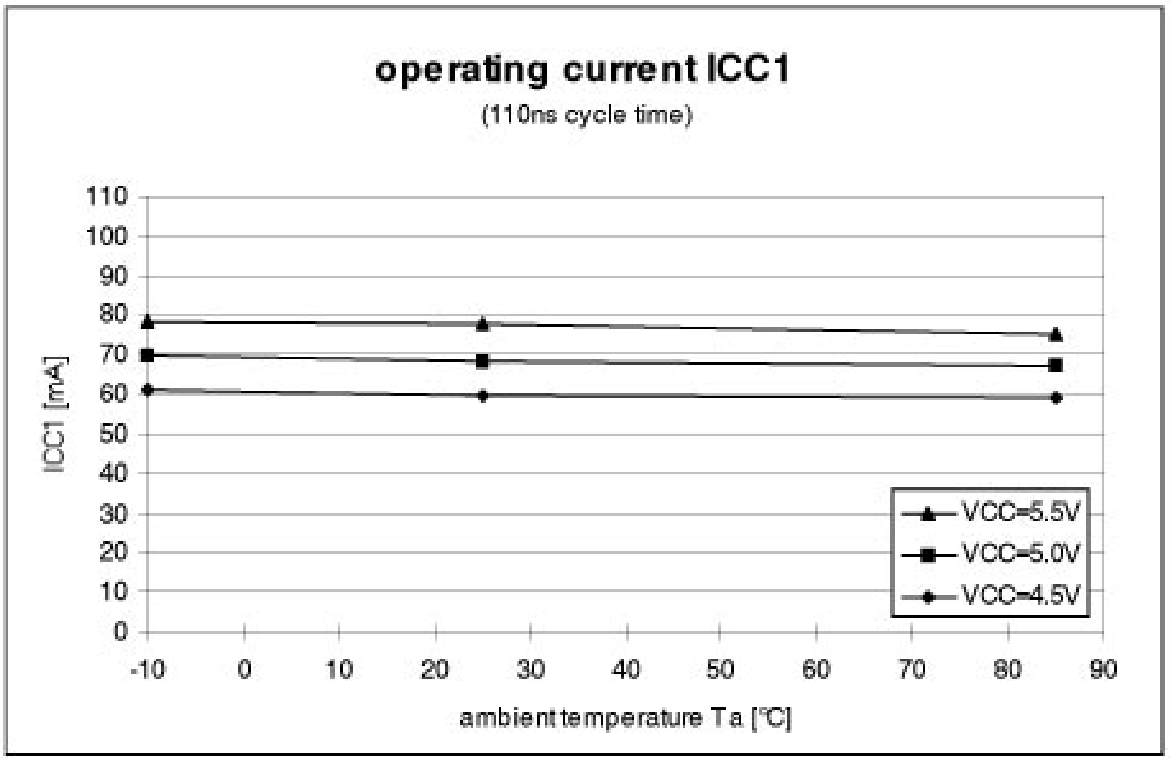
PEAK CURRENT PROFILES

Fig. 9 through 11 show the current profiles for Read Data "0" , Read Data "1" and for a Write Cycle.

Influence of Capacitive Loads on Access Time

All DRAM access times depend on output loading. The influence of capacitive loading from 50 pF to 150 pf is shown in fig. 12. Note that all parametric measurements in all other figures and tables are performed with a 100 pF load according to the data sheets for fast page mode DRAMs.

All measurements shown in this information note have been performed on an ADVANTEST 5361 dedicated memory test system.


operating current ICC1
(110ns cycle time)
ICC1 [mA]
110
100
90
80
70
60
50
40
30
20
10
0
-10
0
10
20
30
40
50
60
70
80
90
ambient temperature Ta [°C]
VCC=5.5V
VCC=5.0V
VCC=4.5V

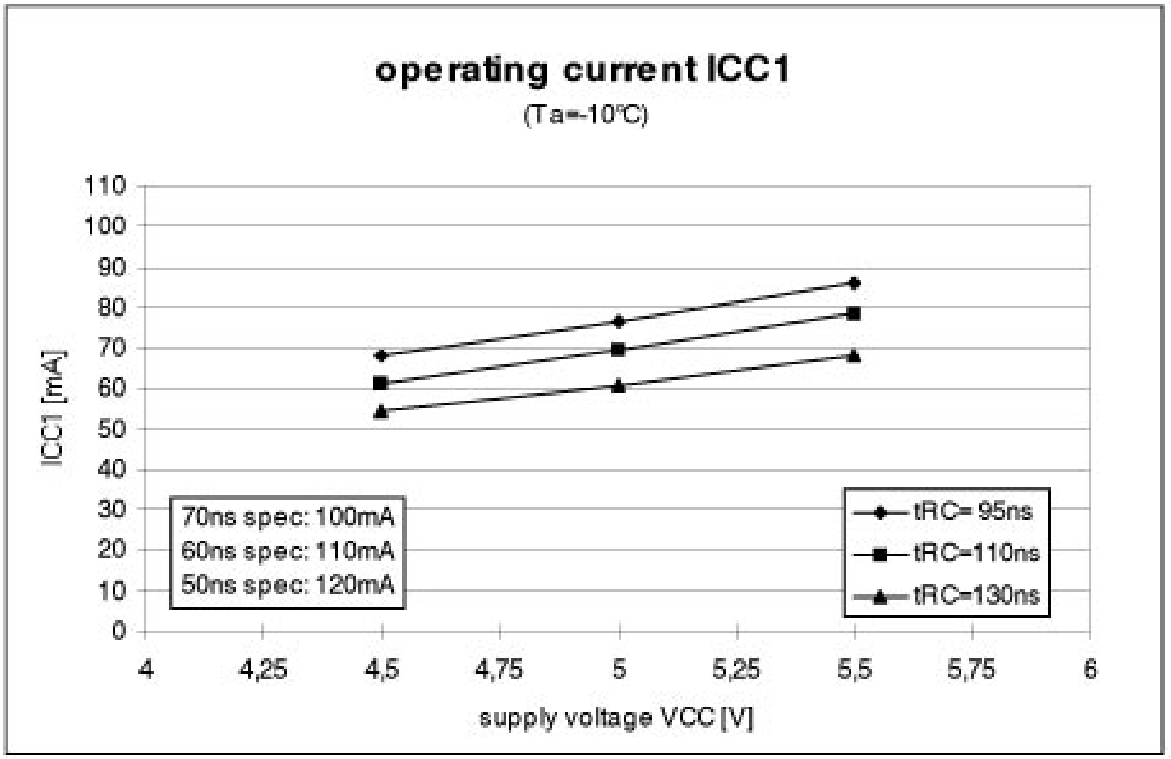
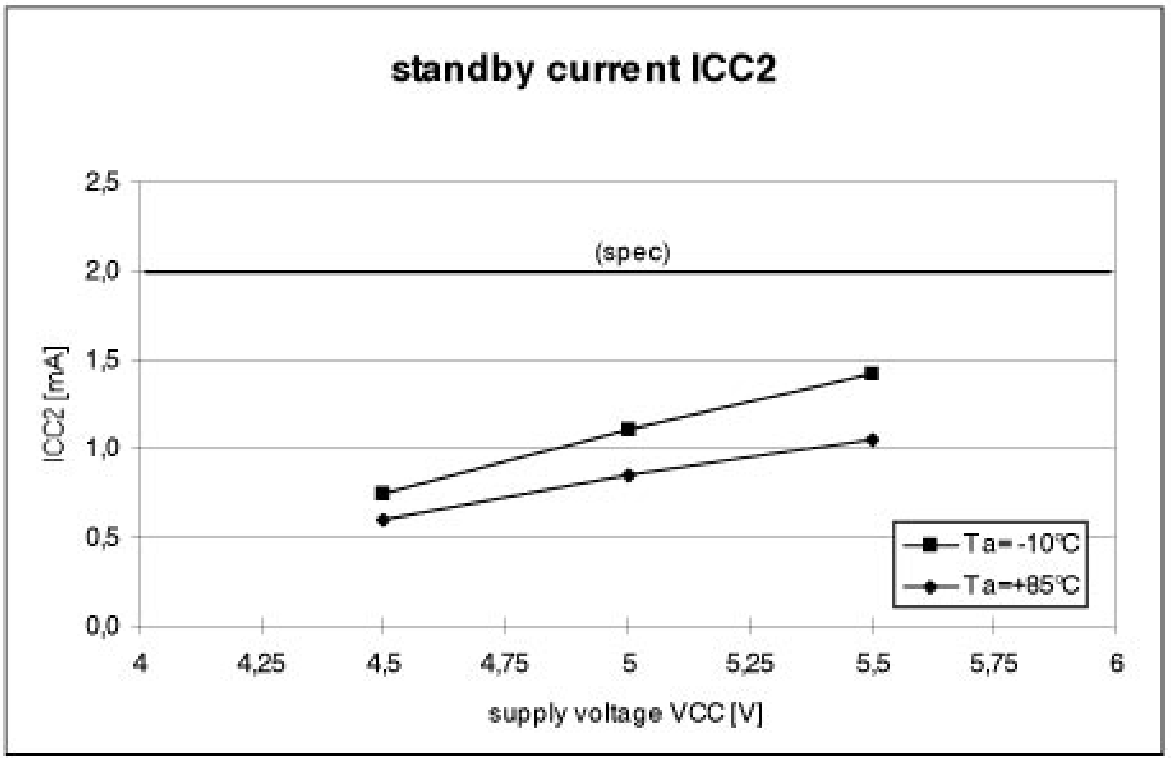

operating current ICC1
(Ta=-10°C)
ICC1 [mA]
110
100
90
80
70
60
50
40
30
20
10
0
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
70ns spec: 100mA
60ns spec: 110mA
50ns spec: 120mA
tRC= 95ns
tRC=110ns
tRC=130ns

fig.1


standby current ICC2
2,5
2,0
1,5
1,0
0,5
0,0
ICC2 [mA]
(spec)
Ta= -10°C
Ta=+85°C
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]

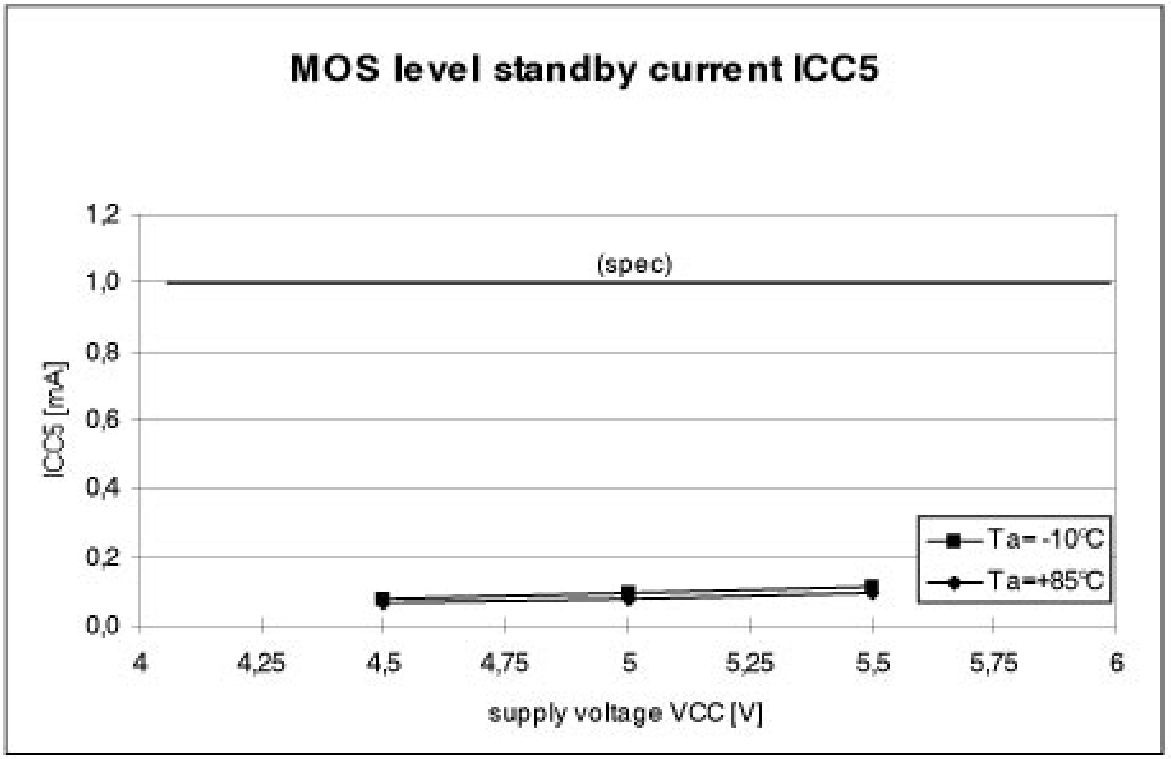
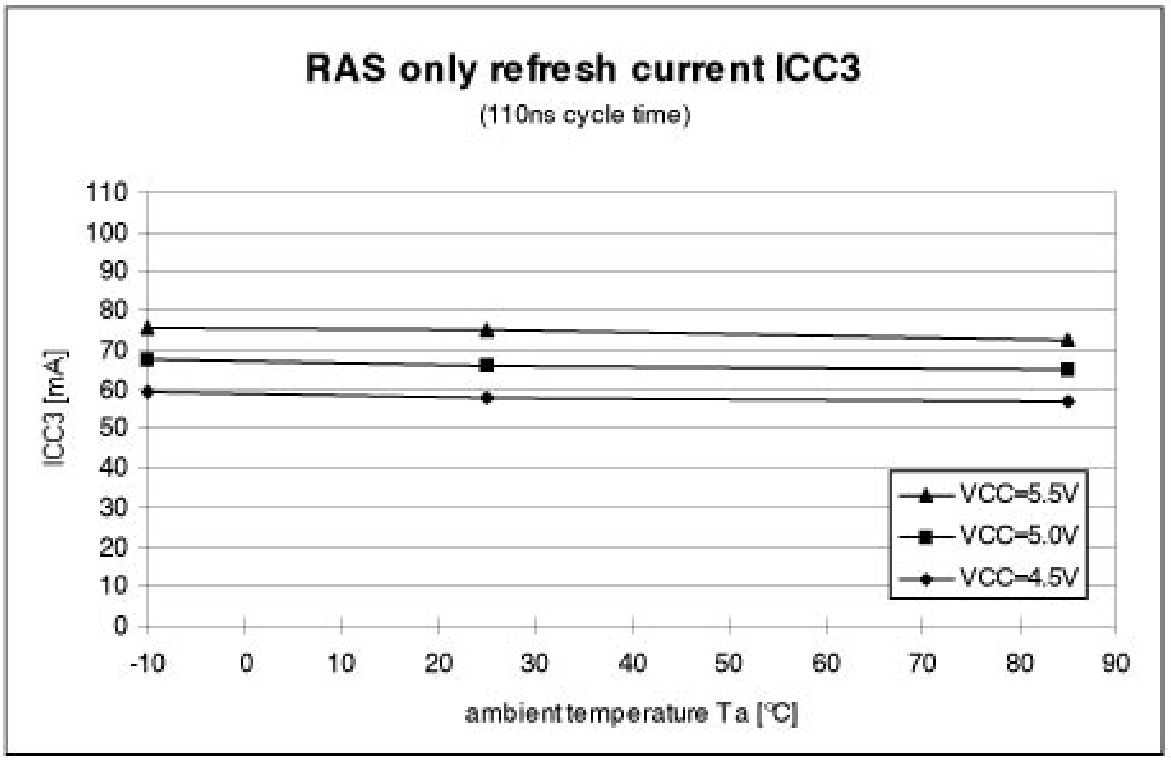

MOS level standby current ICC5
1,2
1,0
0,8
0,6
0,4
0,2
0,0
ICC5 [mA]
(spec)
Ta= -10°C
Ta=+85°C
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]

fig.2


RAS only refresh current ICC3
(110ns cycle time)
ICC3 [mA]
110
100
90
80
70
60
50
40
30
20
10
0
-10
0
10
20
30
40
50
60
70
80
90
ambient temperature Ta [°C]
VCC=5.5V
VCC=5.0V
VCC=4.5V

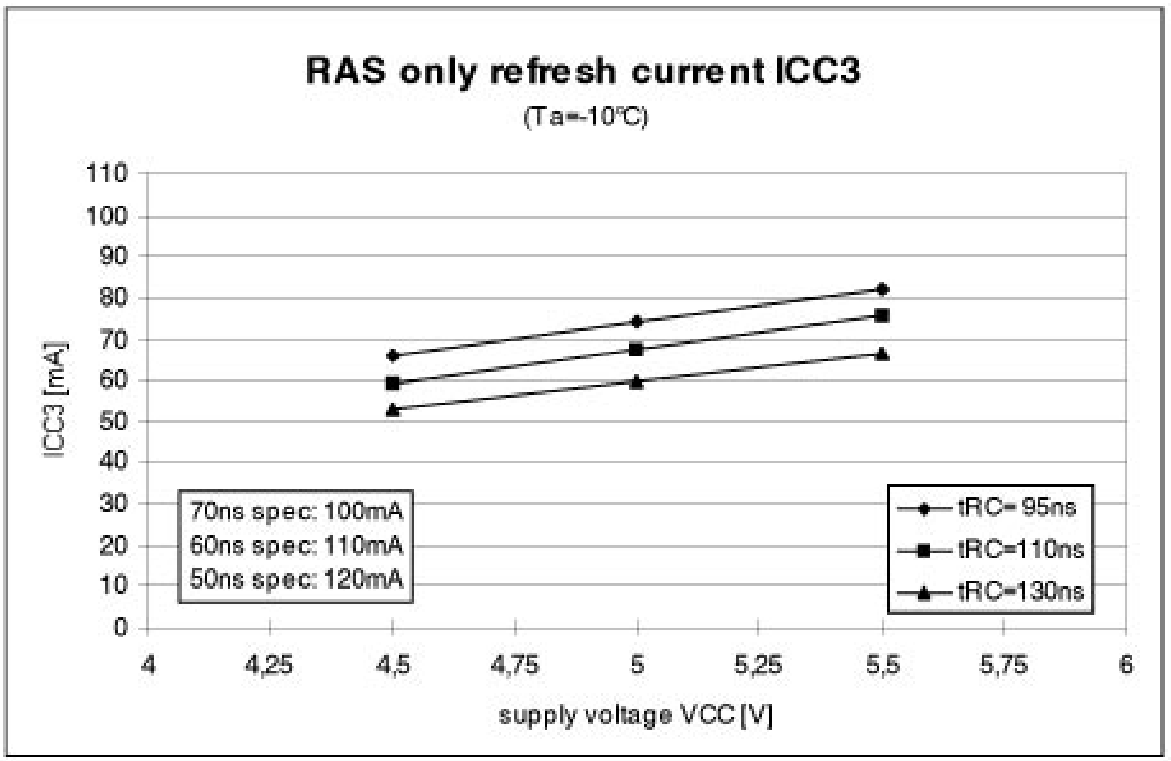
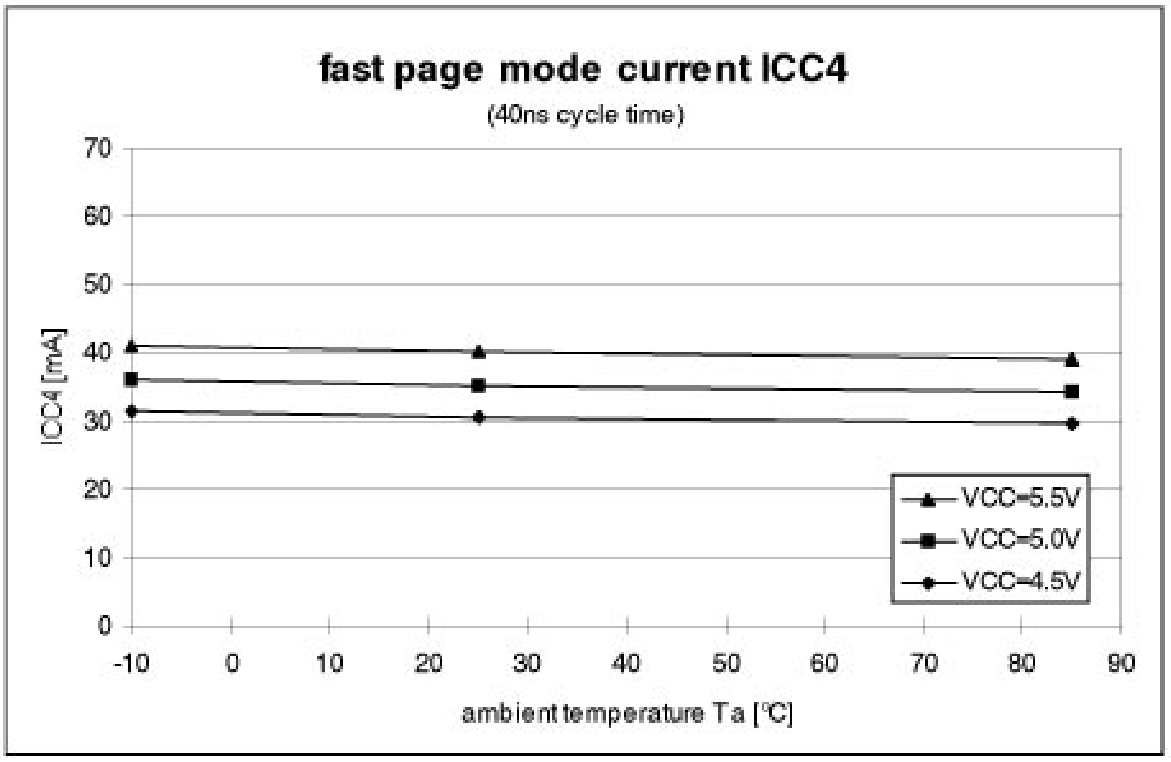

RAS only refresh current ICC3
(Ta=-10°C)
ICC3 [mA]
110
100
90
80
70
60
50
40
30
20
10
0
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
70ns spec: 100mA
60ns spec: 110mA
50ns spec: 120mA
tRC= 95ns
tRC=110ns
tRC=130ns

fig.3


fast page mode current ICC4
(40ns cycle time)
ICC4 [mA]
70
60
50
40
30
20
10
0
-10
0
10
20
30
40
50
60
70
80
90
ambient temperature Ta [°C]
VCC=5.5V
VCC=5.0V
VCC=4.5V

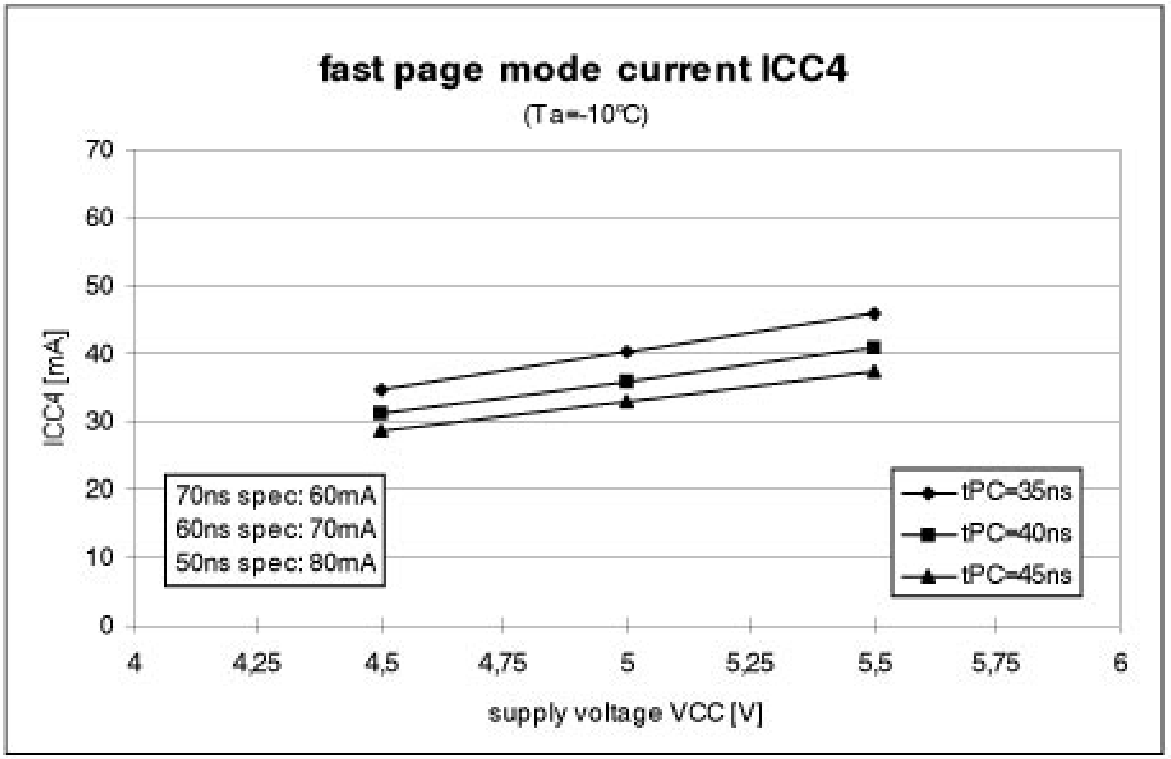
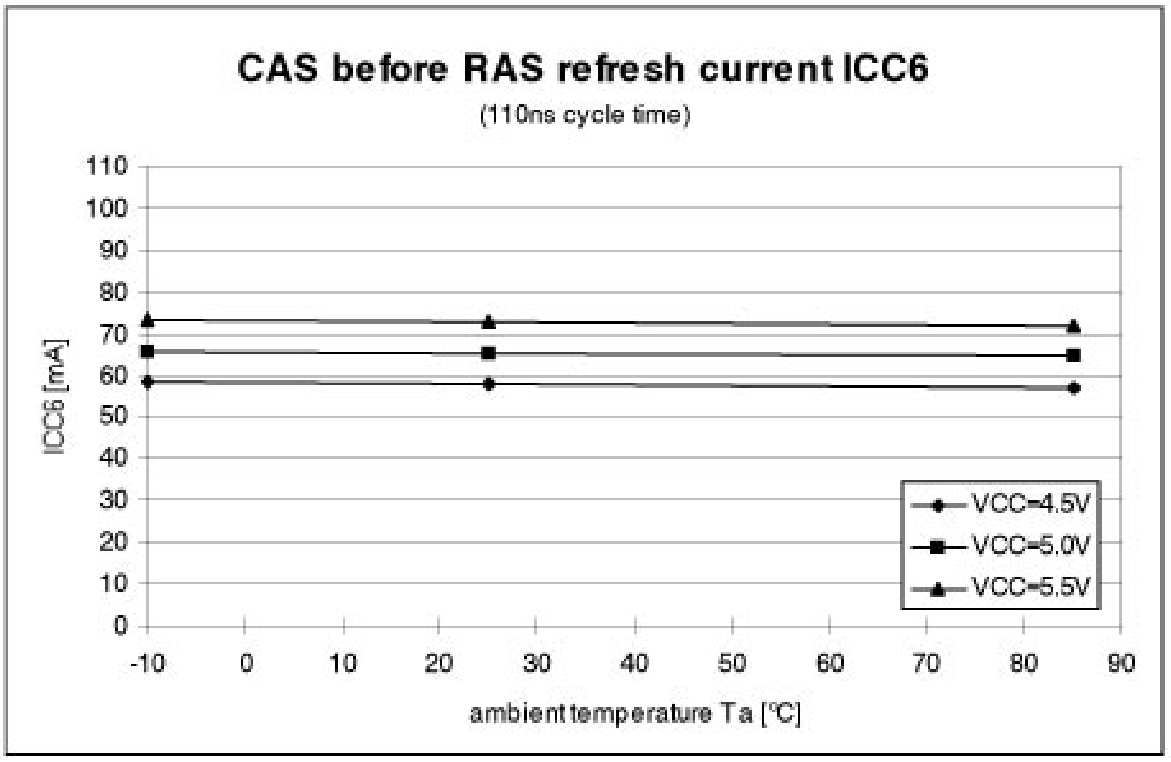

fast page mode current ICC4
(Ta=-10°C)
ICC4 [mA]
70
60
50
40
30
20
10
0
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
70ns spec: 60mA
60ns spec: 70mA
50ns spec: 80mA
tPC=35ns
tPC=40ns
tPC=45ns

fig.4


CAS before RAS refresh current ICC6
(110ns cycle time)
ICC6 [mA]
110
100
90
80
70
60
50
40
30
20
10
0
-10
0
10
20
30
40
50
60
70
80
90
ambient temperature Ta [°C]
VCC=4.5V
VCC=5.0V
VCC=5.5V

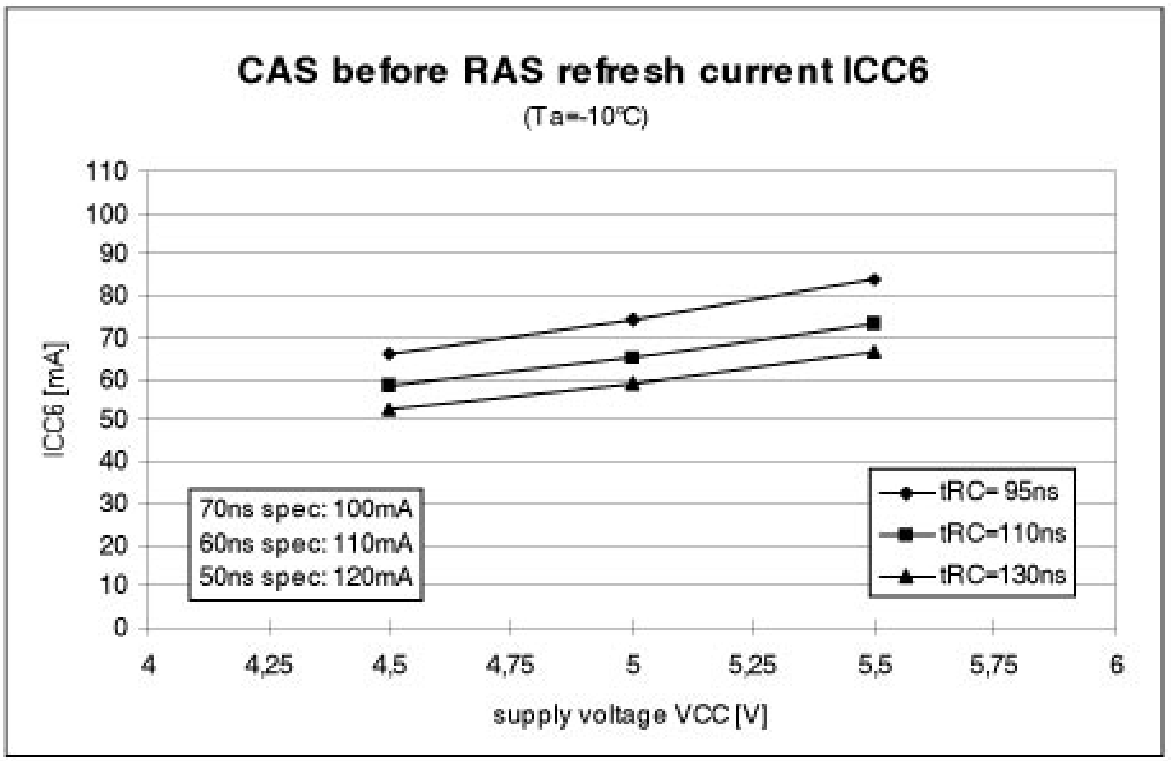
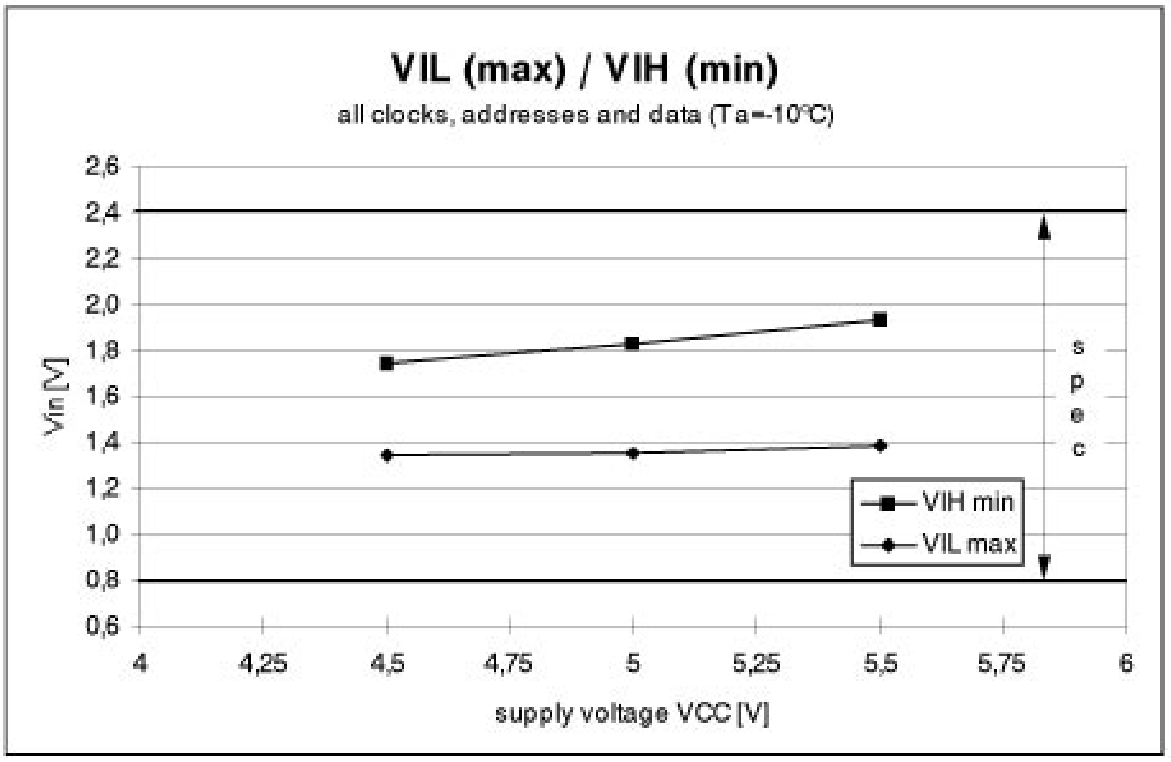

CAS before RAS refresh current ICC6
(Ta=-10°C)
ICC6 [mA]
110
100
90
80
70
60
50
40
30
20
10
0
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
70ns spec: 100mA
60ns spec: 110mA
50ns spec: 120mA
tRC= 95ns
tRC=110ns
tRC=130ns

fig.5


VIL (max) / VIH (min)
all clocks, addresses and data (Ta=-10°C)
Vin [V]
2,6
2,4
2,2
2,0
1,8
1,6
1,4
1,2
1,0
0,8
0,6
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
VIH min
VIL max
spec

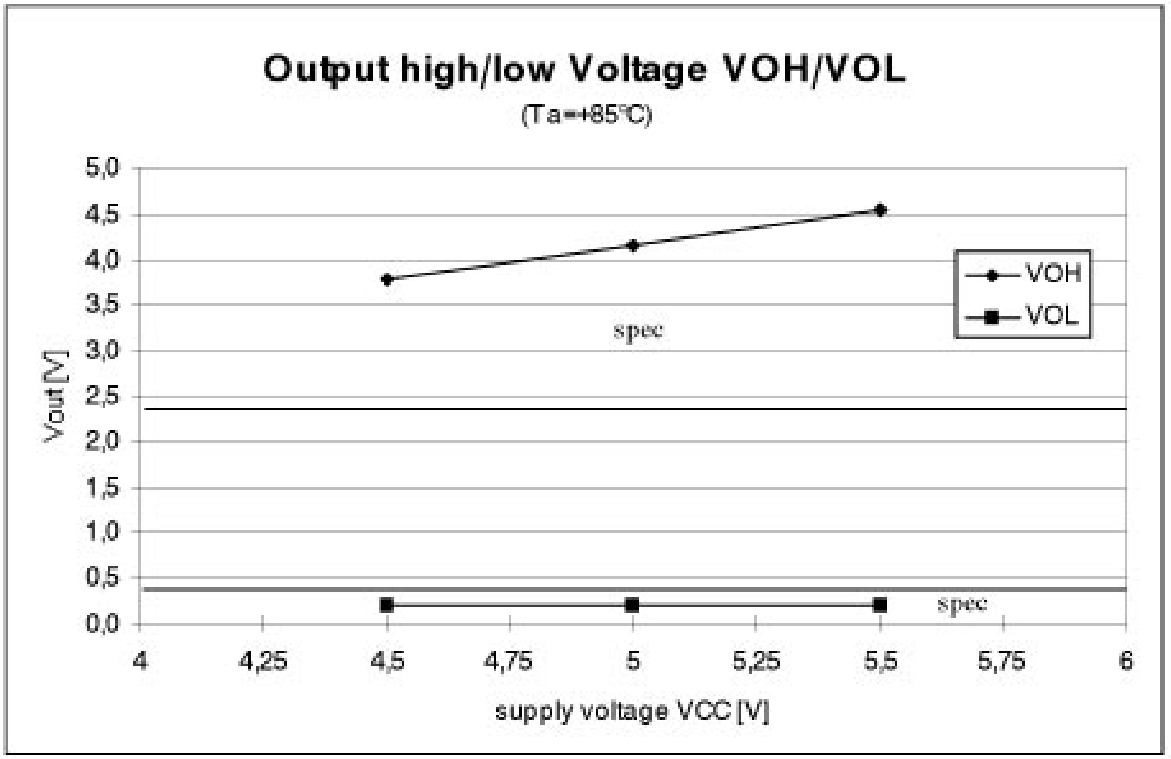
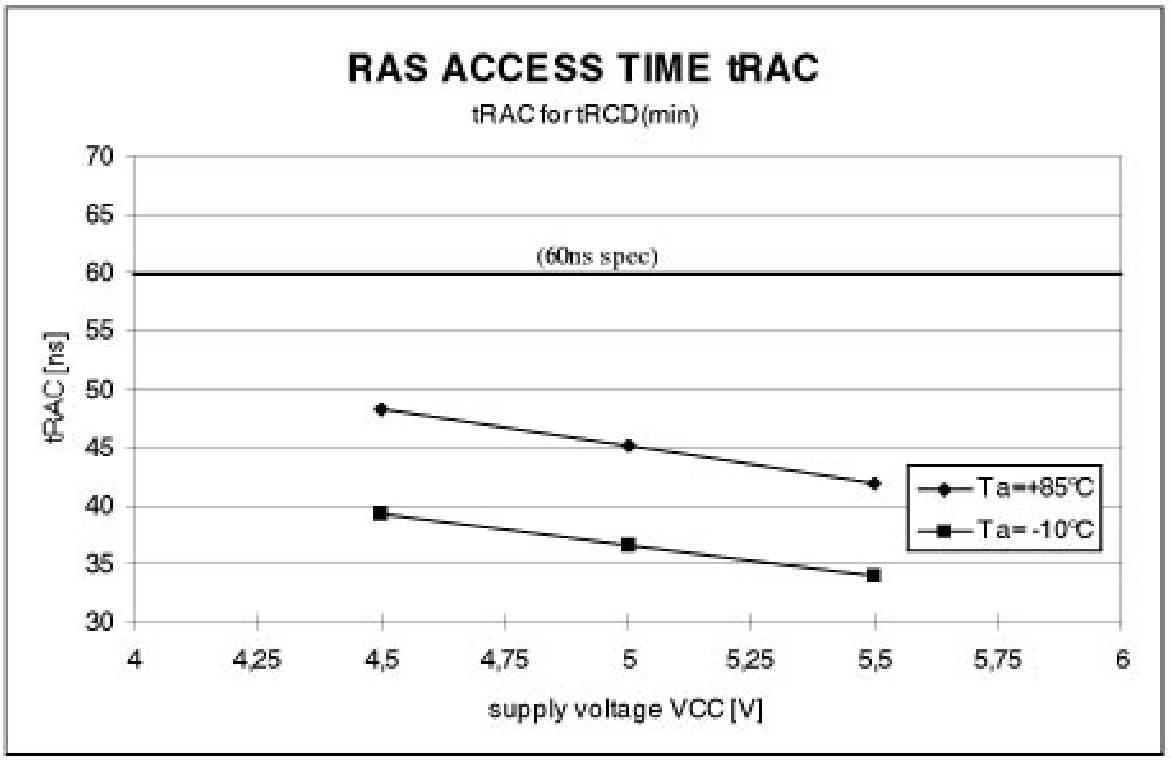

Output high/low Voltage VOH/VOL
(Ta=+85°C)
Vout [V]
5,0
4,5
4,0
3,5
3,0
2,5
2,0
1,5
1,0
0,5
0,0
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
VOH
VOL
spec
spec

fig.6


RAS ACCESS TIME tRAC
tRAC for tRCD(min)
70
65
60
55
50
45
40
35
30
(60ns spec)
tRAC [ns]
Ta=+85°C
Ta= -10°C
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]

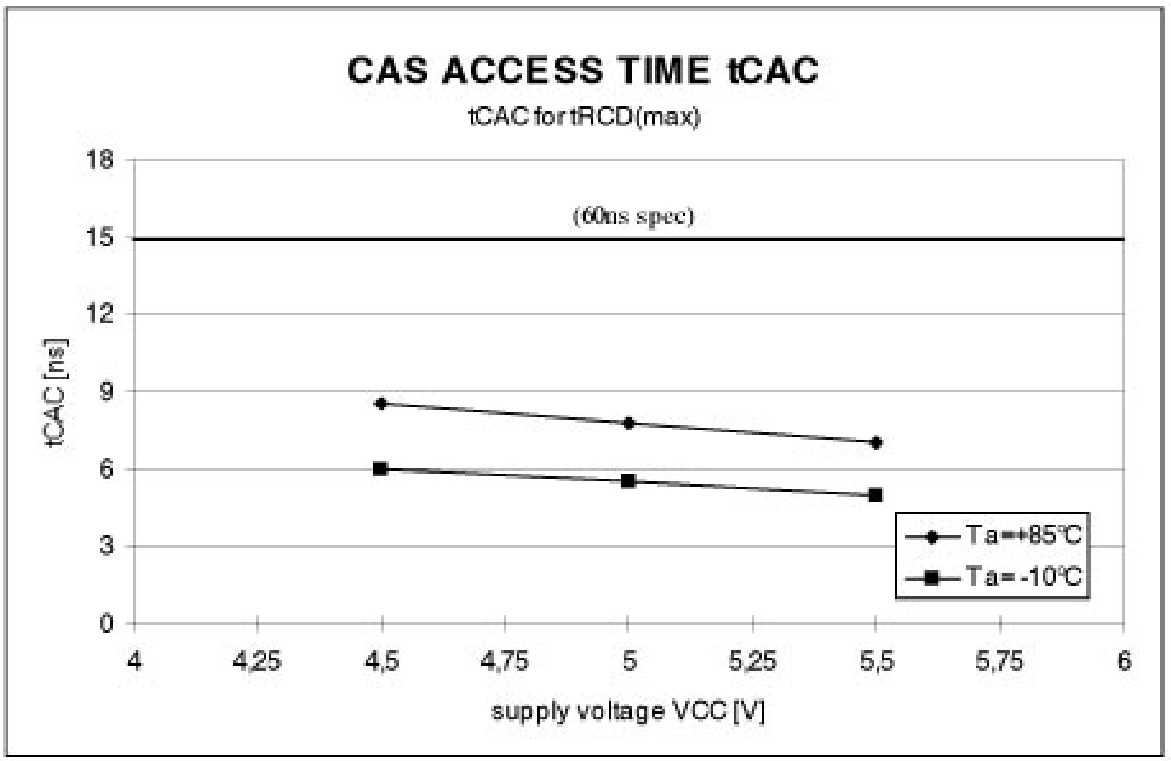
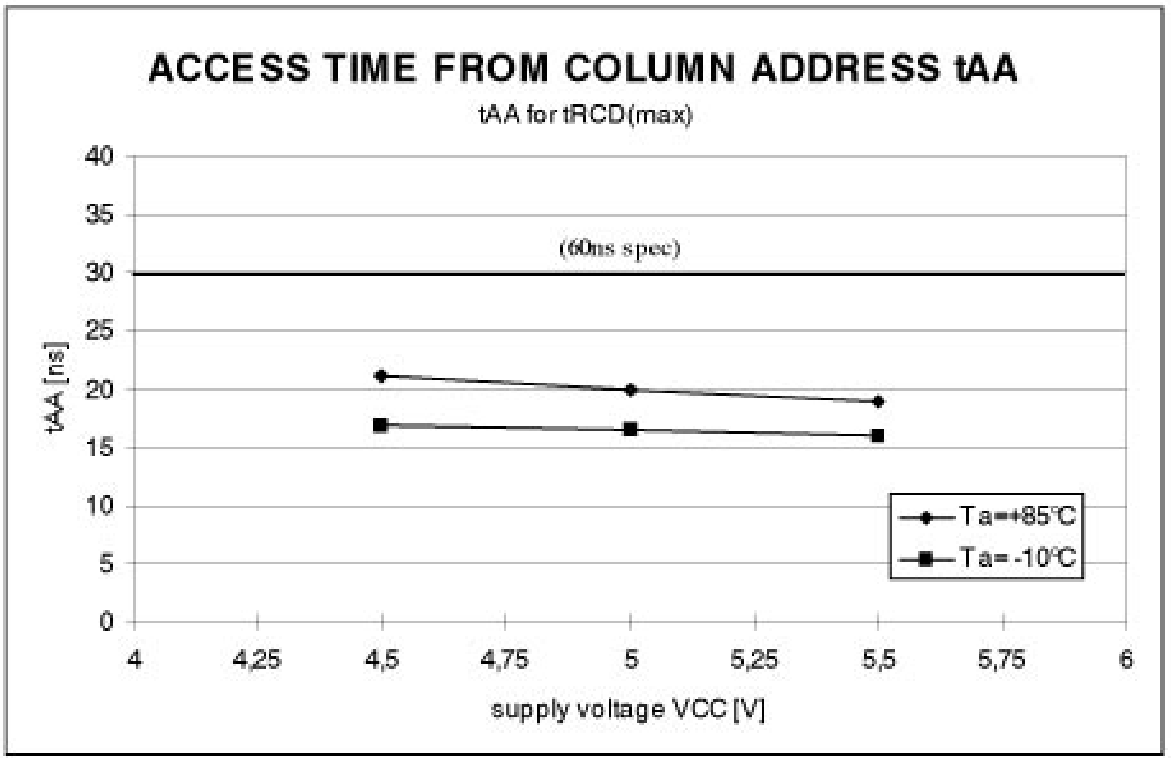

CAS ACCESS TIME tCAC
tCAC for tRCD(max)
18
15
12
9
6
3
0
(60ns spec)
tCAC [ns]
Ta=+85°C
Ta= -10°C
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]

fig.7


ACCESS TIME FROM COLUMN ADDRESS tAA
tAA for tRCD(max)
(60ns spec)
tAA [ns]
40
35
30
25
20
15
10
5
0
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
Ta=+85°C
Ta= -10°C

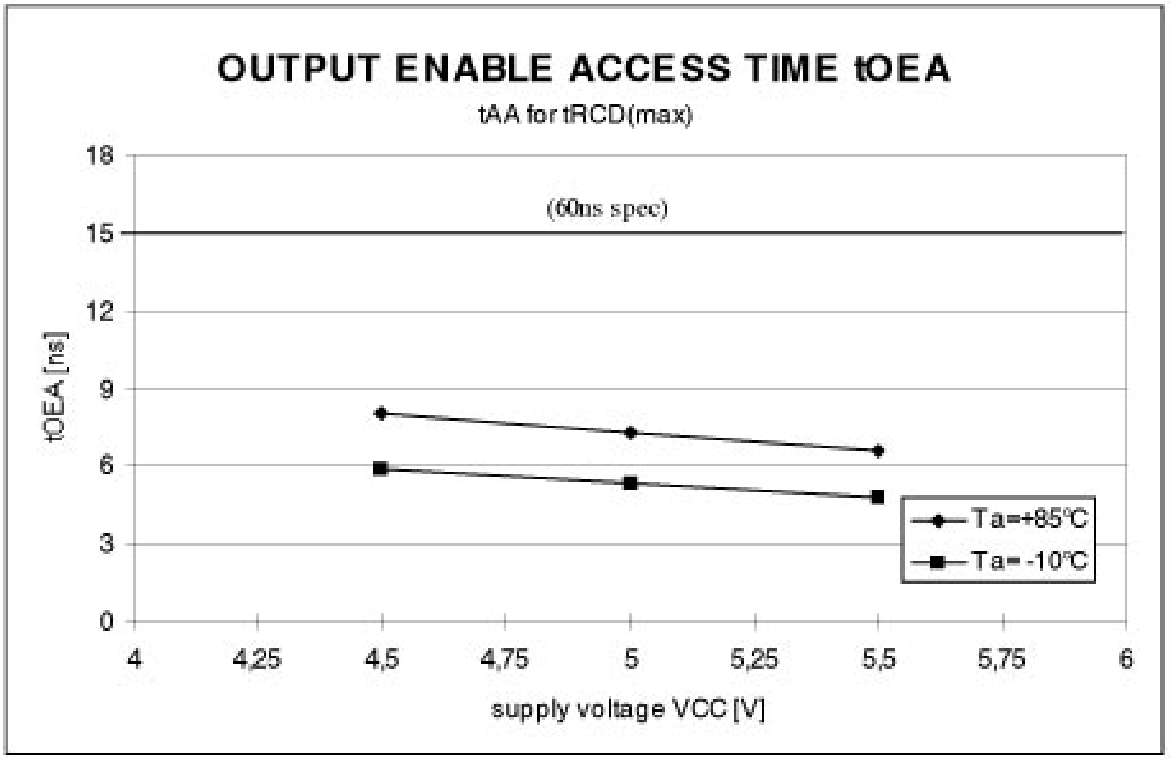

OUTPUT ENABLE ACCESS TIME tOEA
tAA for tRCD(max)
(60ns spec)
tOEA [ns]
18
15
12
9
6
3
0
4
4,25
4,5
4,75
5
5,25
5,5
5,75
6
supply voltage VCC [V]
Ta=+85°C
Ta= -10°C

fig.8

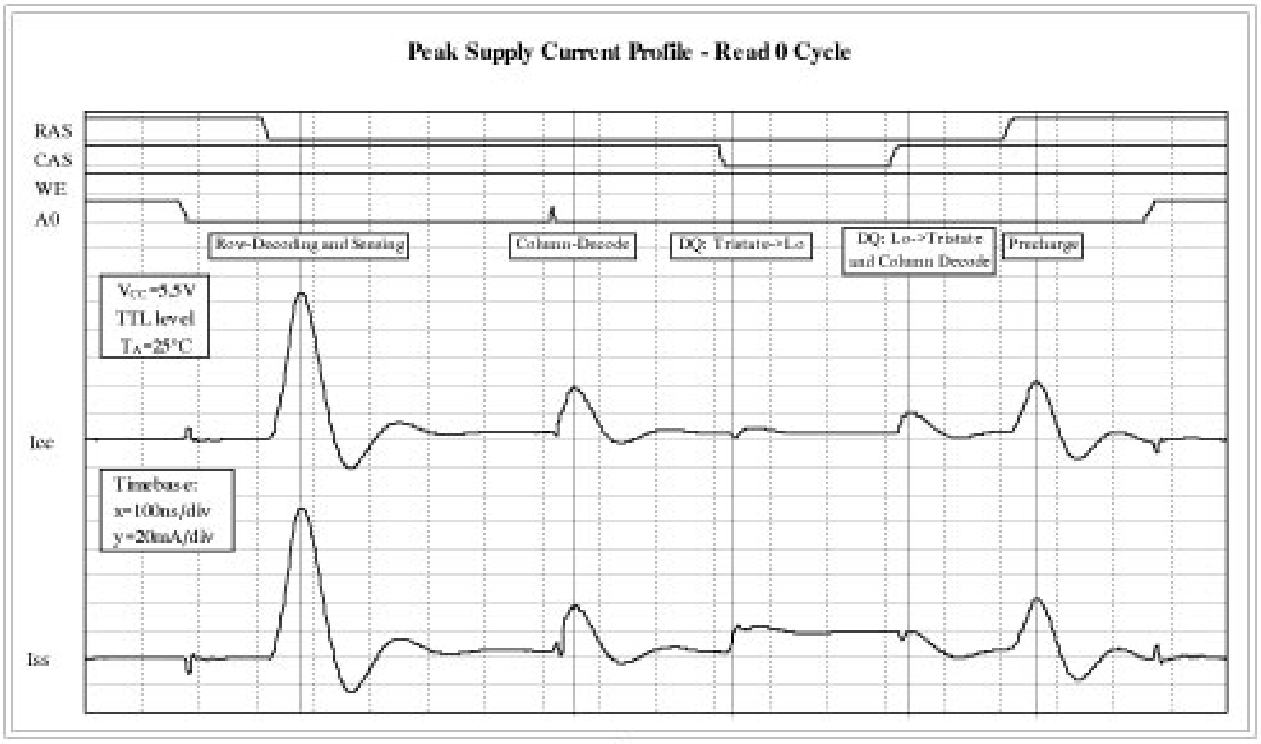

Peak Supply Current Profile - Read 0 Cycle
RAS
CAS
WE
A0
Row-Decoding and Sensing
Column-Decode
DQ: Tristate->Lo
DQ: Lo->Tristate and Column Decode
Precharge
V_{CC}=5.5V
TTL level
T_A=25°C
Icc
Timebase:
x=100ns/div
y=20mA/div
Iss

fig.9

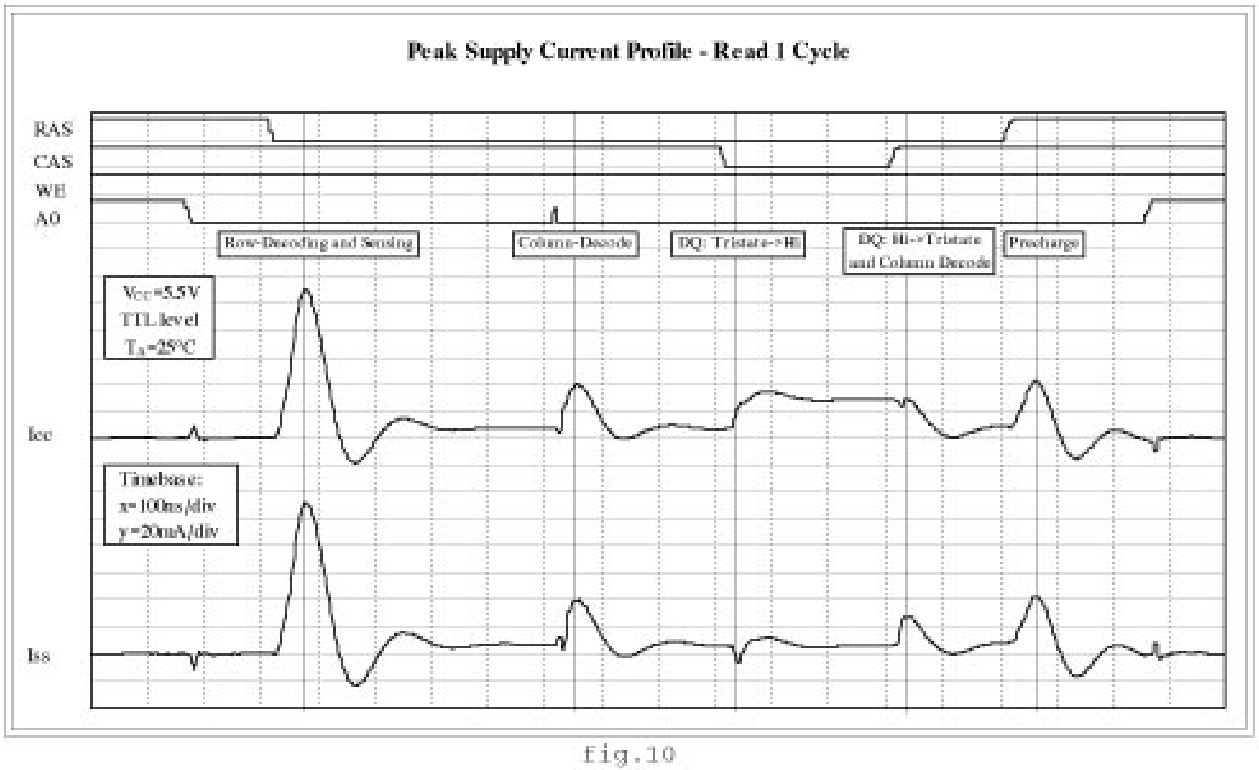

Peak Supply Current Profile - Read 1 Cycle
RAS
CAS
WE
A0
Row-Decoding and Sensing
Column-Decode
DQ: Tristate->HI
DQ: HI->Tristate and Column Decode
Precharge
V_{CC}=5.5V
TTL level
T_A=25°C
Icc
Timebase:
x=100ns/div
y=20mA/div
Iss

fig.10

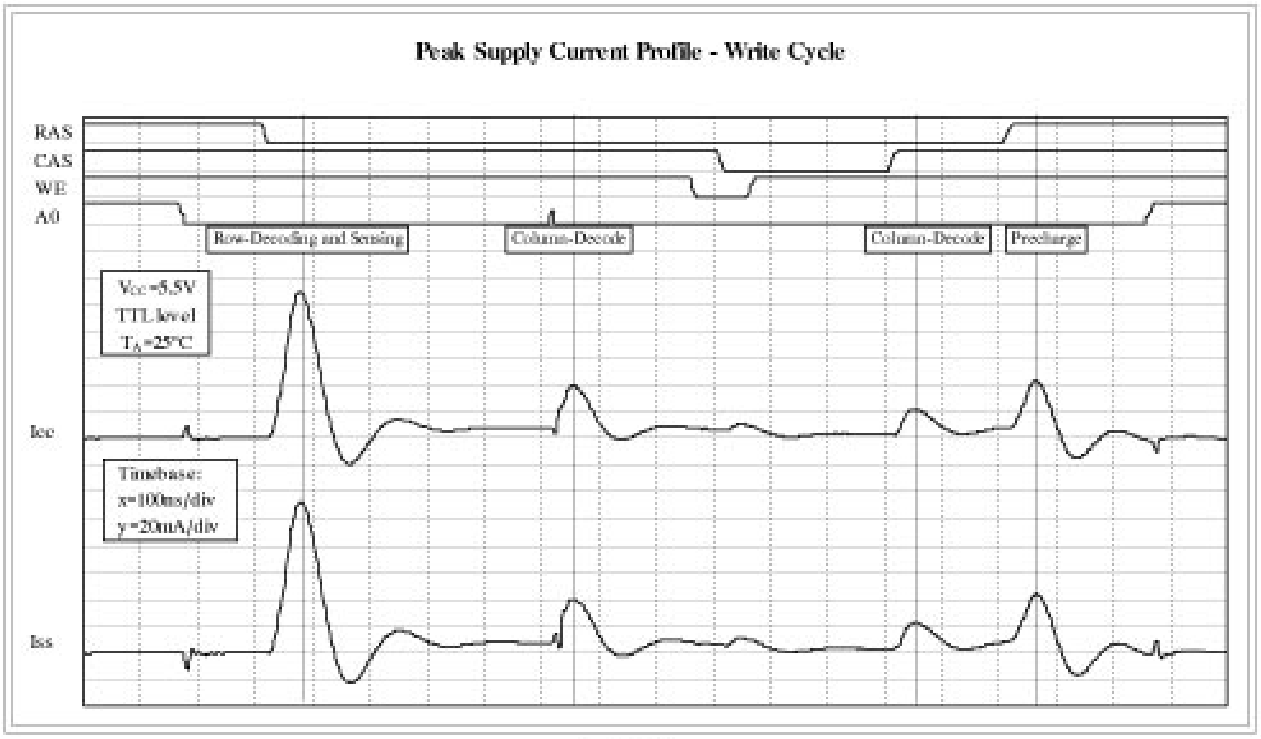

Peak Supply Current Profile - Write Cycle
RAS
CAS
WE
A0
Row-Decoding and Sensing
Column-Decode
Column-Decode
Precharge
Vcc =5.5V
TTL-level
TA =25°C
Icc
Timebase:
x=100ns/div
y=20mA/div
Iss

fig.11

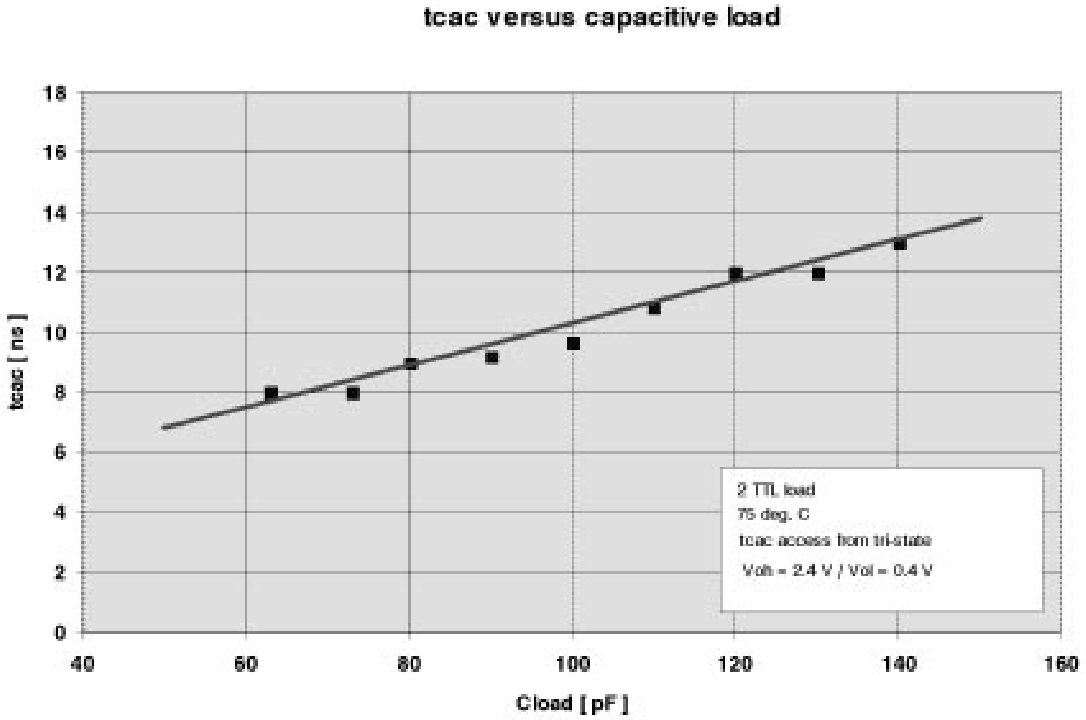

tcac versus capacitive load
tcac [ns]
Cload [pF]
2 TTL load
75 deg. C
tcac access from tri-state
Voh = 2.4 V / Vol = 0.4 V
0
2
4
6
8
10
12
14
16
18
40
60
80
100
120
140
160

fig.12

Table 1:

AC CHARACTERISTICS
Device : 1M x 4 DRAM

COMMON PARAMETERS

Parameter	Spec -60ns		Measurement		(tT = 5ns)		
	Unit [ns]		Ta = -10°C		Ta = +85°C		note
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V	1)
trc	110	-	72	67	83	75	
trp	40	-	15	13	22	19	
tras	60	10000	20	19	25	20	2)
tcas	15	10000	0	0	4	2	3)
tasr	0	-	-7	-6	-9	-7	
trah	10	-	1	0	2	1	
tasc	0	-	-9	-9	-9	-9	
tcah	15	-	3	2	5	3	
tar	50	-	<=25	<=25	29	<=25	
trcd (min)	20	-	5	5	6	6	
trcd (max)	-	-	33	29	40	35	4)
trad	15	30	6	5	7	6	
trsh	15	-	0	-1	1	0	
tcsh	60	-	34	29	43	37	
tcrp	5	-	-3	-2	-3	-2	
troh	10	-	-6	-7	-6	-7	
toez	0	20	7	7	7	7	

READ CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
trac	-	60	39	34	48	42
tcac	-	15	6	5	9	7
taa	-	30	17	16	21	19
toea	-	15	6	5	8	7
trcs	0	-	-8	-7	-9	-8
trch	0	-	-7	-6	-8	-6
trrh	0	-	-7	-5	-7	-6
tral	30	-	<=5	<=5	7	6
toff	0	20	2	2	4	4

WRITE CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
twcs	0	-	-6	-6	-7	-7
twch	10	-	-1	-2	1	0
twp	10	-	-1	-1	0	-1
trwl	15	-	-2	-3	-1	-2
tcwl	15	-	0	-1	2	0
tds	0	-	-6	-5	-7	-6
tdh	15	-	-1	-1	1	0
twcr	50	-	19	18	21	20
tdhr	50	-	<=20	<=20	21	<=20
toeh	20	-	-2	-3	-1	-3

READ-MODIFY-WRITE CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C		note
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V	
trwc	160	-	103	97	113	106	
trwd	90	-	56	51	65	59	
tcwd	45	-	22	21	25	23	
tawd	60	-	34	33	37	36	

REFRESH CYCLE
CAS-BEFORE-RAS CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
tcsr	5	-	-4	-4	-3	-3
tchr	15	-	-7	-8	-7	-8
trpc	0	-	-7	-6	-8	-7
tcpn	10	-	-1	0	-1	0
twrp	10	-	-5	-3	-5	-4
twrh	10	-	-5	-5	-5	-5

FAST PAGE MODE CYCLE

	Unit [ns]		Ta = -10°c		Ta = +85°C		
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V	
tpc	40	-	<=32	<=32	<=32	<=32	
tcp	10	-	-1	0	0	1	
trasp	60	200000	20	19	25	20	2)
tcpa	-	35	21	19	26	24	
tprwc	90	-	51	49	55	54	

TEST MODE CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
twts	10	-	-4	-4	-4	-4
twth	10	-	-4	-5	-4	-5

CAS-BEFORE-RAS COUNTER TEST CYCLE

	Unit [ns]		Ta = -10°C		Ta = +85°C	
	min.	max.	Vcc = 4.5V	Vcc = 5.5V	Vcc = 4.5V	Vcc = 5.5V
tcpt	30	-	0	1	1	1

Notes:

1) all AC-parameters are measured with 0.85V / 2.35 V levels on clock and addresses and with tf = 5ns.
2) the "min."-value is shown.
3) tcas(min.)-value in a write cycle is shown.
4) trcd(max.) is the reference point where the access time is controlled by tcac.