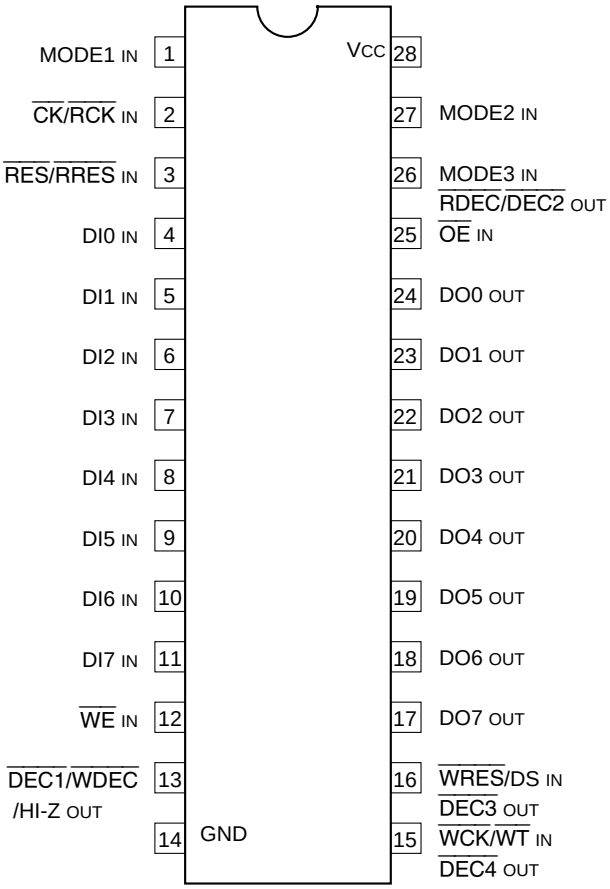
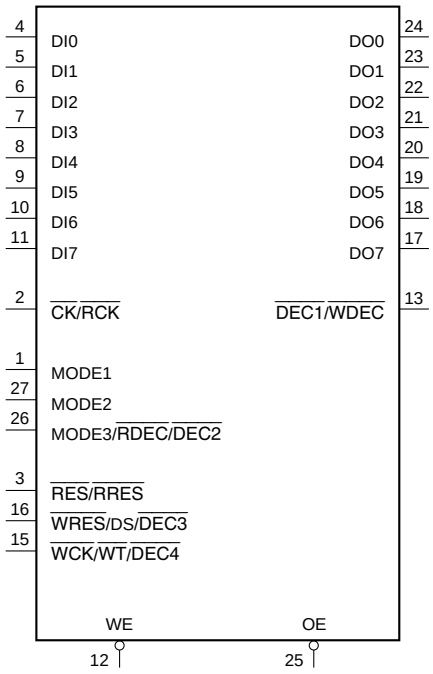
C-MOS 16 K (2,048 × 8)-BIT LINE MEMORY

—TOP VIEW—





MODE1	MODE2	MODE3	MODE
1	1	1	TIME BASE COMPRESSING /EXPANDING
1	1	0	DOUBLE SPEED EXCHANGE
1	0	∗	TBC
0	1	∗	1H/2H DELAY
0	0	∗	DELAY LINE

0 ; LOW LEVEL
1 ; HIGH LEVEL
∗ ; DEC OUTPUT SIGNAL

MODE1, 2, 3 ; MODE SELECT INPUTS
RCK ; READ CLOCK INPUT
WCK ; WRITE CLOCK INPUT
CK ; CLOCK INPUT
RRES ; READ RESET INPUT
RES ; RESET INPUT
DI0 - DI7 ; DATA INPUTS
WE ; WRITE ENABLE INPUT
HI-Z ; HIGH IMPEDANCE
WT ; WRITE TIMING INPUT
DEC1, 2, 3, 4 ; DECODE PULSE OUTPUTS
WDEC ; WRITE DECODE PULSE OUTPUT
RDEC ; READ DECODE PULSE OUTPUT
DS ; DELAY SELECT INPUT
DO0 - DO7 ; DATA OUTPUTS
OE ; OUTPUT ENABLE INPUT

PIN NO.	MODE				
	TIME BASE COMPRESSING /EXPANDING	DOUBLE SPEED EXCHANGE	TBC	1H/2H DELAY	DELAY LINE
1	MODE1				
2	$\overline{RCK}$			$\overline{CK}$	
3	$\overline{RRES}$			$\overline{RES}$	
4 - 11	DI0 - DI7				
12	$\overline{WE}$				
13	HI-Z		$\overline{WDEC}$	$\overline{DEC1}$	
15	$\overline{WCK}$			$\overline{WT}$	$\overline{DEC4}$
16	$\overline{WRES}$			DS	$\overline{DEC3}$
17 - 24	DO0 - DO7				
25	$\overline{OE}$				
26	MODE3		$\overline{RDEC}$	$\overline{DEC2}$	
27	MODE2