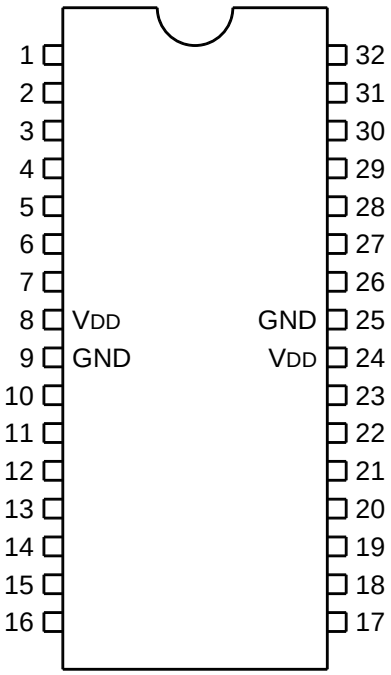
C-MOS 1 M (131,072 × 8)-BIT SRAM

—TOP VIEW—



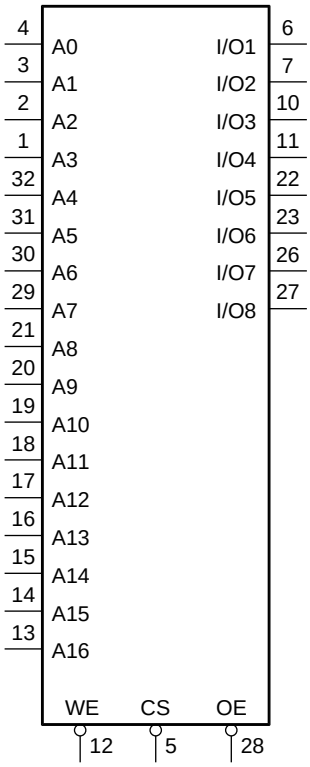
PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	A3	17	I	A12
2	I	A2	18	I	A11
3	I	A1	19	I	A10
4	I	A0	20	I	A9
5	I	$\overline{CS}$	21	I	A8
6	I/O	I/O1	22	I/O	I/O5
7	I/O	I/O2	23	I/O	I/O6
8	—	VDD	24	—	VDD
9	—	GND	25	—	GND
10	I/O	I/O3	26	I/O	I/O7
11	I/O	I/O4	27	I/O	I/O8
12	I	$\overline{WE}$	28	I	$\overline{OE}$
13	I	A16	29	I	A7
14	I	A15	30	I	A6
15	I	A14	31	I	A5
16	I	A13	32	I	A4

INPUT

A0 - A16 : ADDRESS INPUTS
$\overline{CS}$: CHIP SELECT
$\overline{OE}$: OUTPUT ENABLE INPUT
$\overline{WE}$: WRITE ENABLE INPUT

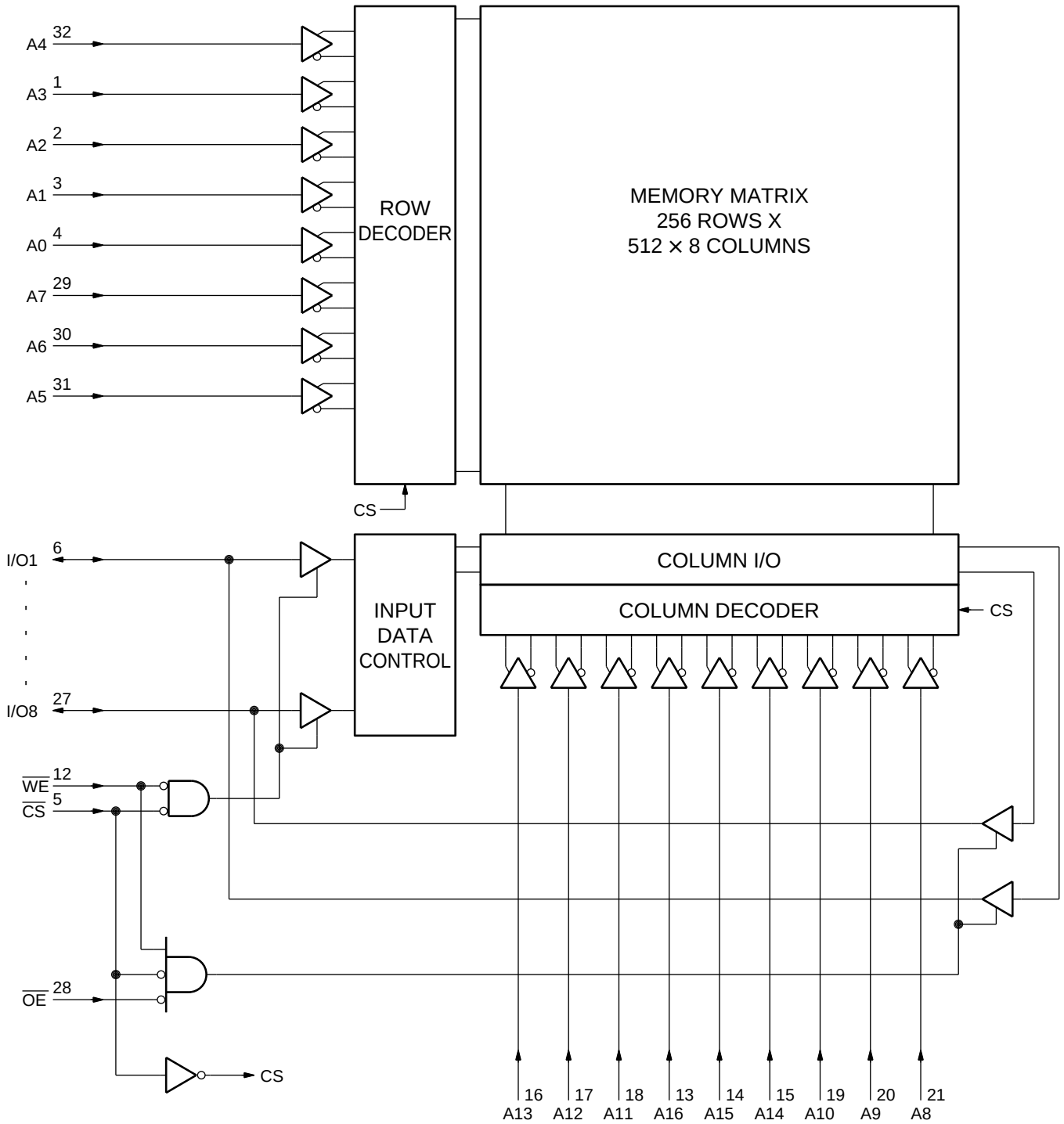
INPUT/OUTPUT

I/O1 - I/O8 : DATA INPUTS/OUTPUTS



$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O
1	×	×	NON SELECT	HI-Z
0	1	1	OUTPUT DISABLE	HI-Z
0	0	1	READ	OUTPUT
0	×	0	WRITE	INPUT

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE
HI-Z : HIGH IMPEDANCE


A4 32
A3 1
A2 2
A1 3
A0 4
A7 29
A6 30
A5 31
ROW DECODER
MEMORY MATRIX
256 ROWS X
512 × 8 COLUMNS
CS
I/O1 6
I/O8 27
INPUT DATA CONTROL
COLUMN I/O
COLUMN DECODER
CS
WE 12
CS 5
OE 28
CS
16 A13
17 A12
18 A11
13 A16
14 A15
15 A14
19 A10
20 A9
21 A8