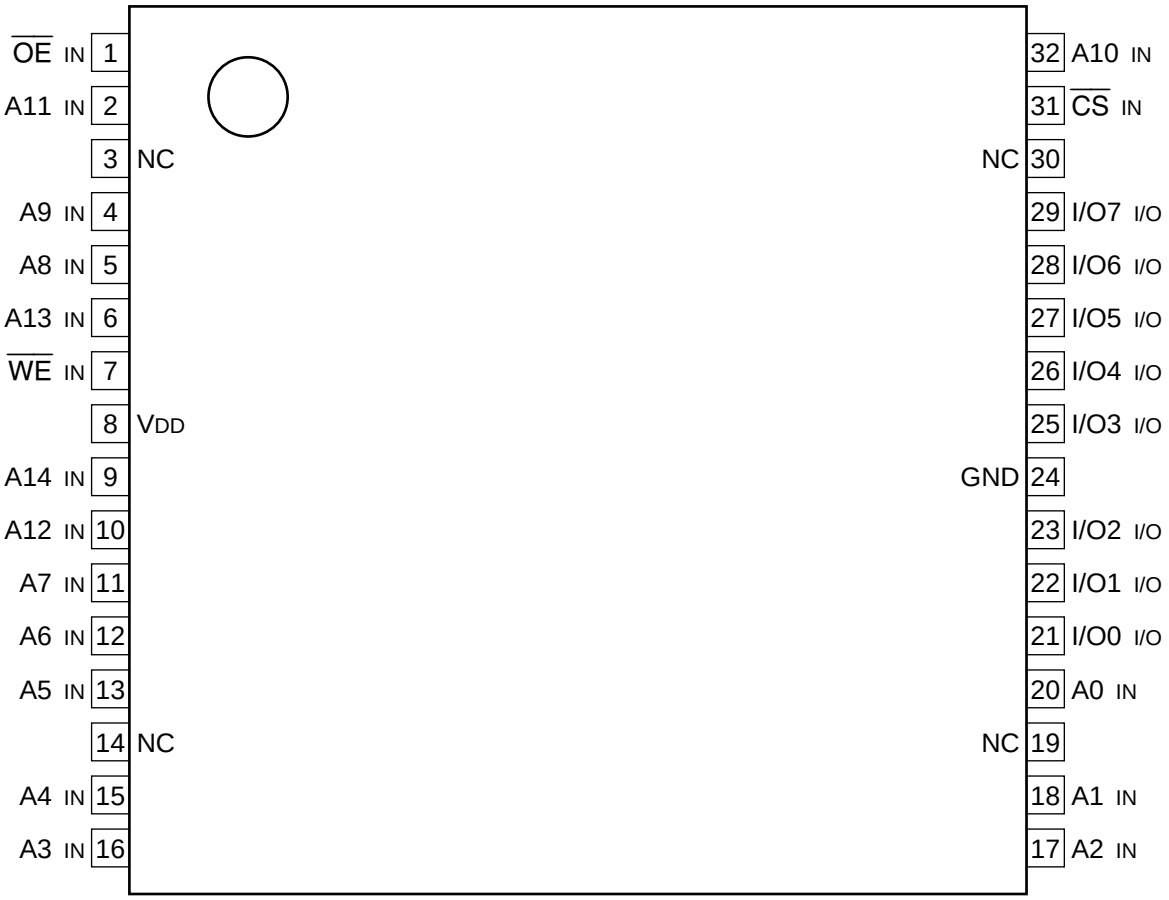
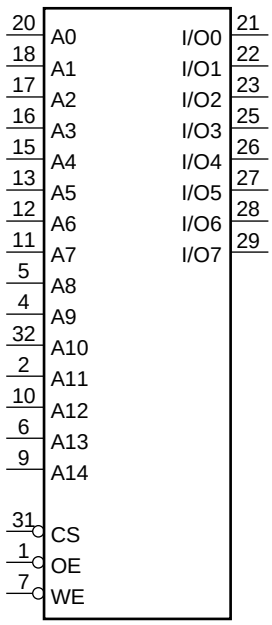
C-MOS SRAM

—TOP VIEW—

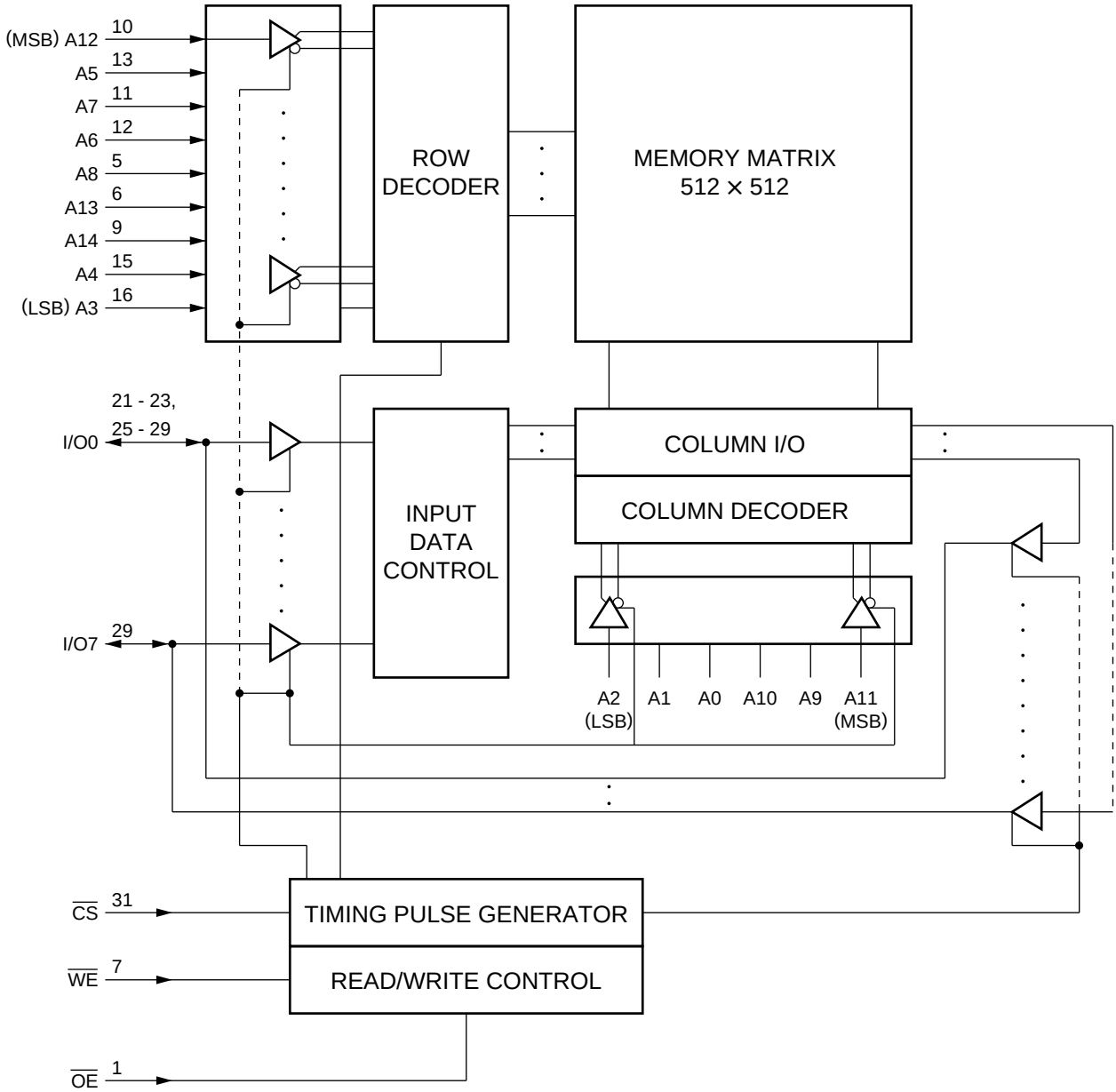




A0 - A14 : ADDRESS INPUTS
$\overline{CS}$: CHIP SELECT INPUT
I/O0 - I/O7 : DATA INPUTS/OUTPUTS
$\overline{OE}$: OUTPUT ENABLE INPUT
$\overline{WE}$: WRITE ENABLE INPUT

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O PIN
1	×	×	NO SELECTION	HI-Z
0	1	1	OUTPUT DISABLE	HI-Z
0	0	1	READ	DOUT
0	1	0	WRITE	DIN
0	0	0	WRITE	DIN

0 : LOW LEVEL
1 : HIGH LEVEL
× : DON'T CARE
HI-Z : HIGH IMPEDANCE


(MSB) A12
10
A5
13
A7
11
A6
12
A8
5
A13
6
A14
9
A4
15
(LSB) A3
16
ROW DECODER
MEMORY MATRIX 512 × 512
21 - 23, 25 - 29
I/O0
I/O7
29
INPUT DATA CONTROL
COLUMN I/O
COLUMN DECODER
A2 (LSB)
A1
A0
A10
A9
A11 (MSB)
CS
31
WE
7
OE
1
TIMING PULSE GENERATOR
READ/WRITE CONTROL