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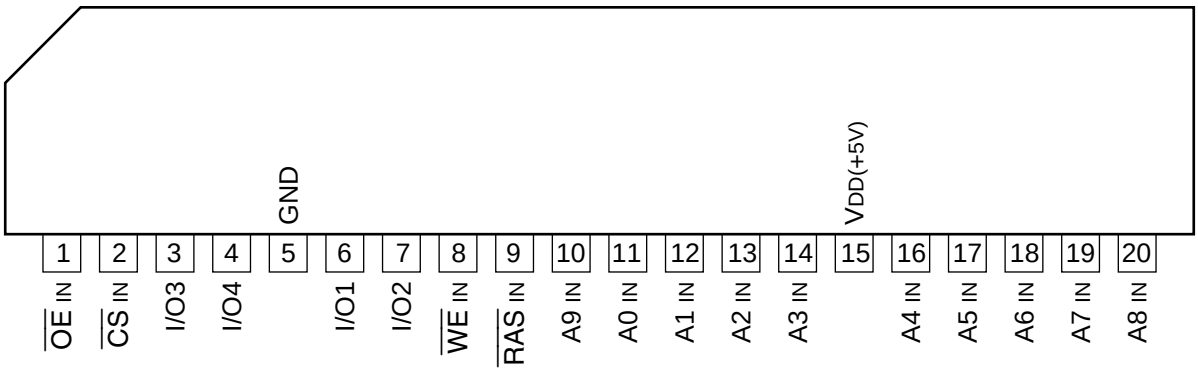
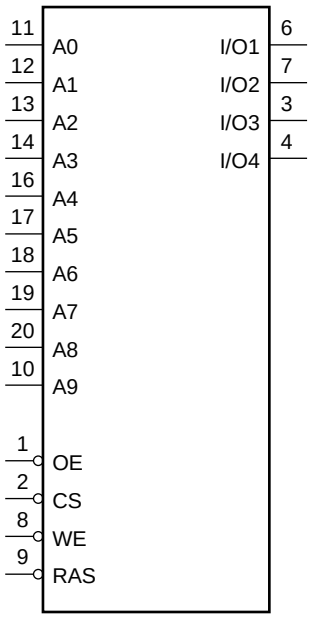
C-MOS 4M (1,048,576 × 4)-BIT DYNAMIC RAM

—SIDE VIEW—



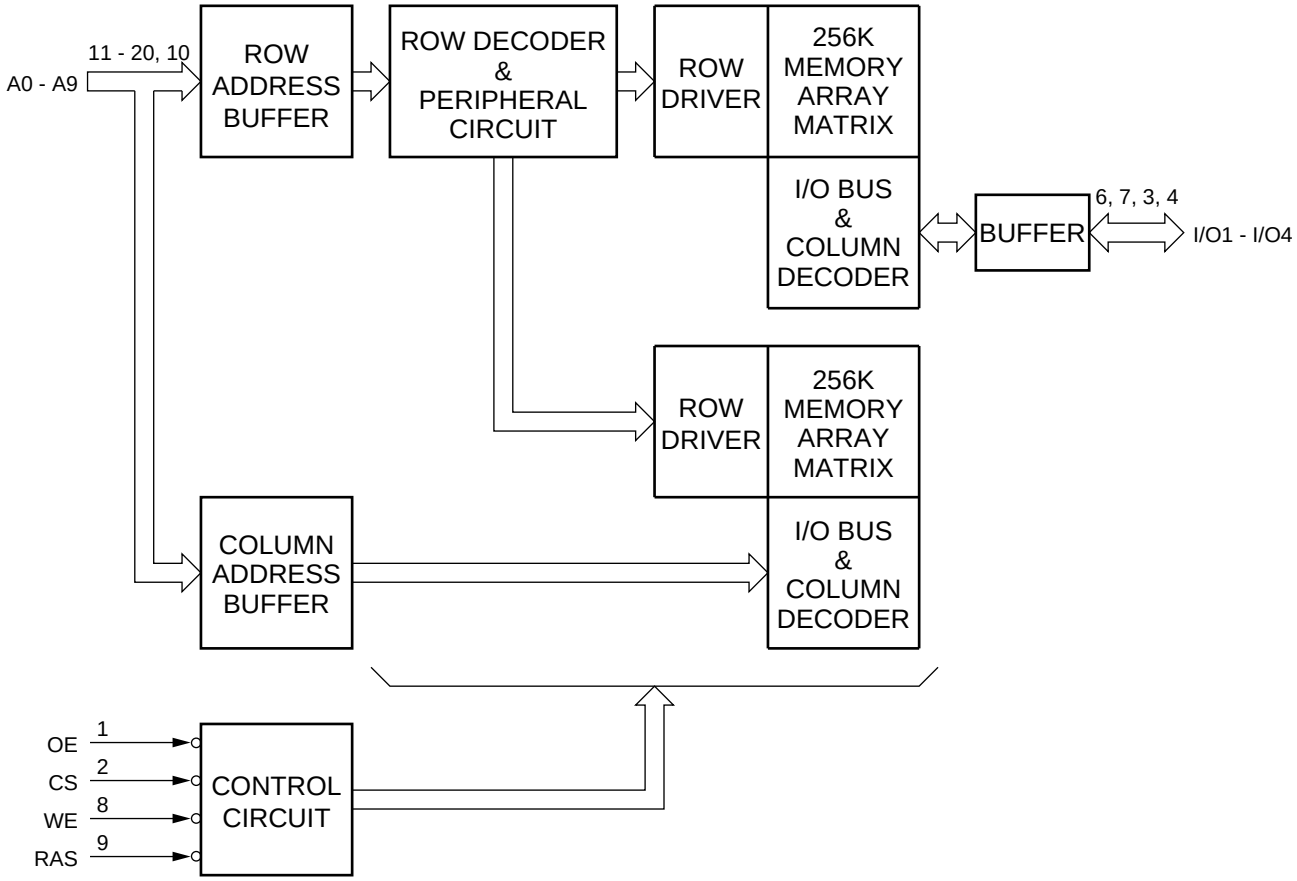


INPUT

A0 - A9	;	ADDRESS
$\overline{CS}$	;	CHIP SELECT
$\overline{OE}$	;	OUTPUT ENABLE
$\overline{RAS}$	;	ROW ADDRESS STROBE
$\overline{WE}$	;	READ/WRITE ENABLE

INPUT/OUTPUT

I/O1 - I/O4 ; DATA


11 - 20, 10
A0 - A9
ROW ADDRESS BUFFER
ROW DECODER & PERIPHERAL CIRCUIT
ROW DRIVER
256K MEMORY ARRAY MATRIX
I/O BUS & COLUMN DECODER
BUFFER
6, 7, 3, 4
I/O1 - I/O4
ROW DRIVER
256K MEMORY ARRAY MATRIX
COLUMN ADDRESS BUFFER
I/O BUS & COLUMN DECODER
OE
1
CS
2
WE
8
RAS
9
CONTROL CIRCUIT