INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4750V
LSI
Frequency synthesizer

Product specification
File under Integrated Circuits, IC04

January 1995

Philips
Semiconductors

PHILIPS

Frequency synthesizer

HEF4750V
LSI

DESCRIPTION

The HEF4750V frequency synthesizer is one of a pair of LOCMOS devices, primarily intended for use in high-performance frequency synthesizers, e.g. in all communication, instrumentation, television and broadcast applications. A combination of analogue and digital techniques results in an integrated circuit that enables high performance. The complementary device is the universal divider type HEF4751V.

Together with a standard prescaler, the two LOCMOS integrated circuits offer low-cost single loop synthesizers with full professional performance. Salient features offered (in combination with HEF4751V) are:

- Wide choice of reference frequency using a single crystal.
- High-performance phase comparator — low phase noise — low spurii.
- System operation to > 1 GHz.
- Typical 15 MHz input at 10 V.
- Flexible programming:
  - frequency offsets
  - ROM compatible
  - fractional channel capability.
- Programme range 6½ decades, including up to 3 decades of prescaler control.
- Division range extension by cascading.
- Built-in phase modulator.
- Fast lock feature.
- Out-of-lock indication.
- Low power dissipation and high noise immunity.

APPLICATION INFORMATION

Some examples of applications for the HEF4750V in combination with the HEF4751V are:

- VHF/UHF mobile radios.
- HF s.s.b. transceivers.
- Airborne and marine communications and navaids.
- Broadcast transmitters.
- High quality radio and television receivers.
- High performance citizens band equipment.
- Signal generators.

SUPPLY VOLTAGE

RATING	RECOMMENDED OPERATING
–0,5 to +15	9,5 to 10,5 V

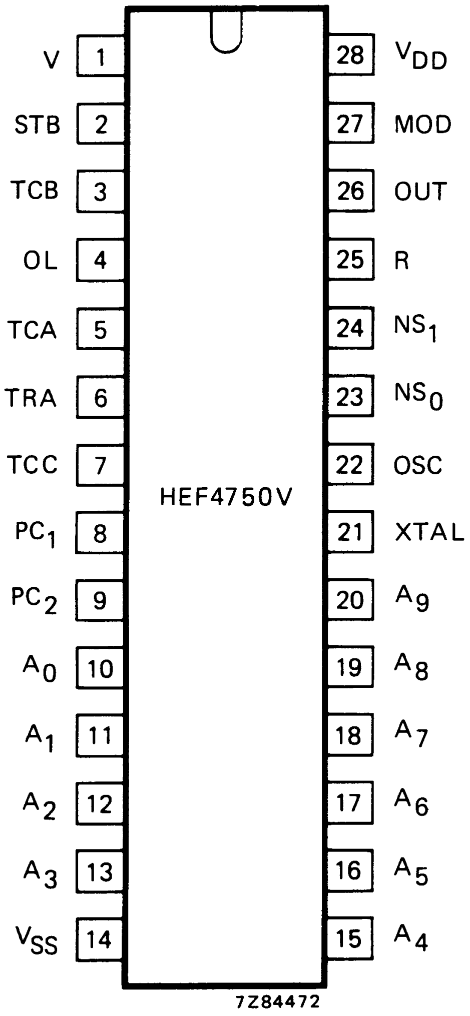


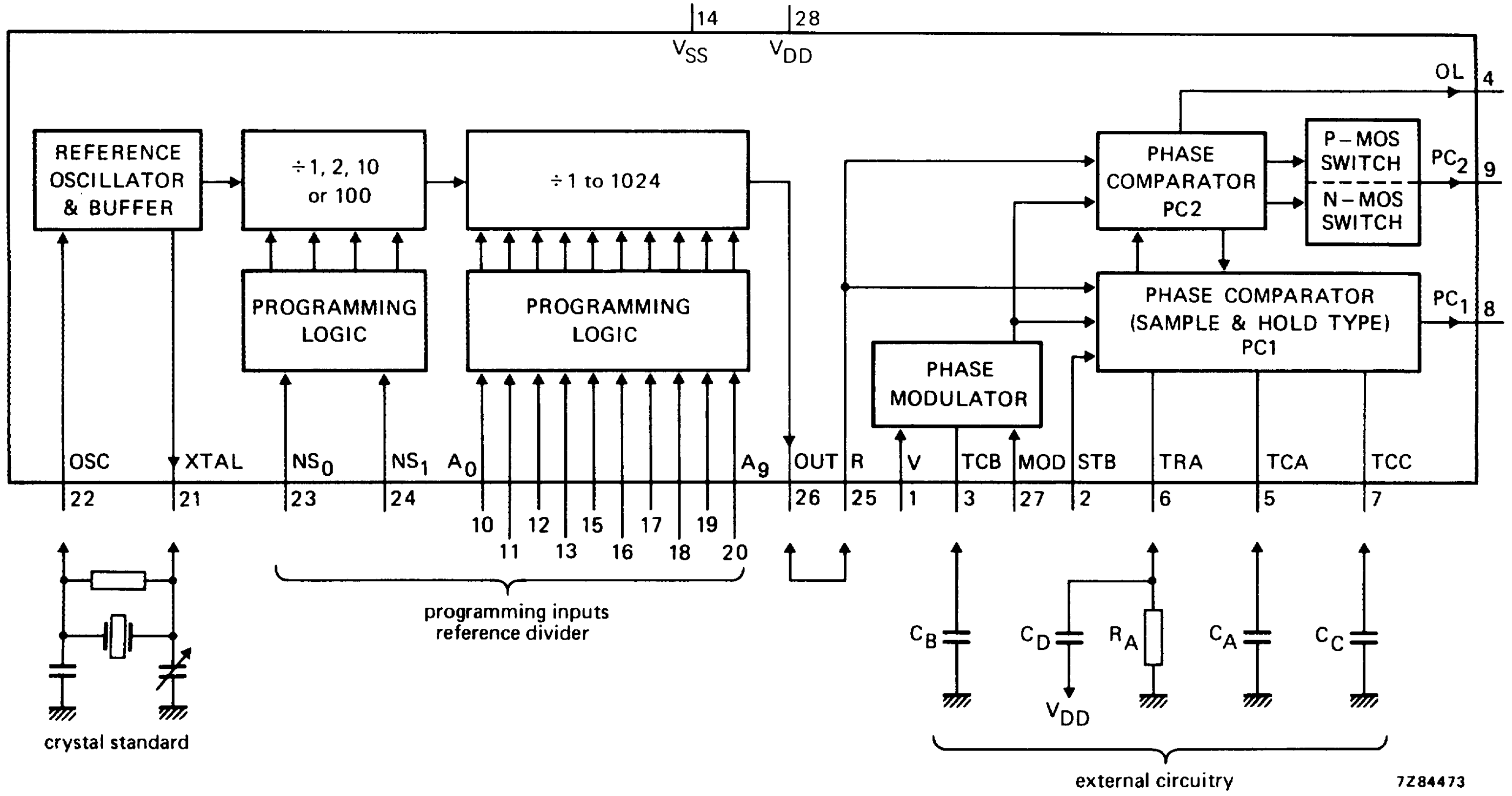
Fig.1 Pinning diagram.

HEF4750VD(F): 28-lead DIL; ceramic (cerdip) (SOT135)

( ): Package Designator North America

PINNING

R	phase comparator input, reference
V	phase comparator input
STB	strobe input
TCA	timing capacitor C_A pin
TCB	timing capacitor C_B pin
TCC	timing capacitor C_C pin
TRA	biasing pin (resistor R_A)
PC_1	analogue phase comparator output
PC_2	digital phase comparator output
MOD	phase modulation input
OL	out-of-lock indication
OSC	reference oscillator/buffer input
XTAL	reference oscillator/buffer output
A_0 to A_9	programming inputs/programmable divider
NS_0, NS_1	programming inputs, prescaler
OUT	reference divider output



N.B. PC_1 = analogue output; PC_2 = 3-state output.

Fig.2 Block diagram comprising five basic functions: phase comparator 1 (PC1), phase comparator 2 (PC2), phase modulator, reference oscillator and reference divider. These functions are described separately.

FUNCTIONAL DESCRIPTION

Phase comparator 1

Phase comparator 1 (PC1) is built around a SAMPLE and HOLD circuit. A negative-going transition at the V-input causes the hold capacitor (C_A) to be discharged and after a specified delay, caused by the Phase Modulator by means of an internal V' pulse, it produces a positive-going ramp. A negative-going transition at the R-input terminates the ramp. Capacitor C_A holds the voltage that the ramp has attained. Via an internal sampling switch this voltage is transferred to C_C and in turn buffered and made available at output PC_1.

If the ramp terminates before an R-input is present, an internal end of ramp (EOR) signal is produced.

These actions are illustrated in Fig.3.

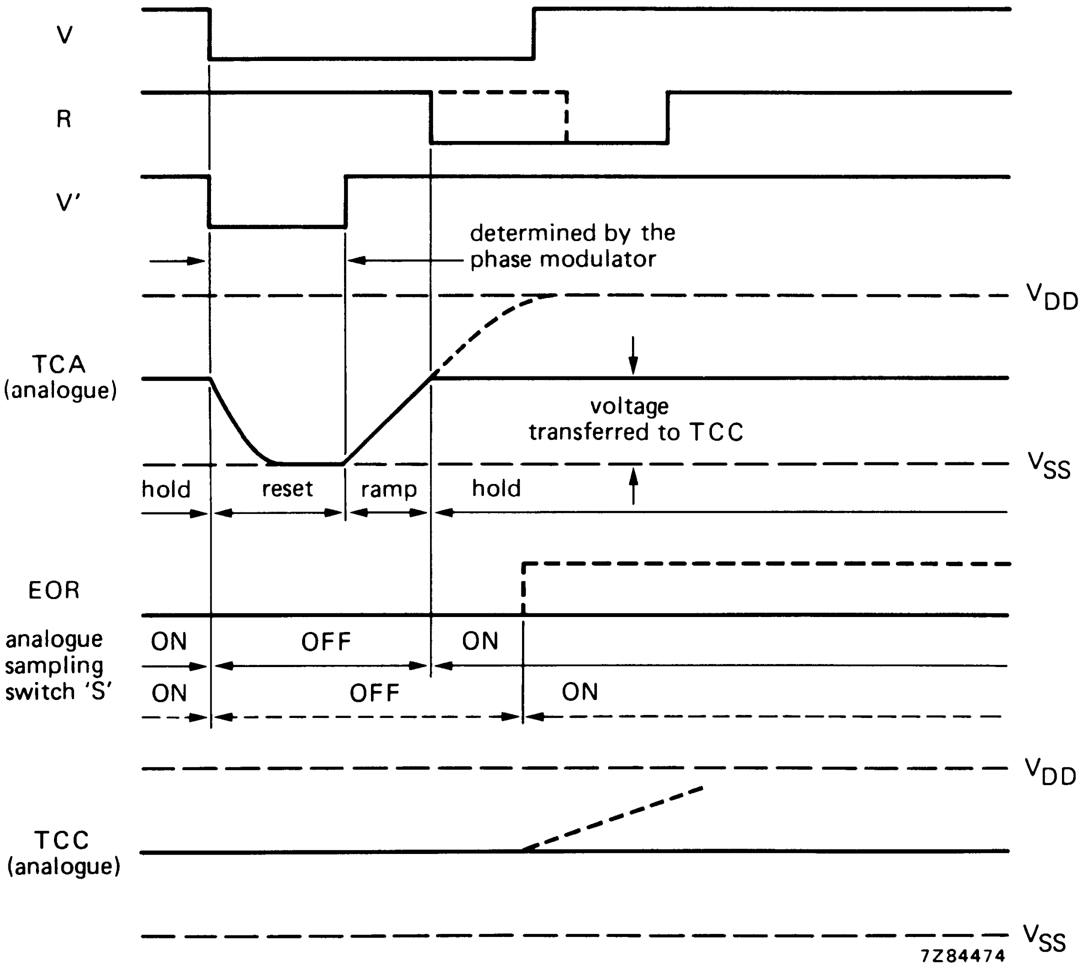


Fig.3 Waveforms associated with PC1.

The resultant phase characteristic is shown in Fig.4.

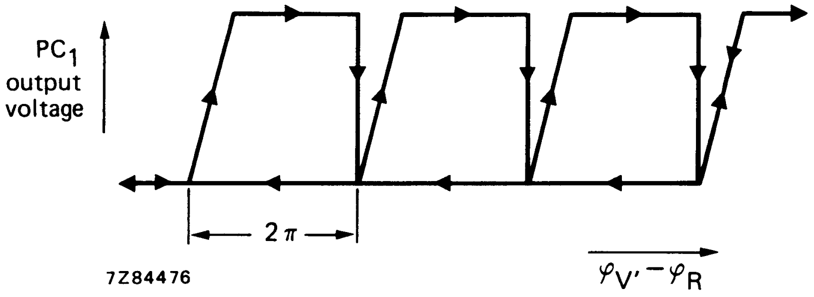


Fig.4 Phase characteristic of PC_1.

PC1 is designed to have a high gain, typically 3200 V/cycle (at 12,5 kHz). This enables a low noise performance.

Phase comparator 2

Phase comparator 2 (PC2) has a wide range, which enables faster lock times to be achieved than otherwise would be possible. It has a linear ± 360° phase range, which corresponds to a gain of typically 5 V/cycle.

This digital phase comparator has three stable states:

- reset state,
- V' leads R state,
- R leads V' state.

Conversion from one state to another takes place according to the state diagram of Fig.5.

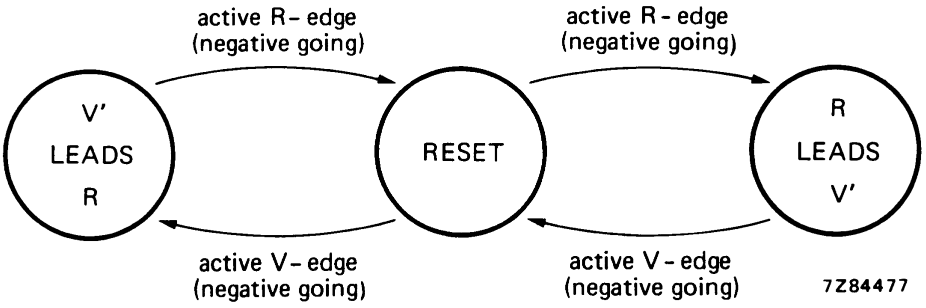


Fig.5 State diagram of PC2.

Output PC_2 produces positive or negative-going pulses with variable width; they depend on the phase relationship of R and V'. The average output voltage is a linear function of the phase difference. Output PC_2 remains in the high impedance OFF-state in the region in which PC1 operates. The resultant phase characteristic is shown in Fig.6.

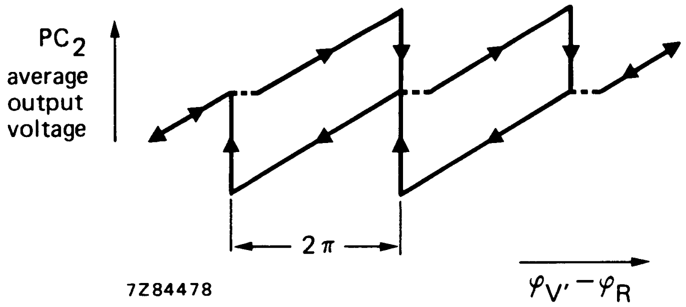


Fig.6 Phase characteristic of PC_2.

Strobe function

The strobe function is intended for applications requiring extremely fast lock times. In normal operation the additional strobe input (STB) can be connected to the V-input and the circuit will function as described in the previous sections.

In single, phase-locked-loop type frequency synthesizers, the comparison frequency generally used is either the nominal channel spacing or a sub-multiple. PC2 runs at the higher frequency (a higher reference frequency must also be used), whilst strobing takes place on the lower frequency, thereby obtaining a decrease in lock time. In a system using the Universal Divider HEF4751V, the output OFS cycles on the lower frequency, the output OFF cycles on the higher frequency.

Out-of-lock function

There are a number of situations in which the system goes from the locked to the out-of-lock state (OL goes HIGH):

1. When V' leads R, however out of the range of PC1.
2. When R leads V'.
3. When an R-pulse is missing.
4. When a V-pulse is missing.
5. When two successive STB-commands occur, the first without corresponding V-signal.

Phase modulator

The phase modulator only uses one external capacitor, C_B at pin TCB. A negative-going transition at the V-input causes C_B to produce a positive-going linear ramp. When the ramp has reached a value almost equal to the modulation input voltage (at MOD), the ramp terminates, C_B discharges and a start signal to the C_A-ramp at TCA is produced. A linear phase modulation is reached in this way. If no modulation is required, the MOD-input must be connected to a fixed voltage of a certain positive value up to V_{DD}. Care must be taken that the V' pulse is never smaller than the minimum value to ensure that the external capacitor of PC1 (C_A) can be discharged during that time. Since the V' pulse width is directly related to the TCB ramp duration, there is a requirement for the minimum value of this ramp duration.

Reference oscillator

The reference oscillator normally operates with an external crystal as shown in Fig.2. The internal circuitry can be used as a buffer amplifier in case an external reference should be required.

Reference divider

The reference divider consists of a binary divider with a programmable division ratio of 1 to 1024 and a prescaler with selectable division ratios of 1, 2, 10 and 100, according to the following tables:

Binary divider

N (A_0 TO A_9)	DIVISION RATIO
0	1024
$0 \leq N \leq 1023$	N

Prescaler

PROGRAMMING WORD (NS_0, NS_1)	DIVISION RATIO
0	1
1	2
2	10
3	100

In this way suitable comparison frequencies can be obtained from a range of crystal frequencies. The divider can also be used as a ‘stand alone’ programmable divider by connecting input TRA to V_{DD}, which causes all internal analogue currents to be switched off.

Biasing circuitry

The biasing circuitry uses an external current source or resistor, which has to be connected between the TRA and V_{SS} pins. This circuitry supplies all analogue parts of the circuit. Consequently the analogue properties of the device, such as gain, charge currents, speed, power dissipation, impedance levels etc., are mainly determined by the value of the input current at TRA. The TRA input must be decoupled to V_{DD}, as shown in Fig.7. The value of C_D has to be chosen such that the TRA input is ‘clean’, e.g. 10 nF at R_A = 68 kΩ.

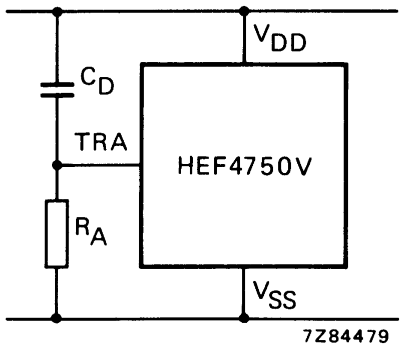


Fig.7 Decoupling of input TRA.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}		–0,5 to + 15	V
Voltage on any input	V_I		–0,5 to V_{DD} + 0,5	V
D.C. current into any input or output	± I	max.	10	mA
Power dissipation per package				
for T_{amb} = 0 to + 85 °C	P_{tot}	max.	500	mW
Power dissipation per output				
for T_{amb} = 0 to 85 °C	P	max.	100	mW
Storage temperature	T_{stg}		–65 to + 150	°C
Operating ambient temperature	T_{amb}		–40 to + 85	°C

DC CHARACTERISTICS

at V_{DD} = 10 V ± 5%; voltages are referenced to V_{SS} = 0 V, unless otherwise specified; for definitions see note 1.

PARAMETER	SYMBOL	T_{amb} (°C									UNIT	NOTES
		–40			+ 25			+ 85				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Quiescent device current	I_{DD}	–	–	100	–	–	100	–	–	750	µA	2
Input current; logic inputs, MOD	± I_{IN}	–	–	300	–	–	300	–	–	1000	nA	3
Output leakage current at ½ V_{DD}												3,4
TCA, hold-state	± I_Z	–	–	20	–	0,05	20	–	–	60	nA	
TCC, analogue switch OFF	± I_Z	–	–	20	–	0,05	20	–	–	60	nA	
PC_2, high impedance OFF-state	± I_Z	–	–	50	–	–	50	–	–	500	nA	
Logic input voltage												
LOW	V_{IL}	max. 0,3 V_{DD}									V	
HIGH	V_{IH}	max. 0,7 V_{DD}									V	
Logic output voltage												
LOW; at $\lvert I_O \rvert < 1$ µA	V_{OL}	–	–	50	–	–	50	–	–	50	mV	3
HIGH	V_{OH}	min. V_{DD} – 50 mV									mV	3
Logic output current LOW; at V_{OL} = 0,5 V												3
outputs OL, PC_2, OUT	I_{OL}	5,5	–	–	4,6	–	–	3,6	–	–	mA	
output XTAL	I_{OL}	2,8	–	–	2,4	–	–	1,9	–	–	mA	
Logic output current HIGH; at $V_{OH} = V_{DD}$ – 0,5 V												3
outputs OL, PC_2,OUT	$-I_{OH}$	1,5	–	–	1,3	–	–	1,0	–	–	mA	
output XTAL	$-I_{OH}$	1,4	–	–	1,2	–	–	0,9	–	–	mA	
Output TCC sink current	I_O	–	–	–	–	2,1	–	–	–	–	mA	3,4,5
Output TCC source current	$-I_O$	–	–	–	–	1,9	–	–	–	–	mA	3,4,6
Internal resistance of TCC $\lvert$output swing$\rvert$ ≤ 200 mV specified output range: 0,3 V_{DD} to 0,7 V_{DD}	R_i	–	–	–	–	0,7	–	–	–	–	kΩ	3,4

PARAMETER	SYMBOL	T_{amb} (°C									UNIT	NOTES
		–40			+ 25			+ 85				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Output TCC voltage with respect to TCA input voltage	ΔV	–	0	–	–	0	–	–	0	–	V	3,4,7
Output PC_1 sink current	I_O	–	–	–	–	1,1	–	–	–	–	mA	3,4,8
Output PC_1 source current	$-I_O$	–	–	–	–	1,0	–	–	–	–	mA	3,4,9
Internal resistance of PC_1 $\lvert$output swing$\rvert$ ≤ 200 mV specified output range: 0,3 V_{DD} to 0,7 V_{DD}	R_i	–	–	–	–	1,4	–	–	–	–	kΩ	3,4
Output PC_1 voltage with respect to TCC input voltage	ΔV	–	0	–	–	0	–	–	0	–	V	3,4,10
EOR generation $V_{EOR} = V_{DD} - V_{TCA}$	V_{EOR}	–	0,9	–	–	0,7	–	–	0,6	–	V	3,4,11
Source current; HIGH at $V_{OUT} = \frac{1}{2} V_{DD}$; output in ramp mode												3,4
TCA	I_O	–	–	–	–	13	–	–	–	–	mA	
TCB	I_O	–	–	–	–	2,5	–	–	–	–	mA	

AC CHARACTERISTICS

General note

The dynamic specifications are given for the circuit built-up with external components as given in Fig.8, under the following conditions; for definitions see note 1; for definitions of times see Fig.19; V_{DD} = 10 V ± 5%; T_{amb} = 25 °C; input transition times ≤ 20 ns; R_A = 68 kΩ ± 30% (see also note 4); C_A = 270 pF; C_B = 150 pF; C_C = 1 nF; C_D = 10 nF; unless otherwise specified.

	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS	NOTES
Slew rate							
TCA	S_{TCA}	–	52	–	V/μs	R_A = minimum	12
TCA	S_{TCA}	–	28	–	V/μs	R_A = maximum	12
TCB	S_{TCB}	–	20	–	V/μs	R_A = minimum	12
TCB	S_{TCB}	–	10	–	V/μs	R_A = maximum	12
Ramp linearity							
TCA	l_{TCA}	–	2	–	%		13
TCB	l_{TCB}	–	2	–	%		13
Start of TCA-ramp delay	t_{CBCA}	–	200	–	ns		
Delay of TCA-hold	t_{RCA}	–	40	–	ns		
Delay of TCA-discharge	t_{VCA}	–	60	–	ns		
Start of TCB-ramp delay	t_{VCB}	–	60	–	ns		
TCB-ramp duration	t_{rCB}	–	250	–	ns	V_{MOD} = 4 V	
	t_{rCB}	–	350	–	ns	V_{MOD} = 6 V	
	t_{rCB}	–	450	–	ns	V_{MOD} = 8 V	
Required TCB min. ramp duration	t_{rCB}	–	150	–	ns		14
Pulse width							
V : LOW	t_{PWVL}	–	20	–	ns		
V : HIGH	t_{PWVH}	–	20	–	ns		
R : LOW	t_{PWRL}	–	20	–	ns		
R : HIGH	t_{PWRH}	–	20	–	ns		
STB : LOW	t_{PWSL}	–	20	–	ns		
STB : HIGH	t_{PWSH}	–	20	–	ns		
Fall time							
TCA	t_{fCA}	–	50	–	ns		
TCB	t_{fCB}	–	50	–	ns		
Prescaler input frequency	f_{PR}	–	30	–	MHz	all division ratios	
Binary divider frequency	f_{DIV}	–	30	–	MHz	all division ratios	
Crystal oscillator frequency	f_{OSC}	–	10	–	MHz		
Average power supply current						locked state	
with speed-up 1 : 10	I_P	–	3,6	–	mA		15
without speed-up	I_P	–	3,2	–	mA		16

Notes

1. Definitions:
   R_A = external biasing resistor between pins TRA and V_{SS}; 68 kΩ ± 30%.
   C_A = external timing capacitor for time/voltage converter, between pins TCA and V_{SS}.
   C_B = external timing capacitor for phase modulator, between pins TCB and V_{SS}.
   C_C = external hold capacitor between pins TCC and V_{SS}.
   C_D = decoupling capacitor between pins TRA and V_{DD}.
   Logic inputs: V, R, STB, A_0 to A_9, NS_0, NS_1, OSC.
   Logic outputs: OL, PC_2, XTAL, OUT.
   Analogue signals: TCA, TCB, TCC, TRA, PC_1, MOD.
2. TRA at V_{DD}; TCA, TCB, TCC and MOD at V_{SS}; logic inputs at V_{SS} or V_{DD}.
3. All logic inputs at V_{SS} or V_{DD}.
4. R_A connected; its value chosen such that I_{TRA} = 100 μA.
5. The analogue switch is in the ON position (see Fig.9).
6. The analogue switch is in the ON position (see Fig.10).
7. See Fig.11.
   This guarantees the d.c. voltage gain, combined with d.c.-offset.
   Input condition: $0,3\ V_{DD} \leq V_{TCA} \leq 0,7\ V_{DD}$.
   $\Delta V = V_{TCC} - V_{TCA}$.
8. See Fig.12.
9. See Fig.13.
10. See Fig.14.
    This guarantees the d.c. voltage gain, combined with d.c.-offset.
    Input condition: $0,3\ V_{DD} \leq V_{TCC} \leq 0,7\ V_{DD}$.
    $\Delta V = V_{PC1} - V_{TCC}$.
11. Switching level at TCA, generating an EOR-signal, during increasing input voltage.
12. See Fig.15.
13. See Fig.16.
    Definition of the ramp linearity at full swing.
14. The external components and modulation input voltage must be chosen such that this requirement will be fulfilled, to ensure that C_A is sufficiently discharged during that time.
15. See Fig.17.
    Circuit connections for power supply current specification, with speed-up 1 : 10. V and R are in the range of PC1, such that the output voltage at PC_1 is equal to 5 V.
    f_{OSC} = 5 MHz (external clock)
    f_{STB} = 12,5 kHz
    f_V = 125 kHz
16. See Fig.18.
    Circuit connections for power supply current specification, without speed-up. V and R are in the range of PC1, such that the output voltage at PC_1 is equal to 5 V.
    f_{OSC} = 5 MHz (external clock)
    f_{STB} = 12,5 kHz
    f_V = 12,5 kHz

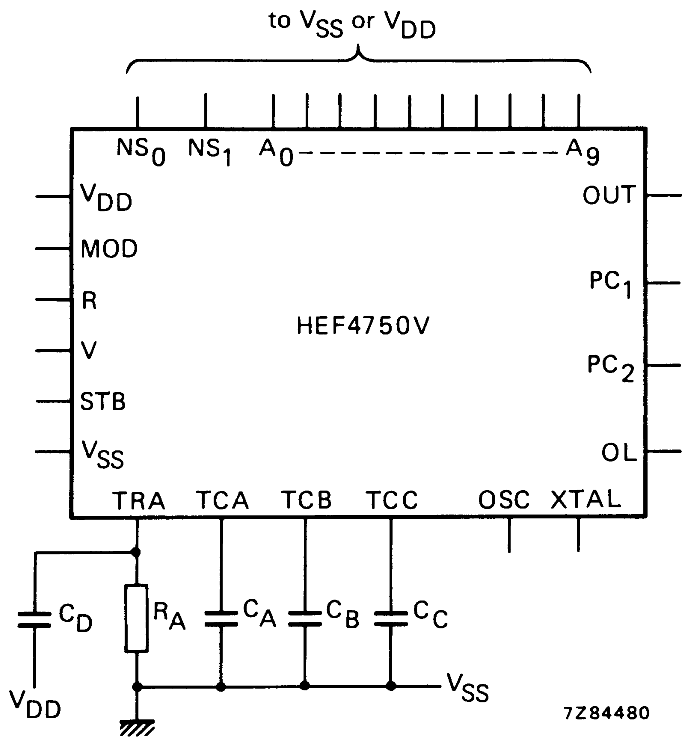


Fig.8 Test circuit for measuring a.c. characteristics.

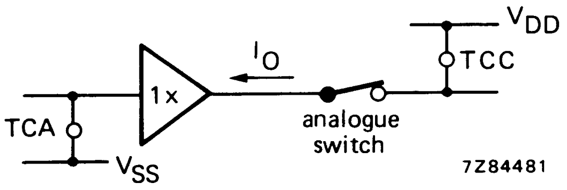


Fig.9 Equivalent circuit for note 5.

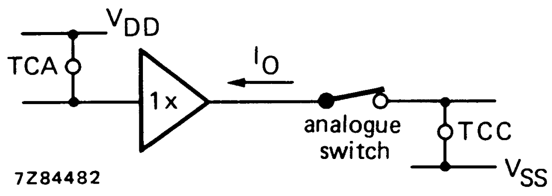


Fig.10 Equivalent circuit for note 6.

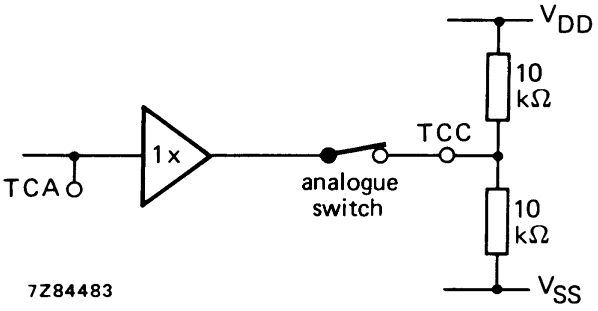


Fig.11 Circuit for note 7.

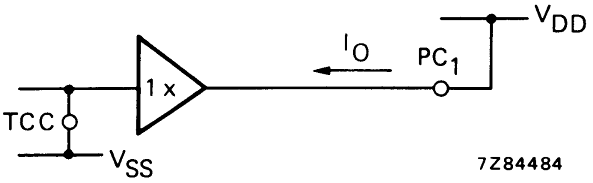


Fig.12 Equivalent circuit for PC_1 sink current.

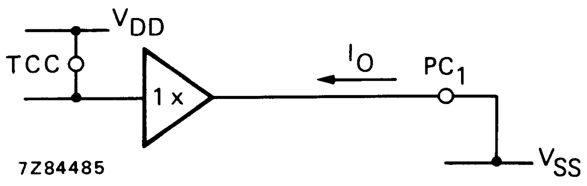


Fig.13 Equivalent circuit for PC_1 source current.

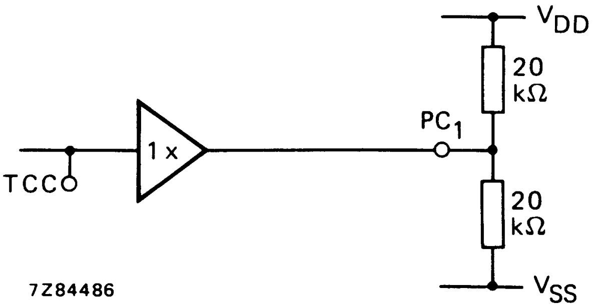


Fig.14 Circuit for note 10.

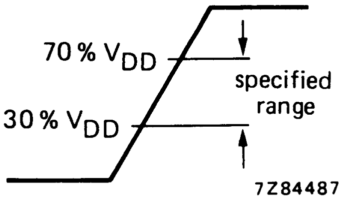
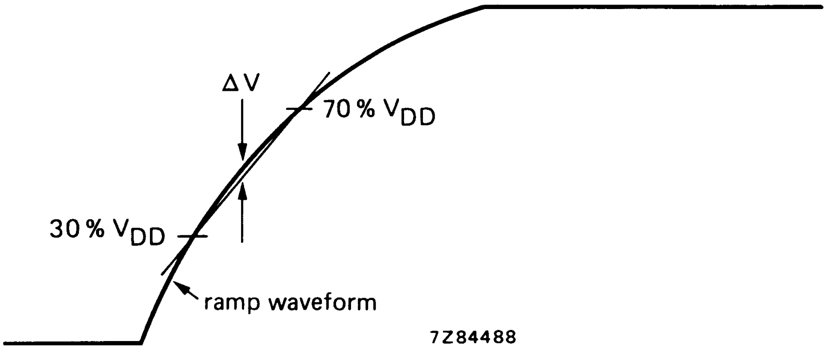


Fig.15 Waveform at the output.



$$\text{Linearity} = \frac{\Delta V}{1/2\ V_{DD}} \times 100\%.$$

Fig.16 Definition of the ramp linearity at full swing.
ΔV is the maximum deviation of the ramp waveform to the straight line, which joins the 30% V_{DD} and 70% V_{DD} points.

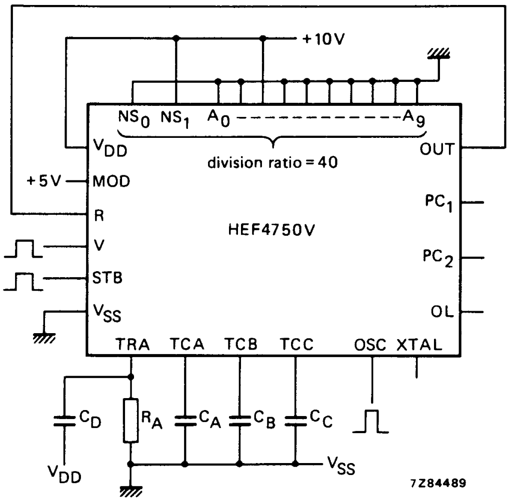


Fig.17 Circuit for note 15.

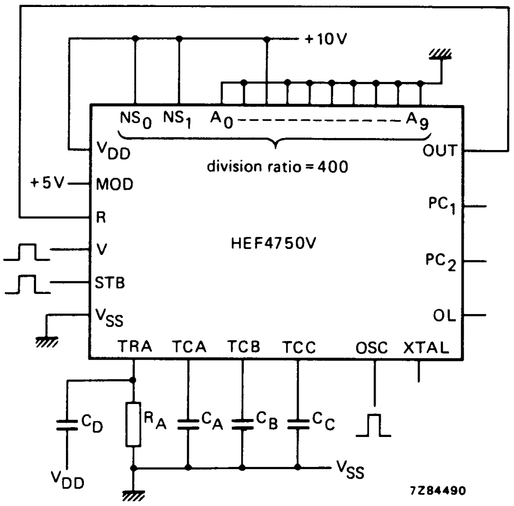
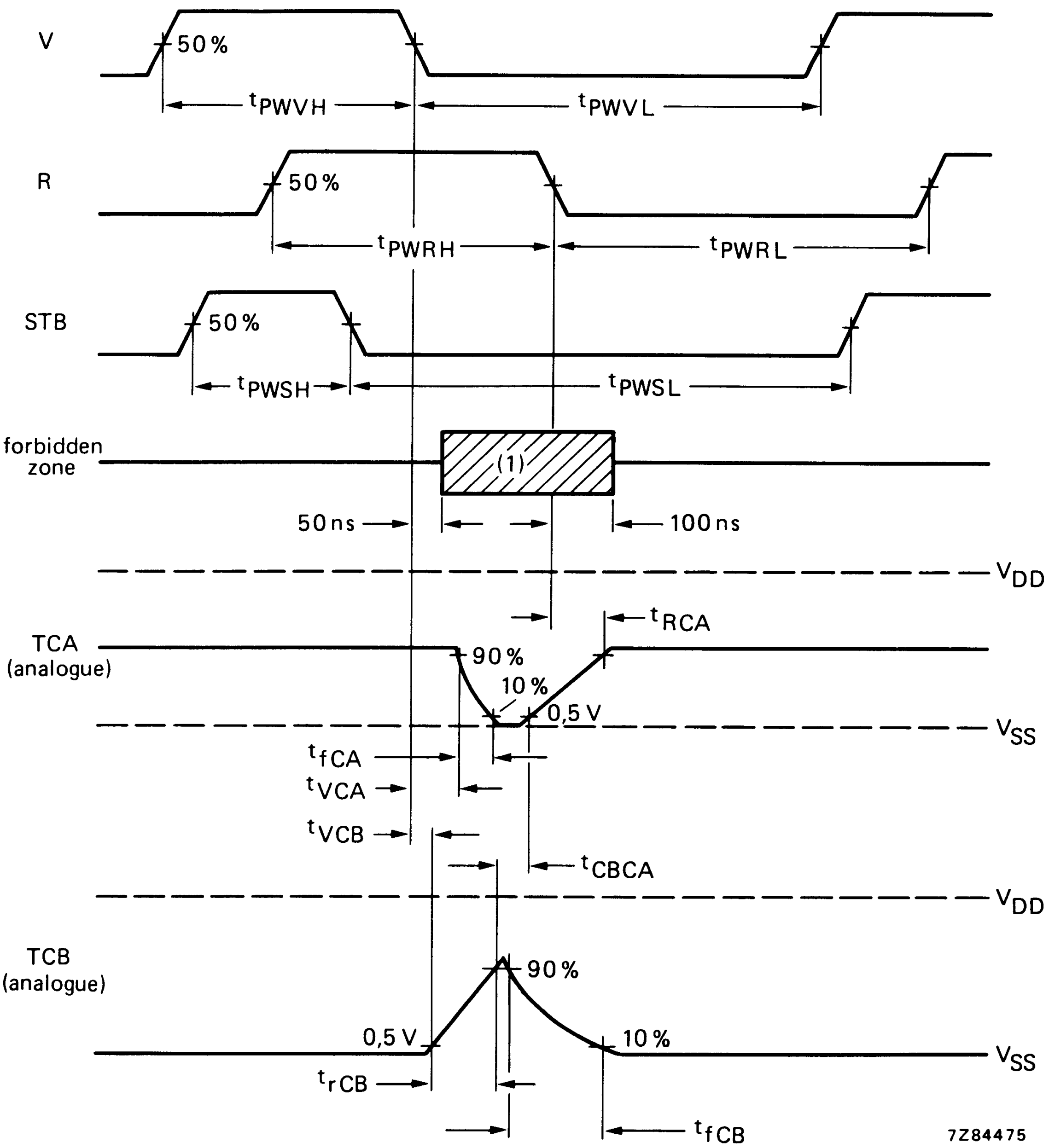


Fig.18 Circuit for note 16.



(1) Forbidden zone in the *locked state* for the positive edge of V and R and both edges of STB.

Fig.19 Waveforms showing times in the locked state.

APPLICATION INFORMATION

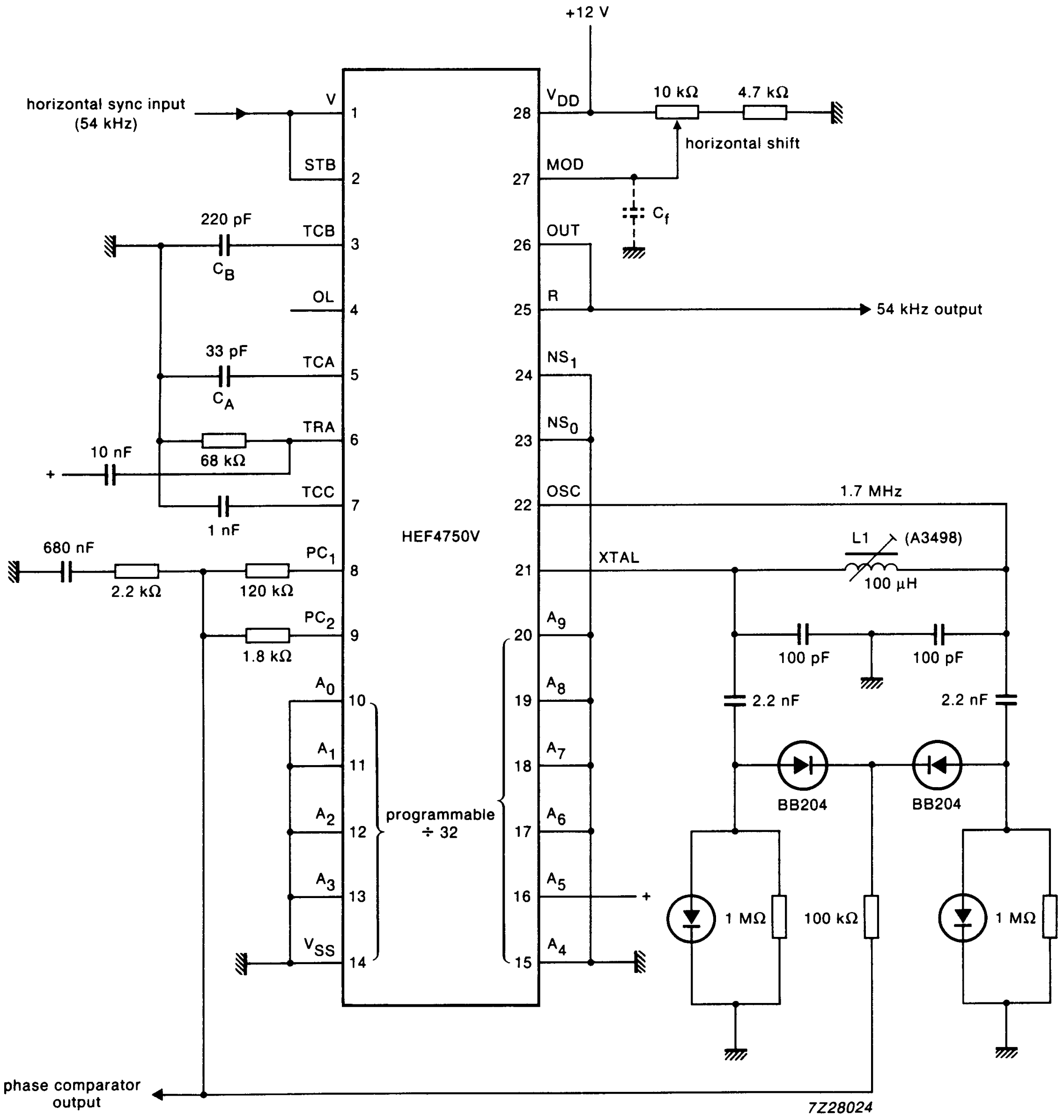


Fig.20 Application of HEF4750V as horizontal sync circuit with Phase-Locked Loop (PLL) and LC oscillator with vari-cap control.