

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOC莫斯 HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOC莫斯 HE4000B Logic Package Outlines/Information HEF, HEC

HEF4532B MSI 8-input priority encoder

Product specification
File under Integrated Circuits, IC04

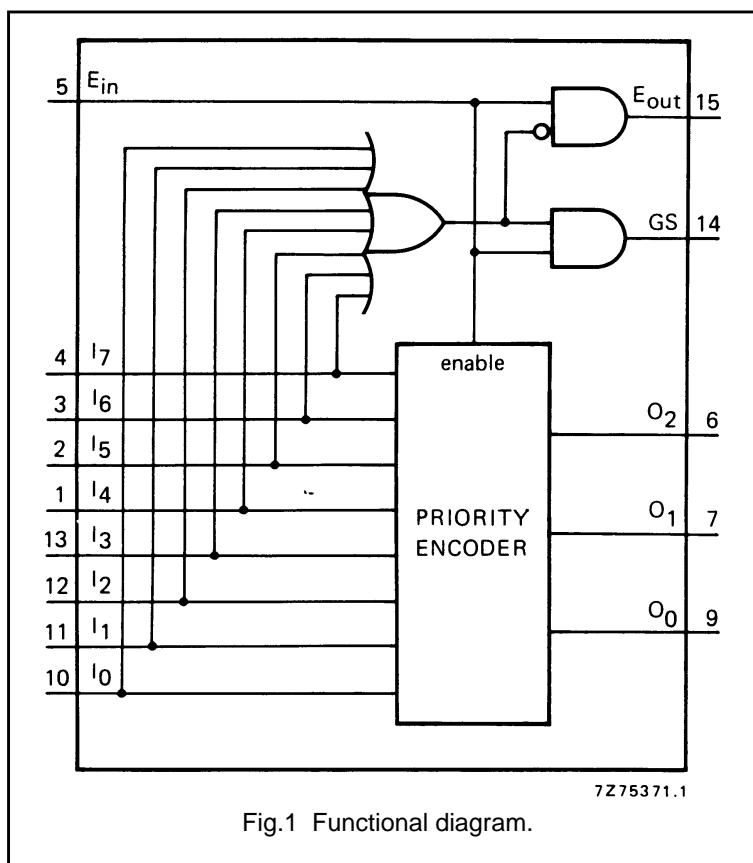
January 1995

**HEF4532B
MSI**
8-input priority encoder
DESCRIPTION

The HEF4532B is an 8-input priority encoder with eight active HIGH priority inputs (I_0 to I_7), three active HIGH outputs (O_0 to O_2), an active HIGH enable input (E_{in}), an active HIGH enable output (E_{out}) and an active HIGH group select output (GS).

Data is accepted on inputs I_0 to I_7 . The binary code

corresponding to the highest priority input (I_0 to I_7) which is HIGH, is generated on O_0 to O_2 if E_{in} is HIGH. Input I_7 is assigned the highest priority. GS is HIGH when one or more priority inputs and E_{in} are HIGH. E_{out} is HIGH when I_0 to I_7 are LOW and E_{in} is HIGH. E_{in} , when LOW, forces all outputs (O_0 to O_2 , GS, E_{out}) LOW.



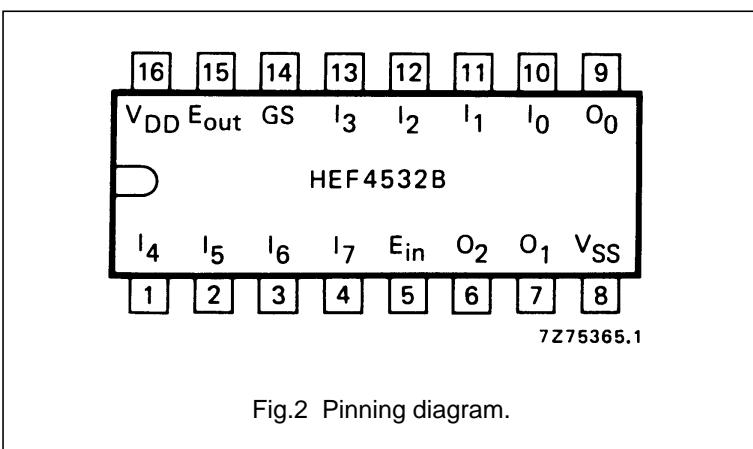
- HEF4532BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4532BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4532BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

I_0 to I_7	priority inputs
E_{in}	enable input
E_{out}	enable output
GS	group select output
O_0 to O_2	outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications



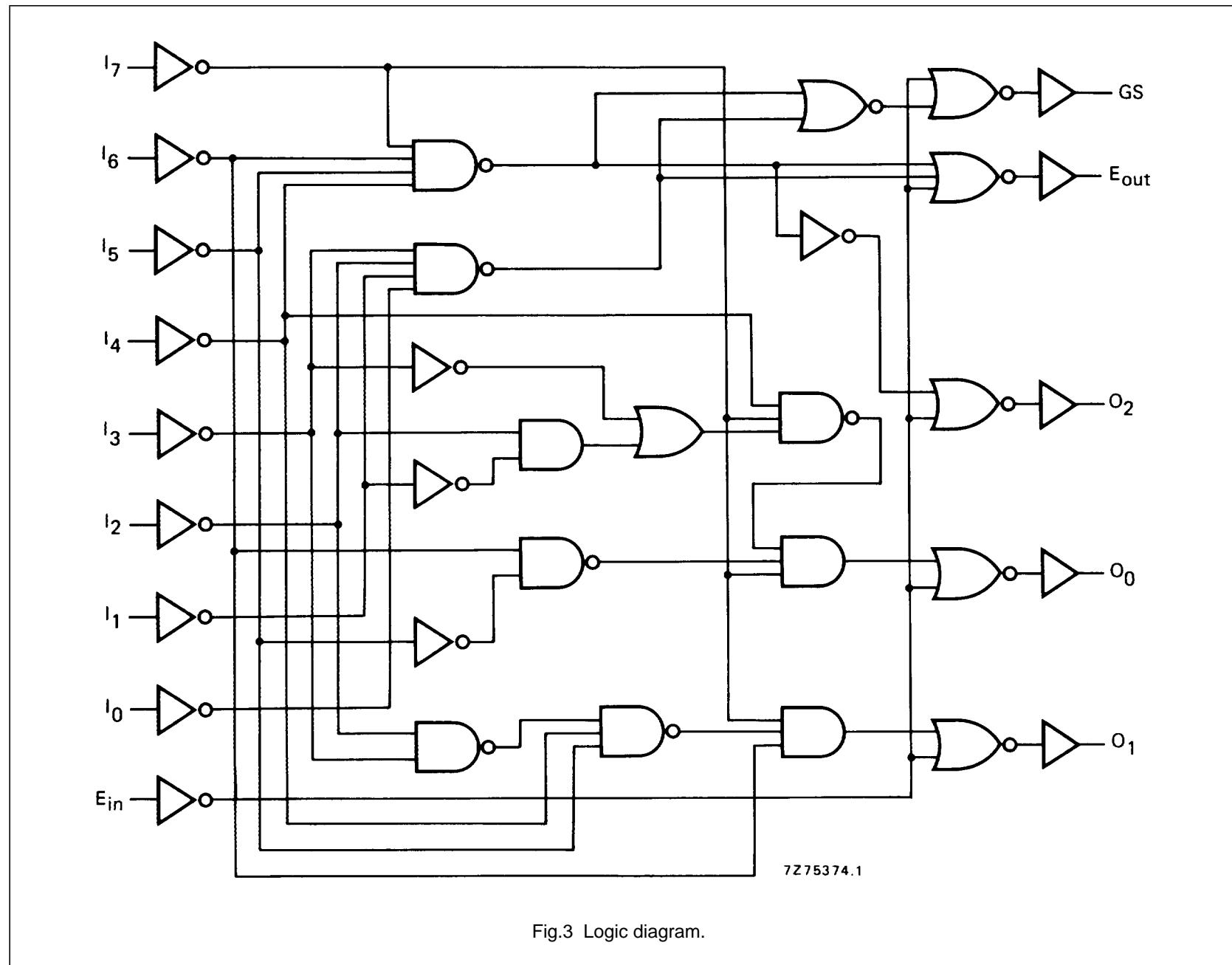


Fig.3 Logic diagram.

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TRUTH TABLE

INPUTS									OUTPUTS				
E_{in}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	O_2	O_1	O_0	E_{out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial

LOGIC EQUATIONS

$$\begin{aligned}
 O_2 &= E_{in} \cdot (I_4 + I_5 + I_6 + I_7) \\
 O_1 &= E_{in} \cdot (I_2 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_5 + I_6 + I_7) \\
 O_0 &= E_{in} \cdot (I_1 \cdot \bar{I}_2 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_3 \cdot \bar{I}_4 \cdot \bar{I}_6 + I_5 \cdot \bar{I}_6 + I_7) \\
 E_{out} &= E_{in} \cdot \bar{I}_0 \cdot \bar{I}_1 \cdot \bar{I}_2 \cdot \bar{I}_3 \cdot \bar{I}_4 \cdot \bar{I}_5 \cdot \bar{I}_6 \cdot \bar{I}_7 \\
 GS &= E_{in} \cdot (I_0 + I_1 + I_2 + I_3 + I_4 + I_5 + I_6 + I_7)
 \end{aligned}$$

AC CHARACTERISTICS

 $V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

		V_{DD} V	TYPICAL FORMULA FOR P (μ W)	
Dynamic power dissipation per package (P)	5		$1\ 620 f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10		$6\ 600 f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15		$15\ 970 f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

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AC CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$; see also waveforms Fig.4

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays	E _{in} → E _{out} HIGH to LOW	t _{PHL}	95	190	ns	68 ns + (0,55 ns/pF) C _L
			10	45	ns	34 ns + (0,23 ns/pF) C _L
			15	35	70	27 ns + (0,16 ns/pF) C _L
	LOW to HIGH	t _{PLH}	5	80	ns	53 ns + (0,55 ns/pF) C _L
			10	35	70	24 ns + (0,23 ns/pF) C _L
			15	30	60	22 ns + (0,16 ns/pF) C _L
	E _{in} → GS HIGH to LOW	t _{PHL}	5	85	ns	58 ns + (0,55 ns/pF) C _L
			10	45	ns	34 ns + (0,23 ns/pF) C _L
			15	35	70	27 ns + (0,16 ns/pF) C _L
	LOW to HIGH	t _{PLH}	5	80	ns	53 ns + (0,55 ns/pF) C _L
			10	40	80	29 ns + (0,23 ns/pF) C _L
			15	30	60	22 ns + (0,16 ns/pF) C _L
	E _{in} → O _n HIGH to LOW	t _{PHL}	5	80	ns	53 ns + (0,55 ns/pF) C _L
			10	40	80	29 ns + (0,23 ns/pF) C _L
			15	30	60	22 ns + (0,16 ns/pF) C _L
	LOW to HIGH	t _{PLH}	5	85	ns	58 ns + (0,55 ns/pF) C _L
			10	40	80	29 ns + (0,23 ns/pF) C _L
			15	30	60	22 ns + (0,16 ns/pF) C _L
	I _n → O _n HIGH to LOW	t _{PHL}	5	115	230	88 ns + (0,55 ns/pF) C _L
			10	50	100	39 ns + (0,23 ns/pF) C _L
			15	35	70	27 ns + (0,16 ns/pF) C _L
	LOW to HIGH	t _{PLH}	5	115	230	88 ns + (0,55 ns/pF) C _L
			10	50	100	39 ns + (0,23 ns/pF) C _L
			15	35	70	27 ns + (0,16 ns/pF) C _L
	I _n → GS HIGH to LOW	t _{PHL}	5	115	230	88 ns + (0,55 ns/pF) C _L
			10	50	100	39 ns + (0,23 ns/pF) C _L
			15	40	80	32 ns + (0,16 ns/pF) C _L
	LOW to HIGH	t _{PLH}	5	115	230	88 ns + (0,55 ns/pF) C _L
			10	50	100	39 ns + (0,23 ns/pF) C _L
			15	40	80	32 ns + (0,16 ns/pF) C _L
Output transition times	HIGH to LOW	t _{THL}	5	60	120	10 ns + (1,0 ns/pF) C _L
			10	30	60	9 ns + (0,42 ns/pF) C _L
			15	20	40	6 ns + (0,28 ns/pF) C _L
	LOW to HIGH	t _{TLH}	5	60	120	10 ns + (1,0 ns/pF) C _L
			10	30	60	9 ns + (0,42 ns/pF) C _L
			15	20	40	6 ns + (0,28 ns/pF) C _L

8-input priority encoder

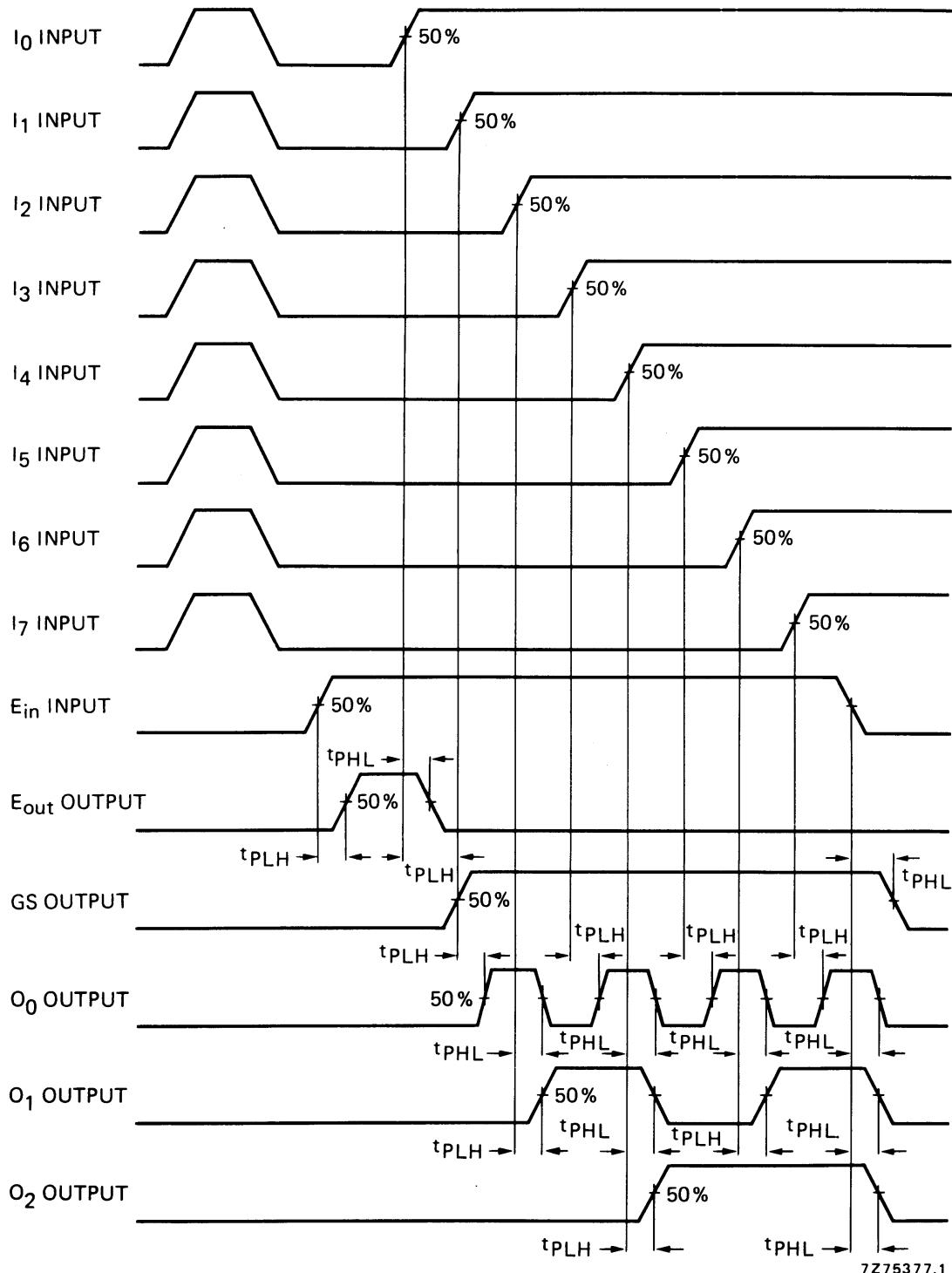
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Fig.4 Waveforms showing propagation delays from inputs to outputs.

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APPLICATION INFORMATION

Some examples of applications for the HEF4532B are:

- Priority encoder
- Keyboard encoder

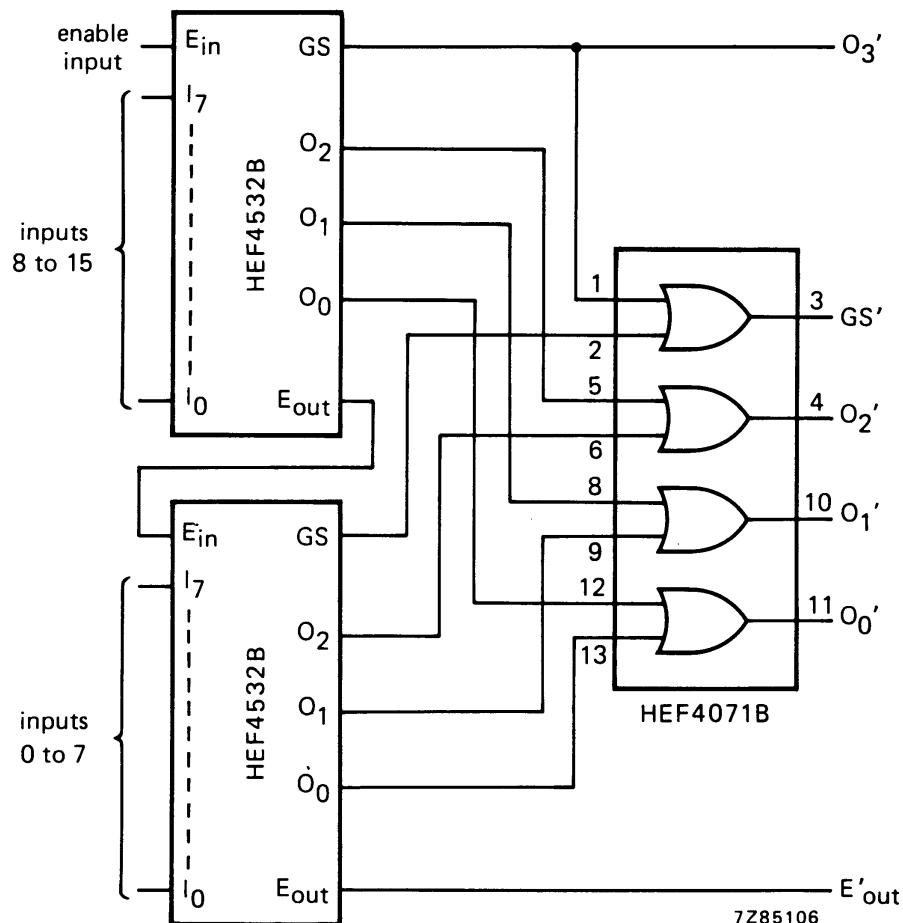


Fig.5 16-level priority encoder.

8-input priority encoder

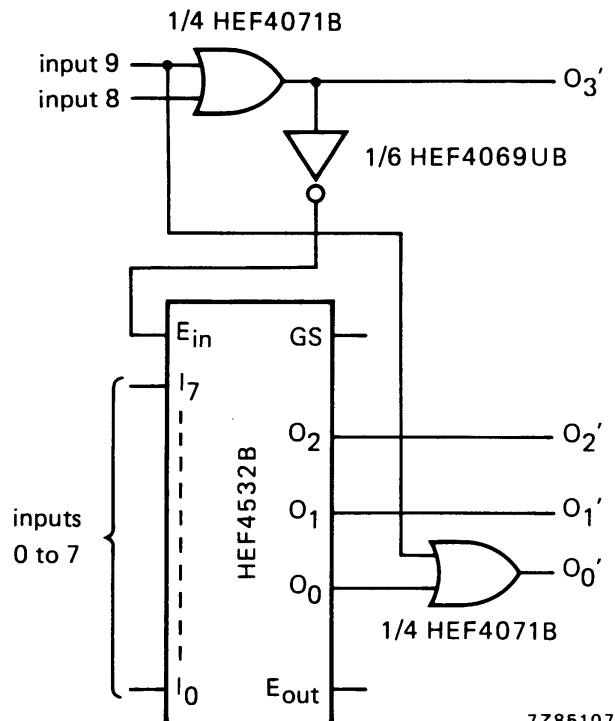
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Fig.6 0-to-9 keyboard encoder.

TRUTH TABLE (for Fig.6)

INPUTS										OUTPUTS				
9	8	7	6	5	4	3	2	1	0	GS	O_3'	O_2'	O_1'	O_0'
H	X	X	X	X	X	X	X	X	X	L	H	L	L	H
L	H	X	X	X	X	X	X	X	X	L	H	L	L	L
L	L	H	X	X	X	X	X	X	X	H	L	H	H	H
L	L	L	H	X	X	X	X	X	X	H	L	H	L	H
L	L	L	L	H	X	X	X	X	X	H	L	H	L	L
L	L	L	L	L	H	X	X	X	X	H	L	H	L	H
L	L	L	L	L	L	H	X	X	X	H	L	H	L	L
L	L	L	L	L	L	L	H	X	X	H	L	H	L	L

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial