DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4511B
MSI
BCD to 7-segment latch/decoder/driver

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

BCD to 7-segment latch/decoder/driver

HEF4511B MSI

DESCRIPTION

The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D_A to D_D), an active LOW latch enable input ($\overline{EL}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH n-p-n bipolar transistor segment outputs (O_a to O_g).

When $\overline{EL}$ is LOW, the state of the segment outputs (O_a to O_g) is determined by the data on D_A to D_D.
When $\overline{EL}$ goes HIGH, the last data present on D_A to D_D are stored in the latches and the segment outputs remain stable. When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.

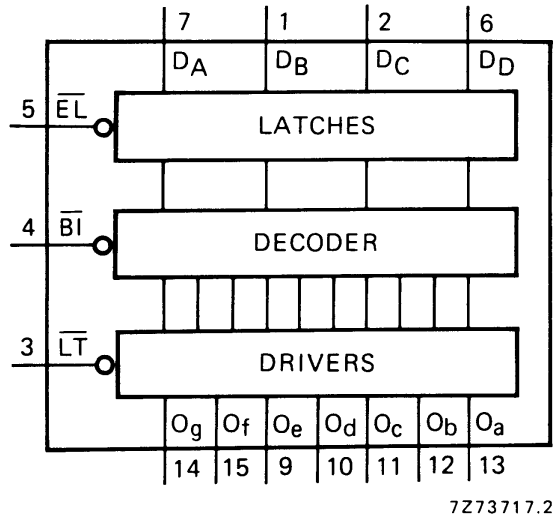


Fig.1 Functional diagram.

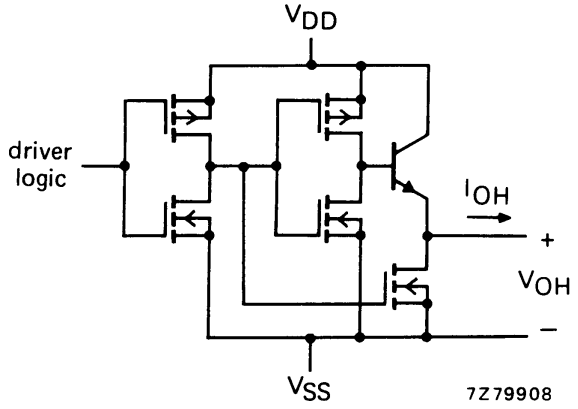


Fig.3 Schematic diagram of output stage.

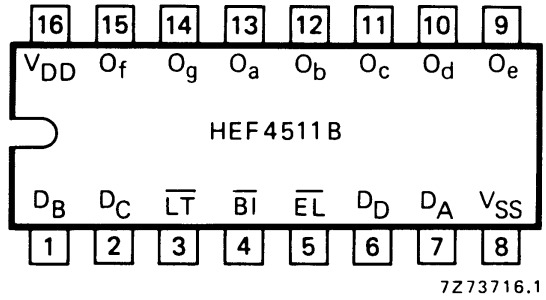


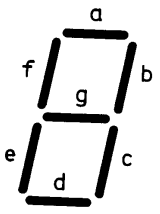
Fig.2 Pinning diagram.

HEF4511BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4511BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4511BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

D_A to D_D	address (data) inputs
$\overline{EL}$	latch enable input (active LOW)
$\overline{BI}$	ripple blanking input (active LOW)
$\overline{LT}$	lamp test input (active LOW)
O_a to O_g	segment outputs

Fig.4 Segment designation.



FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

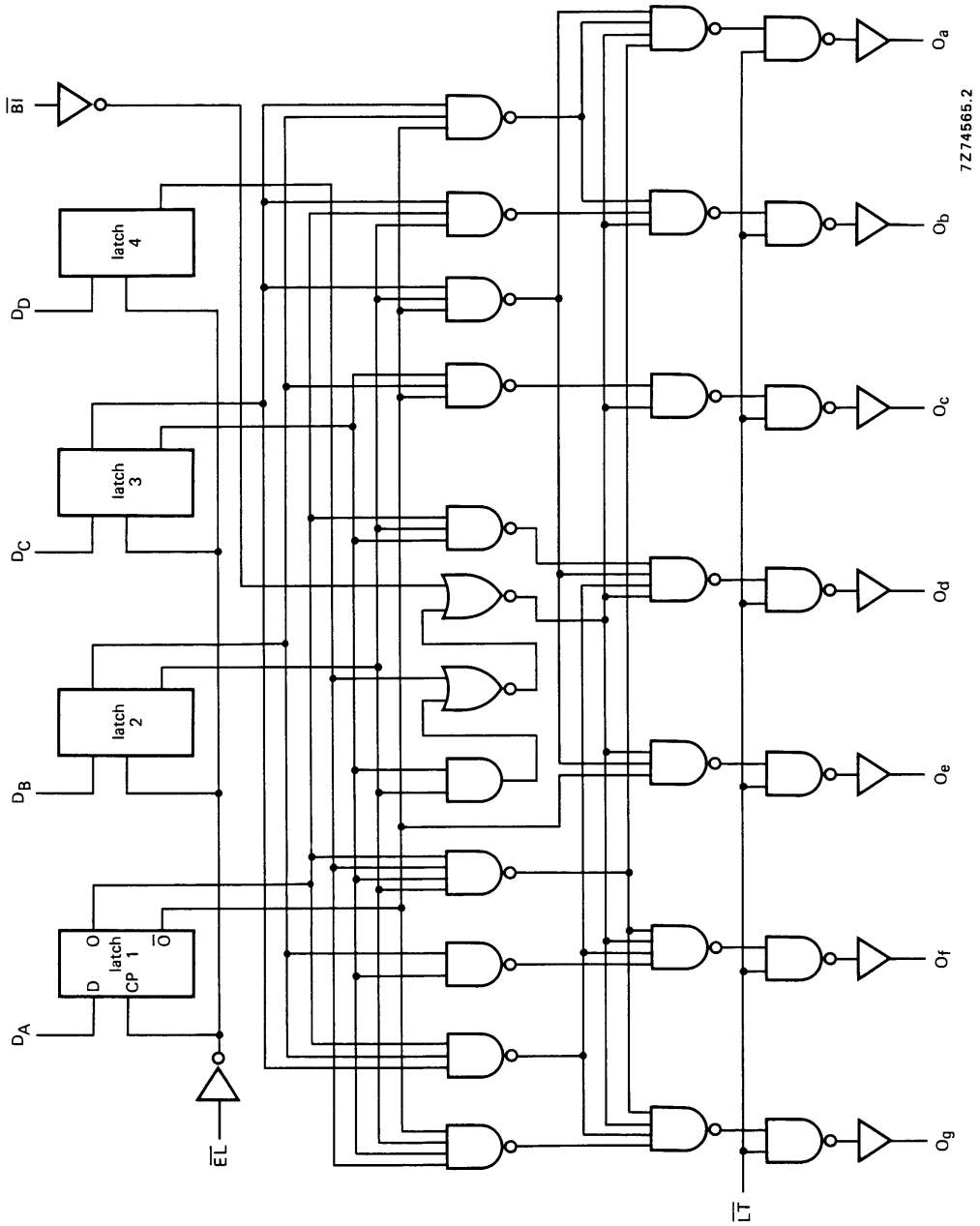


Fig.5 Logic diagram; for one latch see Fig.6.

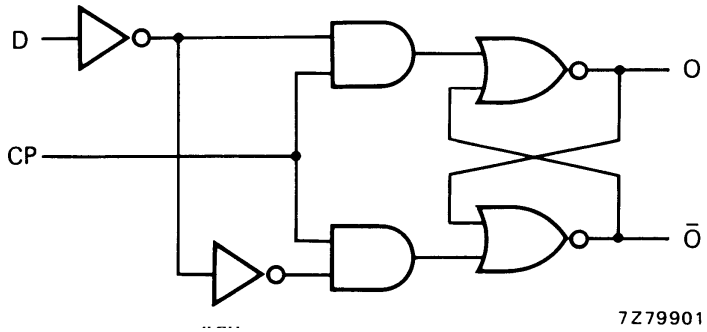


Fig.6 Logic diagram (one latch); see also Fig.5.

FUNCTION TABLE

INPUTS							OUTPUTS							
$\overline{EL}$	$\overline{BI}$	$\overline{LT}$	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	DISPLAY
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X				*				*

Note

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   * Depends upon the BCD code applied during the LOW to HIGH transition of $\overline{EL}$.

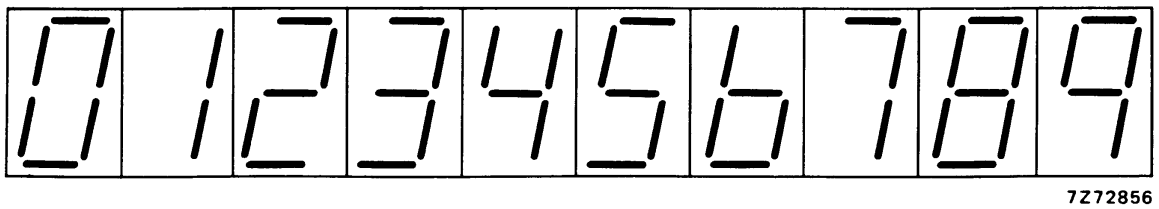


Fig.7 Display.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134).

Output (source) current HIGH	$-I_{OH}$	max.	25	mA

For other RATINGS see Family Specifications.

Note

1. A destructive high current mode may occur if V_I and V_O are not constrained to the range $V_{SS} \leq V_I$ or $V_O \leq V_{DD}$.

DC CHARACTERISTICS

V_{SS} = 0 V

HEF	V_{DD} V	I_{OH} mA	SYMBOL	T_{amb} (°C)						
				−40		+ 25		+ 85		
				MIN.	MAX.	MIN.	TYP.	MIN.	MAX.	
Output voltage	5	0		4,10		4,10	4,40	4,10		V
HIGH	10	0	V_{OH}	9,10		9,10	9,40	9,10		V
	15	0		14,10		14,10	14,40	14,10		V
Output voltage	5	5					4,20			V
HIGH	10	5	V_{OH}				9,20			V
	15	5					14,20			V
Output voltage	5	10		3,60		3,60	4,05	3,30		V
HIGH	10	10	V_{OH}	8,75		8,75	9,10	8,45		V
	15	10		13,75		13,75	14,10	13,45		V
Output voltage	5	15					4,00			V
HIGH	10	15	V_{OH}				9,00			V
	15	15					14,00			V
Output voltage	5	20		2,80		2,80	3,80	2,50		V
HIGH	10	20	V_{OH}	8,10		8,10	9,00	7,80		V
	15	20		13,10		13,10	14,00	12,80		V
Output voltage	5	25					3,70			V
HIGH	10	25	V_{OH}				8,90			V
	15	25					14,00			V

HEC	V_{DD} V	I_{OH} mA	SYMBOL	T_{amb} (°C)						
				−55		+ 25		+ 125		
				MIN.	MAX.	MIN.	TYP.	MIN.	MAX.	
Output voltage	5	0		4,10		4,10	4,40	4,10		V
HIGH	10	0	V_{OH}	9,10		9,10	9,90	9,10		V
	15	0		14,10		14,10	14,40	14,40		V
Output voltage	5	5					4,30			V
HIGH	10	5	V_{OH}				9,30			V
	15	5					14,30			V
Output voltage	5	10		3,60		3,60	4,25	3,20		V
HIGH	10	10	V_{OH}	8,75		8,75	9,25	8,35		V
	15	10		13,75		13,75	14,25	13,35		V
Output voltage	5	15					4,20			V
HIGH	10	15	V_{OH}				9,20			V
	15	15					14,20			V
Output voltage	5	20		2,80		2,80	4,20	2,30		V
HIGH	10	20	V_{OH}	8,10		8,10	9,20	7,60		V
	15	20		13,10		13,10	14,20	12,60		V
Output voltage	5	25					4,15			V
HIGH	10	25	V_{OH}				9,20			V
	15	25					14,20			V

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

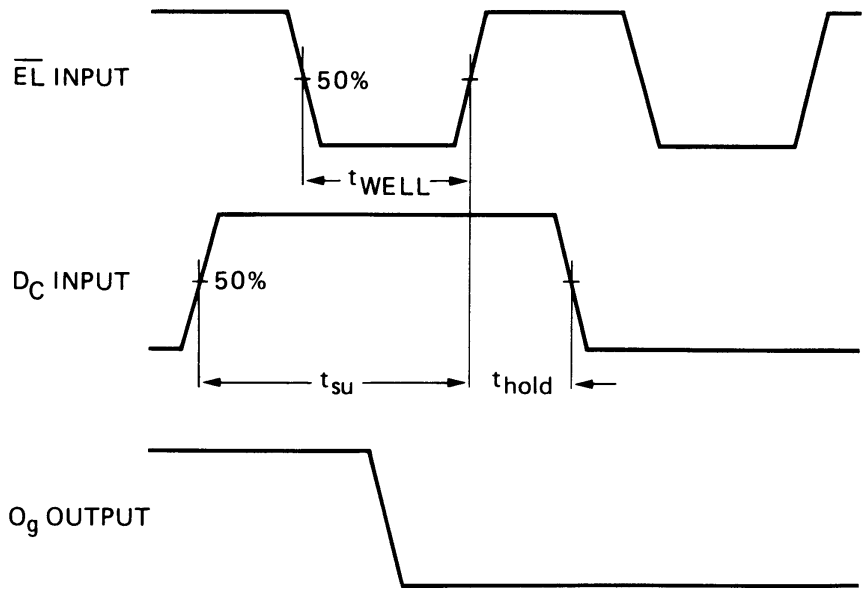
	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$1\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10	$4\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$10\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$D_n \rightarrow O_n$	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			135	270	ns	108 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{EL} \rightarrow O_n$	5			160	320	ns	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			160	320	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$\overline{BI} \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{BI} \rightarrow O_n$	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{LT} \rightarrow O_n$	5			80	160	ns	52 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			20	40	ns	12 ns + (0,16 ns/pF) C_L
	5			60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Output transition times	5			60	120	ns	10 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
	5			25	50	ns	20 ns + (1,0 na/pF) C_L
LOW to HIGH	10	t_{TLH}		16	32	ns	13 ns + (0,06 ns/pF) C_L
	15			13	26	ns	10 ns + (0,06 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Minimum $\overline{EL}$	5		80	40	ns	
pulse width; LOW	10	t_{WELL}	40	20	ns	
	15		35	17	ns	
Set-up time	5		50	25	ns	see also waveforms Fig.8
$D_n \rightarrow \overline{EL}$	10	t_{su}	25	12	ns	
	15		20	9	ns	
Hold-time	5		60	30	ns	
$D_n \rightarrow \overline{EL}$	10	t_{hold}	30	15	ns	
	15		25	12	ns	



Conditions:
D_D = LOW
$D_A = D_B = \overline{B_I} = \overline{LT}$ = HIGH

Fig.8 Waveforms showing minimum $\overline{EL}$ pulse width, set-up and hold time for DC to $\overline{EL}$.

APPLICATION INFORMATION

Some examples of applications for the HEF4511B are:

- Driving LED displays.
- Driving incandescent displays.
- Driving fluorescent displays.
- Driving LCD displays.
- Driving gas discharge displays.

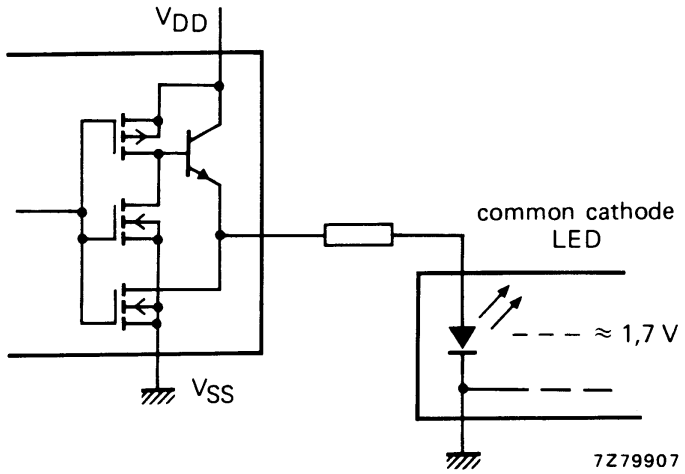


Fig.9 Connection to common cathode LED display readout.

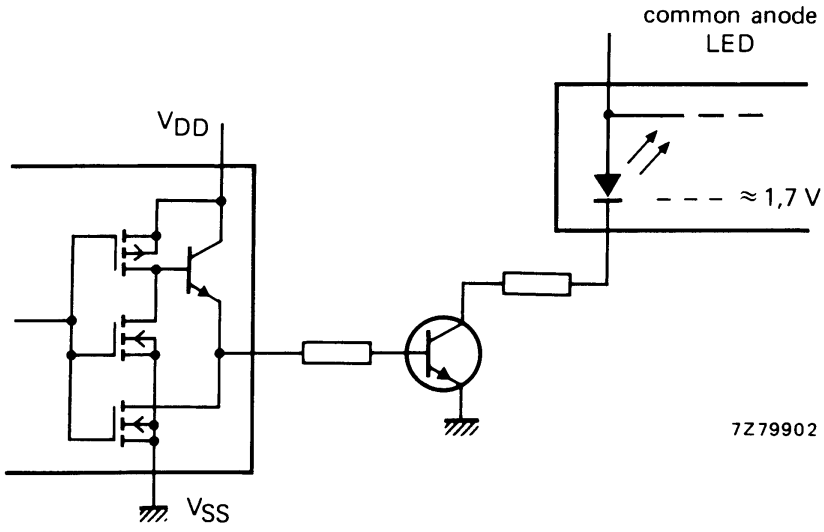
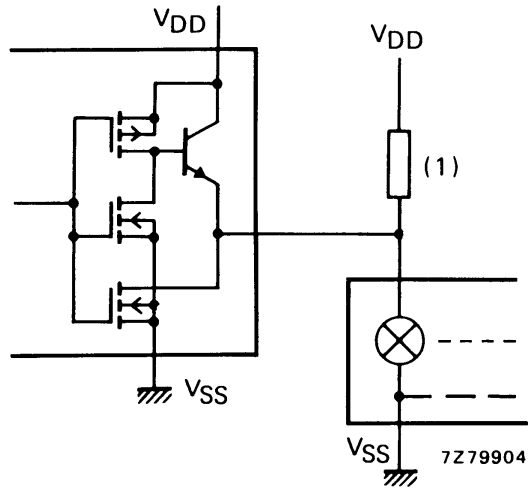


Fig.10 Connection to common anode LED display readout.



(1) A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Fig.11 Connection to incandescent display readout.

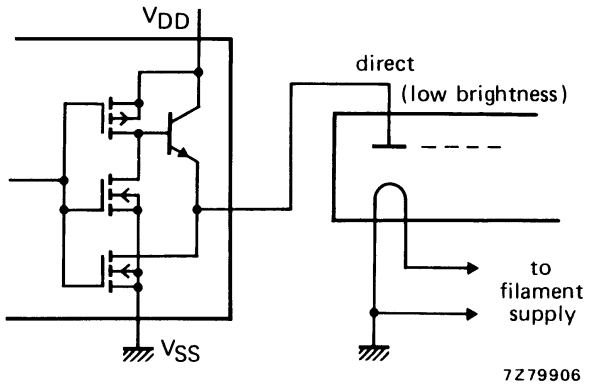


Fig.12 Connection to fluorescent display readout.

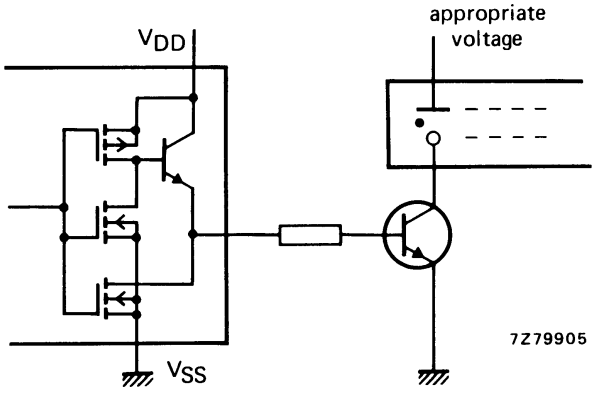


Fig.13 Connection to gas discharge display readout.

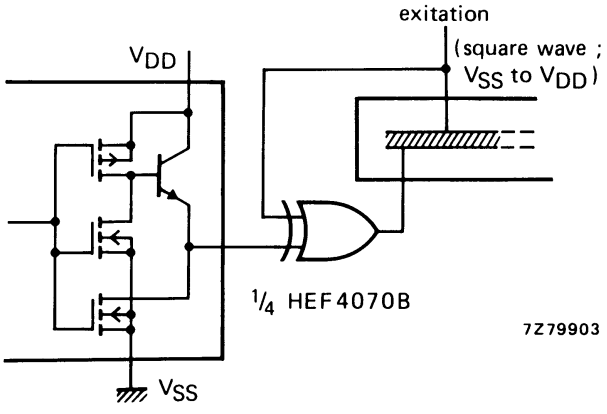


Fig.14 Connection to liquid crystal (LCD) display readout. Direct d.c. drive of LCDs not recommended for life of LCD readouts.