DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40193B MSI

4-bit up/down binary counter

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

4-bit up/down binary counter

HEF40193B
MSI

DESCRIPTION

The HEF40193B is a 4-bit synchronous up/down binary counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input ($\overline{PL}$), four parallel data inputs (P_0 to P_3), an asynchronous master reset input (MR), four counter outputs (O_0 to O_3), an active LOW terminal count-up (carry) output ($\overline{TC}_U$) and an active LOW terminal count-down (borrow) output ($\overline{TC}_D$).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. The outputs $\overline{TC}_U$ and $\overline{TC}_D$ are normally HIGH. When the circuit has reached the maximum count state of '15', the next HIGH to LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again. Likewise, output $\overline{TC}_D$ will go LOW when the circuit is in the zero state and CP_D goes LOW. When $\overline{PL}$ is LOW, the information on P_0 to P_3 is asynchronously loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions. The counter stages are of a static toggle type flip-flop.

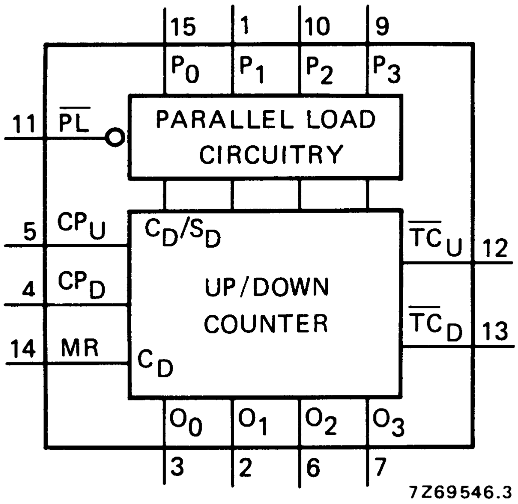

Fig.1 Functional diagram.

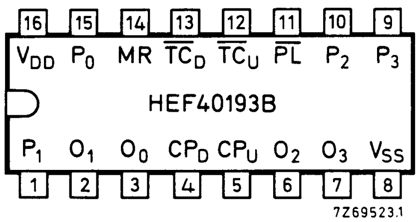

Fig.2 Pinning diagram.

HEF40193BP(N): 16-lead DIL; plastic (SOT38-1)

HEF40193BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)

HEF40193BT(D): 16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

PINNING

$\overline{PL}$	parallel load input (active LOW)
P_0 to P_3	parallel data inputs
CP_U	count-up clock pulse input (LOW to HIGH, edge-triggered)
CP_D	count-down clock pulse input (LOW to HIGH, edge-triggered)
MR	master reset input (asynchronous)
$\overline{TC}_U$	buffered terminal count-up (carry) output (active LOW)
$\overline{TC}_D$	buffered terminal count-down (borrow) output (active LOW)
O_0 to O_3	buffered counter outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specification

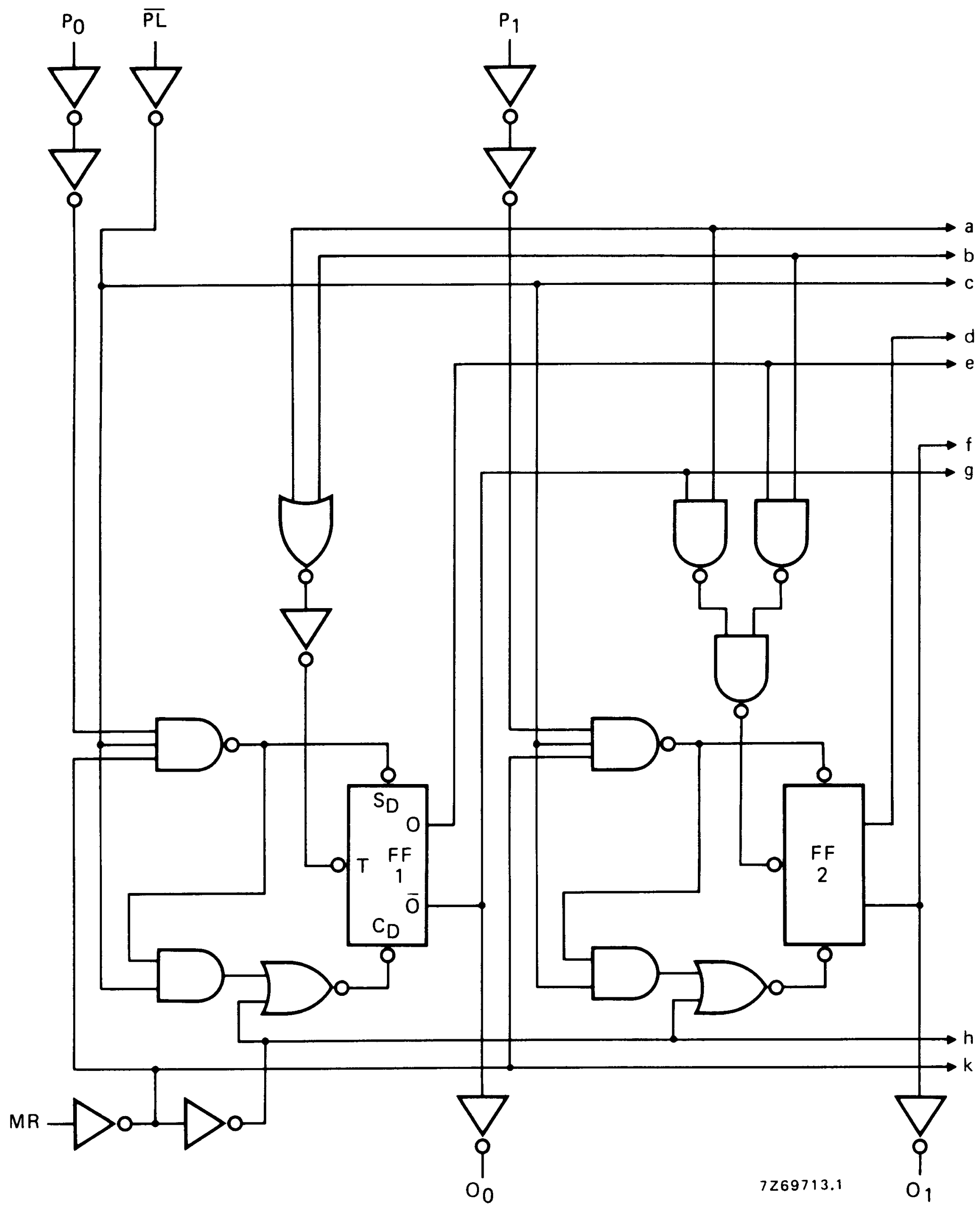

Fig.3 Logic diagram (continued on Fig.4).

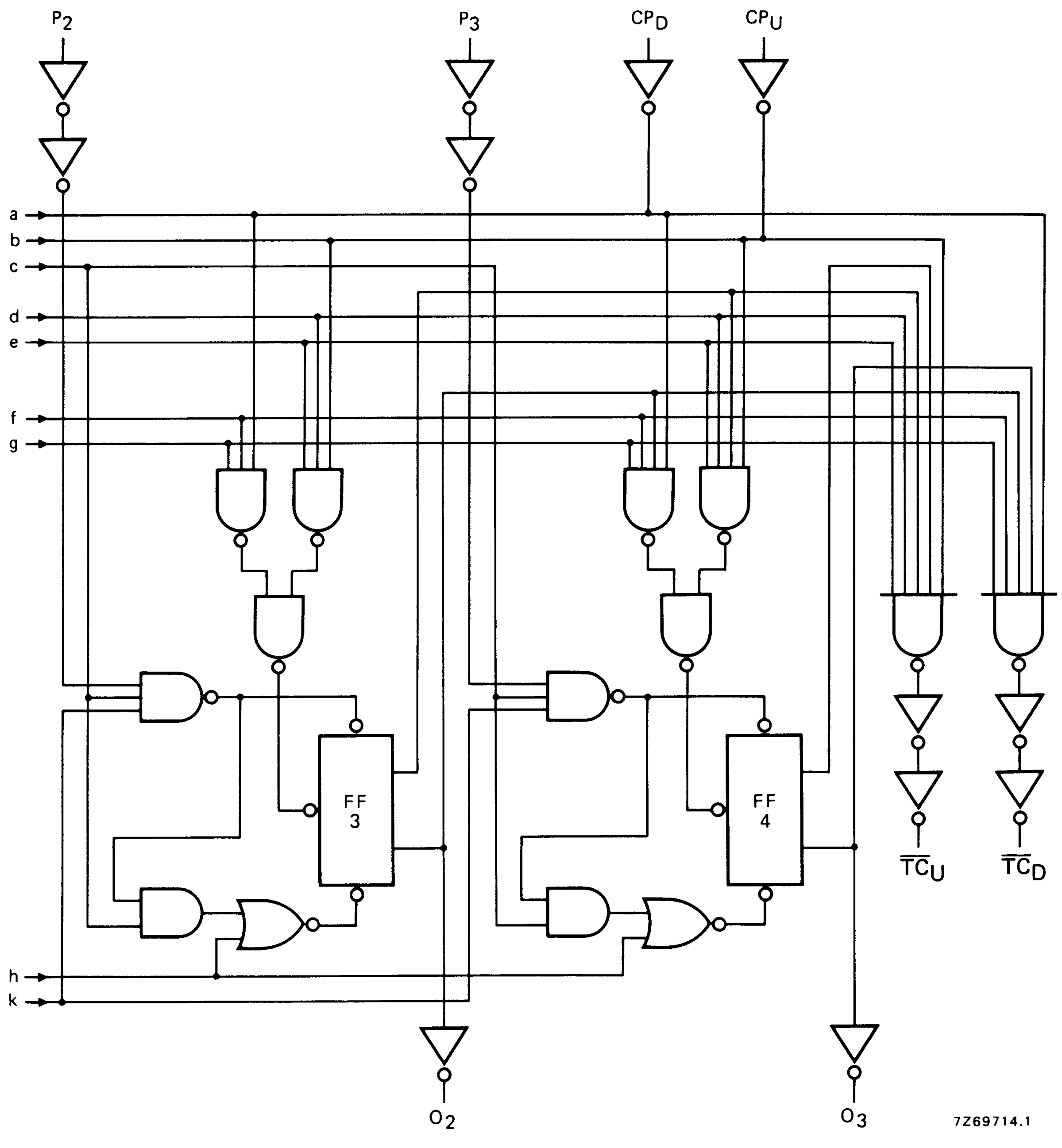

Fig.4 Logic diagram (continued from Fig.3).

4-bit up/down binary counter

HEF40193B
MSI

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H		H	count-up
L	H	H		count-down

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
    = positive-going transition

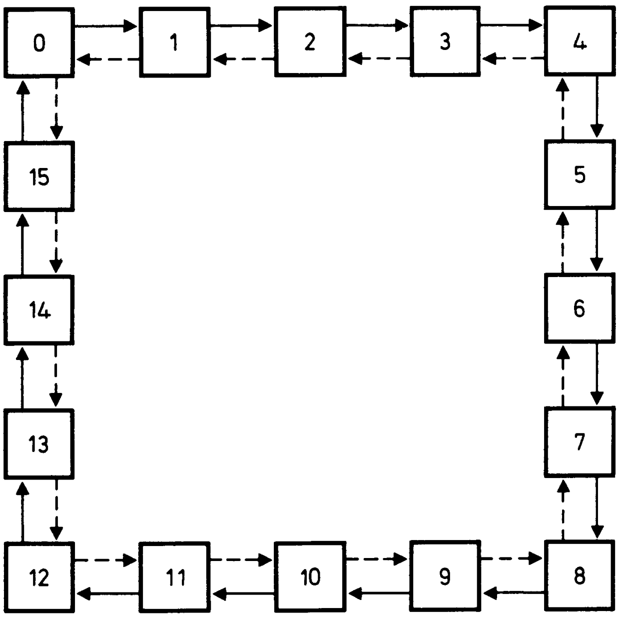

Fig.5 State diagram.

Logic equations for terminal count:

$$\overline{TC}_U = \overline{O_0 \cdot O_1 \cdot O_2 \cdot O_3 \cdot \overline{CP}_U}$$

$$\overline{TC}_D = \overline{\overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \cdot \overline{CP}_D}$$

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	$600\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	where
	10	$2700\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$7500\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\Sigma(f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$CP_U \rightarrow O_n$	5			210	415	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	165	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow O_n$	5			210	425	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			60	125	ns	57 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$CP_U \rightarrow \overline{TC}_U$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	185	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow \overline{TC}_D$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			100	195	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			195	390	ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$MR \rightarrow \overline{TC}_U$	5			145	285	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
$MR \rightarrow \overline{TC}_D$	5			365	730	ns	338 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		130	265	ns	119 ns + (0,23 ns/pF) C_L
	15			100	205	ns	92 ns + (0,16 ns/pF) C_L
$\overline{PL} \rightarrow O_n$	5			185	360	ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
LOW to HIGH	5	t_{PLH}		145	290	ns	118 ns + (0,55 ns/pF) C_L
	10			60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
Set-up time $P_n \rightarrow \overline{PL}$	5	t_{su}	160	80		ns	see also waveforms Fig.6
	10		60	30		ns	
	15		50	25		ns	
Hold time $P_n \rightarrow \overline{PL}$	5	t_{hold}	10	–70		ns	
	10		5	–25		ns	
	15		5	–20		ns	
Minimum CP_U or CP_D pulse width; LOW	5	t_{WCPL}	150	75		ns	
	10		50	25		ns	
	15		35	20		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	180	90		ns	
	10		70	35		ns	
	15		60	30		ns	
Minimum $\overline{PL}$ pulse width; LOW	5	t_{WPLL}	120	60		ns	
	10		45	20		ns	
	15		30	15		ns	
Recovery time for MR	5	t_{RMR}	125	65		ns	
	10		70	35		ns	
	15		50	25		ns	
Recovery time for $\overline{PL}$	5	t_{RPL}	90	45		ns	
	10		35	15		ns	
	15		25	10		ns	
Maximum clock pulse frequency	5	f_{max}	2,5	5		MHz	
	10		7	14		MHz	
	15		9	18		MHz	

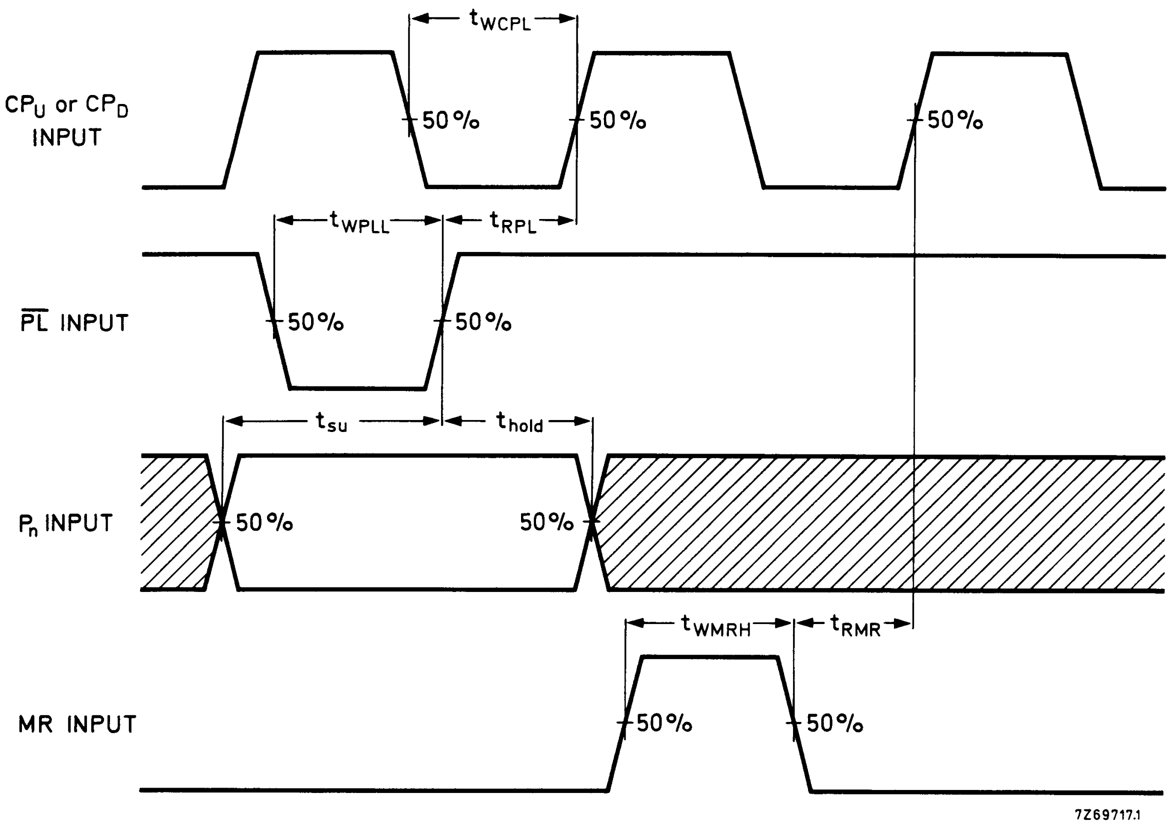

Fig.6 Waveforms showing recovery times for $\overline{PL}$ and MR, minimum pulse widths for CP_U, CP_D, $\overline{PL}$ and MR, and set-up and hold times for P to $\overline{PL}$. Set-up times and hold times are shown as positive values but may be specified as negative values.

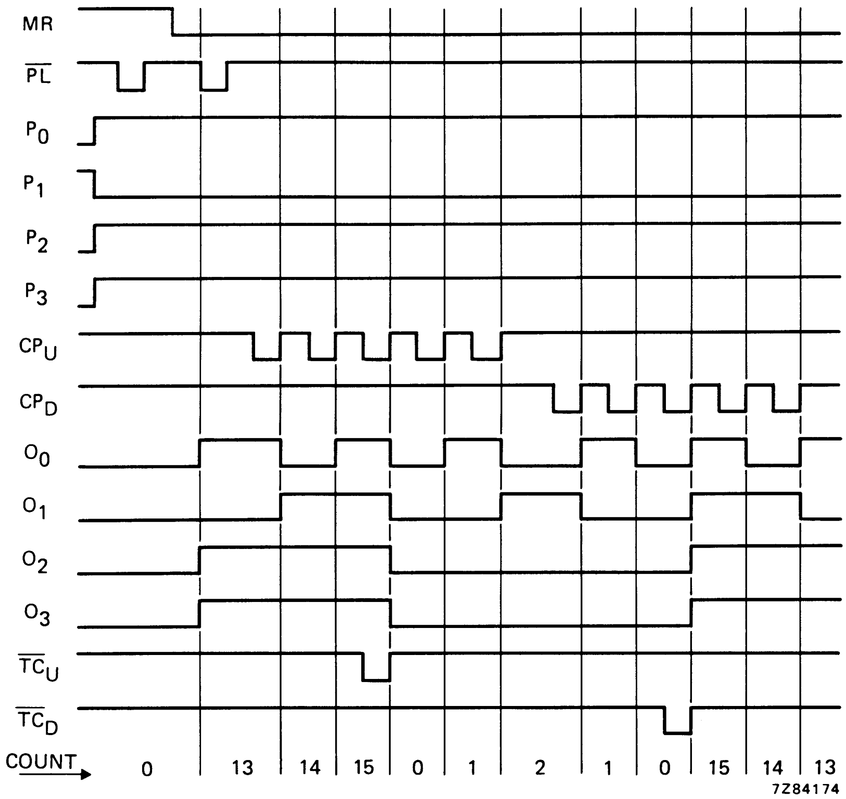

Fig.7 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF40193B are:

- Up/down difference counting
- Multistage ripple counting
- Multistage synchronous counting

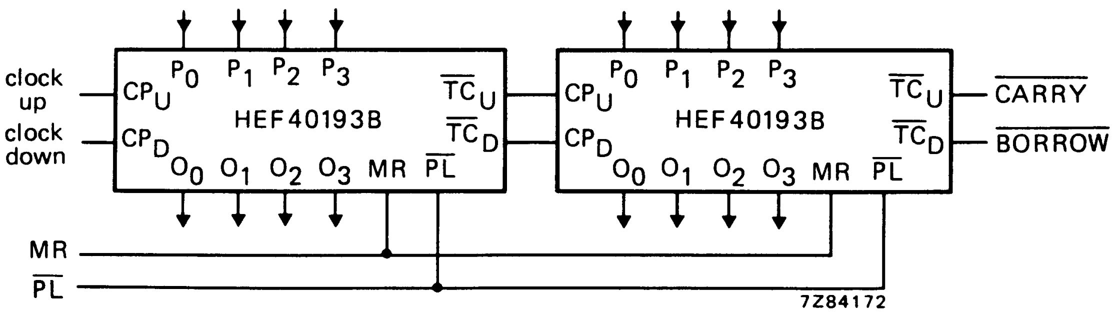

Fig.8 Example of cascaded HEF40193B ICs.