

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOC莫斯 HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOC莫斯 HE4000B Logic Package Outlines/Information HEF, HEC

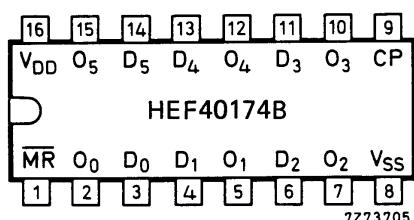
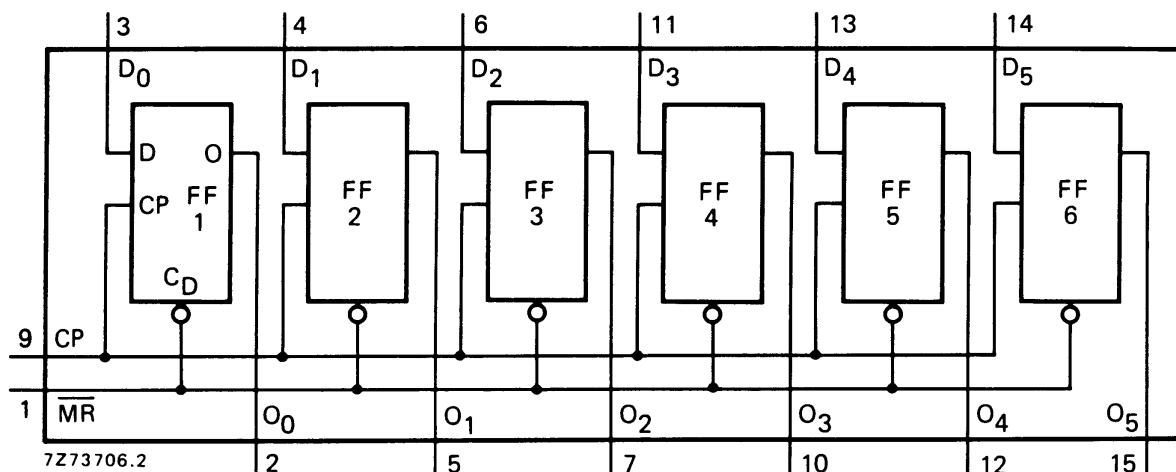
HEF40174B **MSI** **Hex D-type flip-flop**

Product specification
File under Integrated Circuits, IC04

January 1995

Hex D-type flip-flop**HEF40174B
MSI****DESCRIPTION**

The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D_0 to D_5), a clock input (CP), an overriding asynchronous master reset input (MR), and six buffered outputs (O_0 to O_5). Information on D_0 to D_5 is transferred to O_0 to O_5 on the LOW to HIGH transition of CP if \overline{MR} is HIGH. When LOW, \overline{MR} resets all flip-flops (O_0 to O_5 = LOW) independent of CP and D_0 to D_5 .

**PINNING**

D_0 to D_5	data inputs
CP	clock input (LOW to HIGH; edge-triggered)
MR	master reset input (active LOW)
O_0 to O_5	buffered outputs

FUNCTION TABLE

INPUTS			OUTPUT
CP	D	\overline{MR}	O
/	H	H	H
/	L	H	L
\	X	H	no change
X	X	L	L

Notes

1. H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

/ = positive-going transition

\ = negative-going transition

HEF40174BP(N): 16-lead DIL; plastic
(SOT38-1)

HEF40174BD(F): 16-lead DIL; ceramic (cerdip)
(SOT74)

HEF40174BT(D): 16-lead SO; plastic
(SOT109-1)

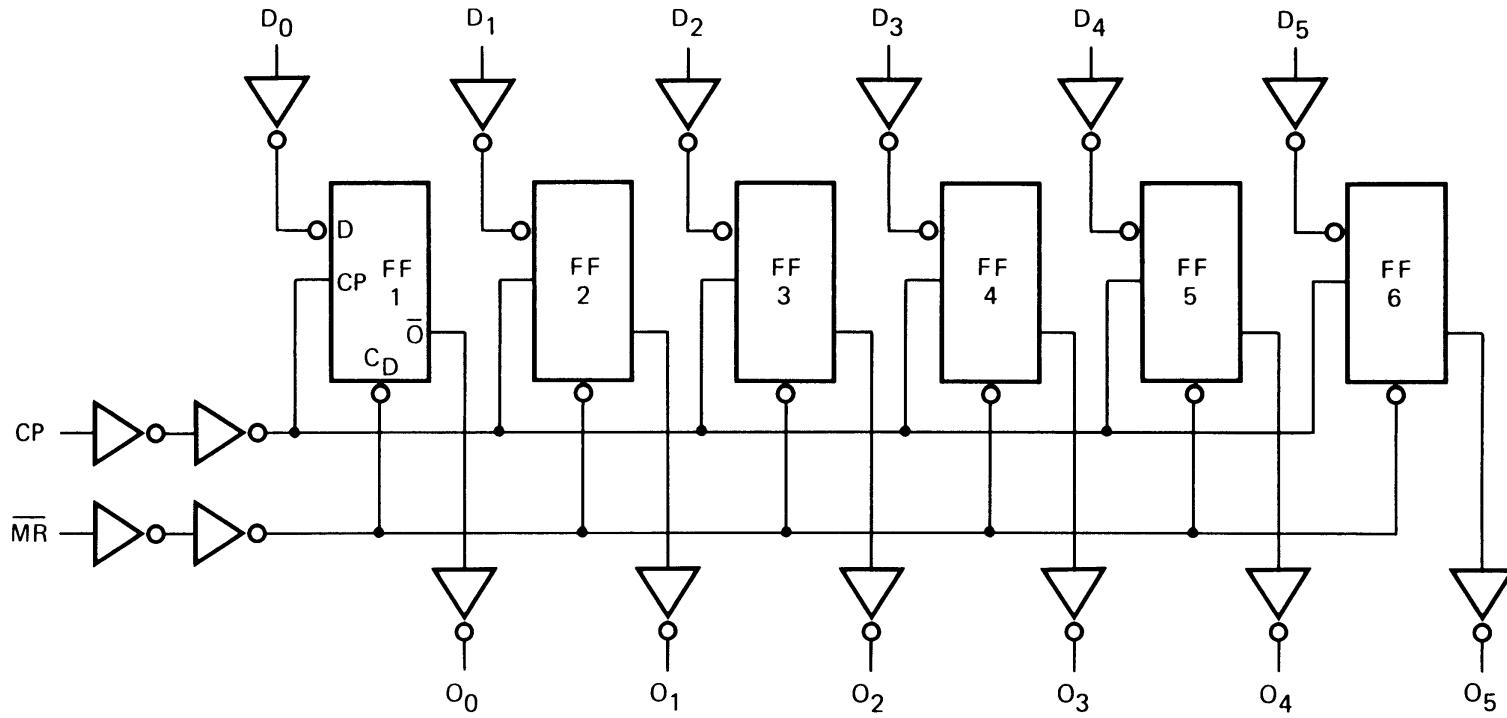
(): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

Hex D-type flip-flop

**HEF40174B
MSI**



7Z73794.1

Fig.3 Logic diagram.

Hex D-type flip-flop

HEF40174B
MSI

AC CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

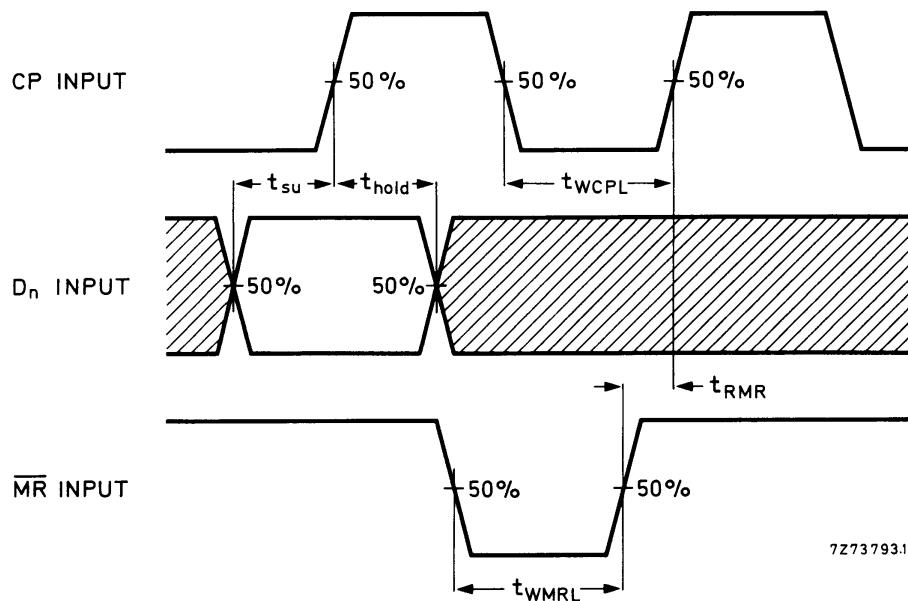
	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $CP \rightarrow O_n$ HIGH to LOW	5 10 15	t_{PHL}	75 30 20	155 65 45	ns	$48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ $19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ $12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{PLH}	75 30 20	155 65 45	ns	$48 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ $19 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ $12 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
$\overline{MR} \rightarrow O_n$ HIGH to LOW	5 10 15	t_{PHL}	85 35 25	175 70 50	ns	$58 \text{ ns} + (0,55 \text{ ns/pF}) C_L$ $24 \text{ ns} + (0,23 \text{ ns/pF}) C_L$ $17 \text{ ns} + (0,16 \text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5 10 15	t_{THL}	60 30 20	120 60 40	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
LOW to HIGH	5 10 15	t_{TLH}	60 30 20	120 60 40	ns	$10 \text{ ns} + (1,0 \text{ ns/pF}) C_L$ $9 \text{ ns} + (0,42 \text{ ns/pF}) C_L$ $6 \text{ ns} + (0,28 \text{ ns/pF}) C_L$
Set-up time $D_n \rightarrow CP$	5 10 15	t_{su}	20 10 10	10 5 5	ns	see also waveforms Fig.4
Hold time $D_n \rightarrow CP$	5 10 15	t_{hold}	10 5 5	0 0 0	ns	
Minimum clock pulse width; LOW	5 10 15	t_{WCPL}	70 30 20	35 15 10	ns	
Minimum \overline{MR} pulse width; LOW	5 10 15	t_{WMRL}	70 35 25	35 15 10	ns	
Recovery time for \overline{MR}	5 10 15	t_{RMR}	45 20 15	25 10 5	ns	
Maximum clock pulse frequency	5 10 15	f_{max}	5 15 20	11 30 45	MHz	

Hex D-type flip-flop

HEF40174B
MSI

	V_{DD} V	TYPICAL FORMULA FOR $P(\mu W)$	
Dynamic power dissipation per package (P)	5	$3500 f_i + \sum (f_o C_L) \times V_{DD}^2$	where
	10	$16\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	15	$42\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)

C_L = load capacitance (pF)
 $\sum (f_o C_L)$ = sum of outputs
 V_{DD} = supply voltage (V)



7273793.1

Fig.4 Waveforms showing minimum pulse widths for CP and \overline{MR} , \overline{MR} to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40174B are:

- Shift registers
- Buffer/storage register
- Pattern generator