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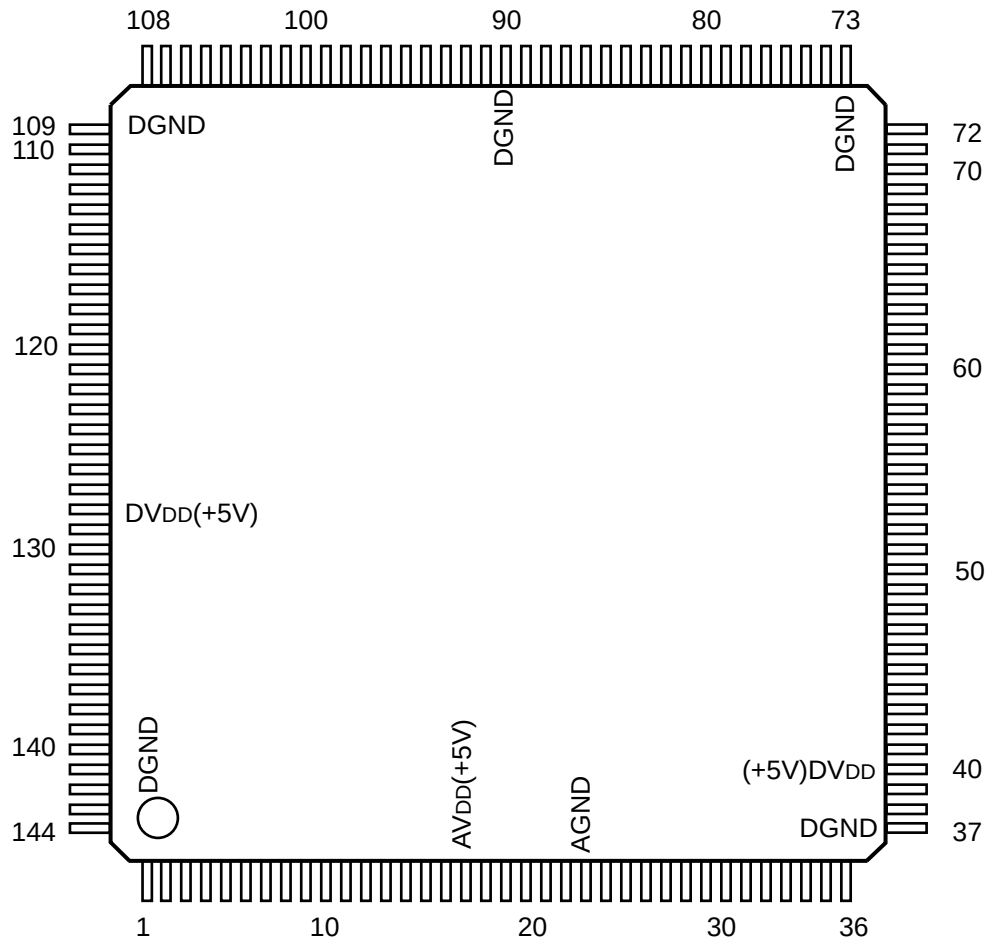
C-MOS ISDNI INTERFACE

-TOP VIEW-



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	-	DGND	37	-	DGND	73	-	DGND	109	-	DGND
2	O	EXHLTA/CDETP	38	O	XTAL	74	I/O	A18	110	I/O	OAD2
3		EXHOLT	39	I	EXTAL	75	I/O	A19	111	O	OAD3
4	I	L3CLK	40	-	DV_{DD}	76	I/O	D7/TQ4	112	O	OAD4
5	I/O	LSW	41	O	CK12M/24M	77	I/O	D6/TQ3	113	O	OAD5
6	O	RBA	42	I	OSCSEL	78	I/O	D5/TQ2	114	O	OAD6
7	O	RBB	43	I	PD	79	I/O	D4/TQ1	115	O	OAD7
8	I	TBA	44	O	CPUCLK	80	I/O	D3/RQ4	116	O	OAD8
9	I	TBB	45	I/O	$\overline{HALT}$	81	I/O	D2/RQ3	117	O	OAD9
10	I/O	CK1536	46	O	ST	82	I/O	D1/RQ2	118	O	OAD10
11	I/O	CK8L	47	I	$\overline{NMI}$	83	I/O	D0/RQ1	119	O	OAD11
12	I/O	CK64K128K	48	I/O	$\overline{INT0}$	84	I	TEST0	120	O	OAD12
13	I	BCH CLK SEL	49	I	$\overline{RESET}$	85	I	TEST1	121	O	OAD13
14	I/O	RTIO	50	I/O	$\overline{LIR}$	86	I	TEST2	122	O	OAD14
15	I/O	RDIO	51	I/O	$\overline{RD}$	87	I	TEST3	123	O	OAD15
16	I/O	TDIO	52	I/O	$\overline{WR}$	88	O	$\overline{RAMCS}$	124	O	OAD16
17	O	RE	53	I/O	$\overline{ME}$	89	O	$\overline{ROMCS}$	125	O	OAD17
18	-	AV_{DD}	54	I/O	$\overline{IOE}$	90	-	DGND	126	O	OAD18
19	I	LRA	55	I/O	A0	91	I/O	OD0	127	I/O	OAD19
20	I	LRB	56	I/O	A1	92	I/O	OD1	128	-	DV_{DD}
21	O	LTA	57	I/O	A2	93	I/O	OD2	129	I	DMA/IO
22	O	LTB	58	I/O	A3	94	I/O	OD3	130	I	B/W
23	-	AGND	59	I/O	A4	95	I/O	OD4	131	I	CPU1
24	I	MODE M/S	60	I/O	A5	96	I/O	OD5	132	I	CPU2
25	I	RCVSEL	61	I/O	A6	97	I/O	OD6	133	O	$\overline{INTR}$
26	I	TXSEL	62	I/O	A7	98	I/O	OD7	134	I	$\overline{CS}$
27	O	CK4K	63	I/O	A8	99	I/O	OD8	135	O	$\overline{UDS}$
28	O	CK200	64	I/O	A9	100	I/O	OD9	136	I/O	$\overline{DTA}$
29	O	SYNC	65	I/O	A10	101	I/O	OD10	137	I/O	$\overline{LDS}$
30	I	ABIT/VDET	66	I/O	A11	102	I/O	OD11	138	I/O	$\overline{AS}$
31	I	L1ACT	67	I/O	A12	103	I/O	OD12	139	I/O	$\overline{OWR}$
32	I	L2ACT	68	I/O	A13	104	I/O	OD13	140	I/O	$\overline{ORD}$
33	O	$\overline{SDO}$	69	I/O	A14	105	I/O	OD14	141	O	$\overline{M}$/IO
34	O	$\overline{WDT}$	70	I/O	A15	106	I/O	OD15	142		BGA
35	I	CLKINH	71	I/O	A16	107	I/O	OAD0	143	I	HLTA/$\overline{DREQ}$
36	O	CLKSTP	72	I/O	A17	108	I/O	OAD1	144	O	HOLT/$\overline{DRDY}$

INPUT

ABIT/VDET	; ABITSET/ VDET
BCH CLK SEL	; B-CHANNEL CLOCK SELECT
B/W	; BYTE/ WORD SELECT
CLKINH	; CLOCK INHIBIT
CPU1,CPU2	; CPU TYPE SELECT
$\overline{CS}$	; CHIP SELECT
DMA/IO	; DMA/ IO MODE SELECT
$\overline{DREQ}$	; REQUEST FOR TRANSMIT D-CHANNEL
EXTAL	; OSCILLATOR (12.288MHz OR 24.576MHz)
HLTA	; HOLD ACKNOWLEDGEMENT FROM UPPER CPU
L1ACT,L2ACT	; LAYER1,2 ACTIVE
L3CLK	; UPPER CPU SYSTEM CLOCK
LRA,LRB	; LINE RECEIVE A,B
MODE M/S	; MASTER/ SLAVE MODE SELECT
$\overline{NMI}$	; NON MASKABLE INTERRUPT
OSCSEL	; SYSTEM CLOCK SELECT (L: 12.288MHz/ H: 24.576MHz)
PD	; POWER DOWN SET
RCVSEL	; RECEIVE TIMING SELECT
$\overline{RESET}$	; RESET
TBA,TBB	; TRANSMIT B-CHANNEL DATA A,B
TEST0-TEST3	; MODE SET
TQ1-TQ4	; TRANSMIT Q-BIT
TXSEL	; TEST MODE

OUTPUT

CDETP	; COLLISION DETECT
CK12M/24M	; 12MHz CLOCK
CK200	; 200Hz CLOCK
CK4K	; 4kHz CLOCK
CLKSTP	; CLOCK STOP
CPUCLK	; SYSTEM CLOCK
$\overline{\text{DRDY}}$	; READY FOR TRANSMIT D-CHANNEL
HOLT	; HOLD REQUEST TO UPPER CPU
$\overline{\text{INTR}}$	; INTERRUPT REQUEST TO UPPER CPU
LTA,LTB	; LINE TRANSMIT A,B
$\overline{\text{M}}$/IO	; MEMORY REQUEST TO 8086 BUS
OAD3-OAD18	; ADDRESS BUS FOR UPPER CPU
$\overline{\text{RAMCS}}$	; RAM CHIP SELECT
RBA,RBB	; RECEIVE B-CHANNEL DATA A,B
RE	; ECHO BIT RECEIVE
$\overline{\text{ROMCS}}$	; ROM CHIP SELECT
RQ1-RQ4	; RECEIVE Q-BIT
$\overline{\text{SDO}}$	; SIGNAL DETECT
ST	; STATUS
SYNC	; SYNCHRONIZATION
$\overline{\text{UDS}}$	; UPPER DATA STROBE
$\overline{\text{WDT}}$	; WATCH DOG TIMER
XTAL	; OSCILLATOR (12.288MHz OR 24.576MHz)

INPUT/OUTPUT

A0-A19	; ADDRESS BUS
$\overline{AS}$	; ADDRESS STROBE
CK1536	; 1.536MHz CLOCK
CK64K/128K	; B-CHANNEL BIT TIMING
CK8K	; B-CHANNEL FRAME TIMING
D0-D7	; DATA BUS
$\overline{DTA}$	; DATA TRANSFER ACKNOWLEDGE
$\overline{HALT}$	; HALT
$\overline{INT0}$	; INTERRUPT 0
$\overline{IOE}$	; I/O ENABLE
$\overline{LDS}$	; LOWER DATA STROBE
$\overline{LIR}$	; LOAD INSTRUCTION REGISTER
LSW	; LAYER1 ACTIVATION SWITCH
$\overline{ME}$	; MEMORY ENABLE
OAD0-OAD2,OAD19	; ADDRESS BUS FOR UPPER CPU
OD0-OD15	; DATA BUS FOR UPPER CPU
$\overline{ORD}$	; READ FOR UPPER CPU
$\overline{OWR}$	; WRITE FOR UPPER CPU
$\overline{RD}$	; READ
RDIO	; RECEIVE D-CHANNEL DATA
RTIO	; D-CHANNEL DATA RECEIVE/ TRANSMIT TIMING CLOCK
TDIO	; TRANSMIT D-CHANNEL DATA
$\overline{WR}$	; WRITE