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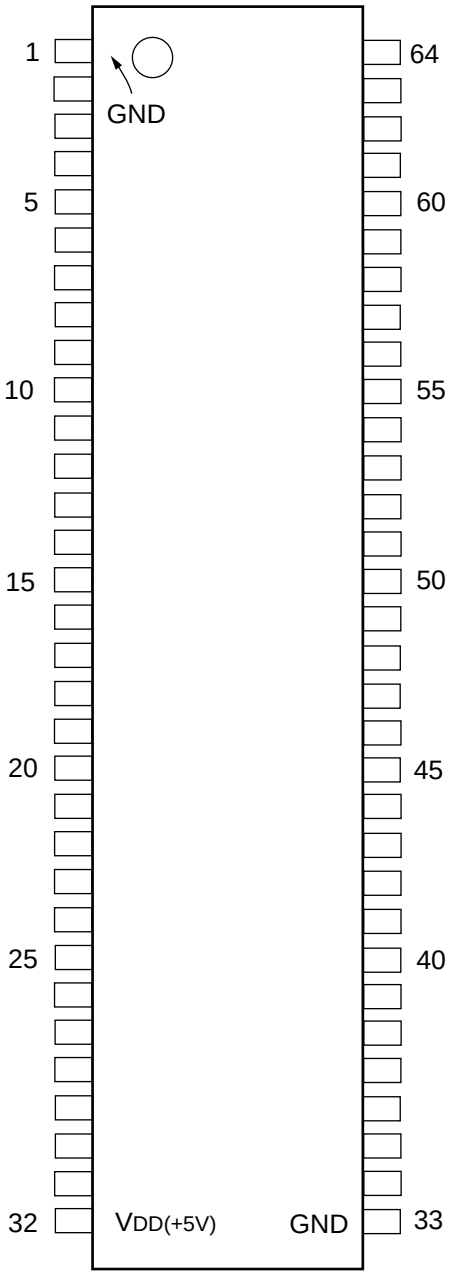
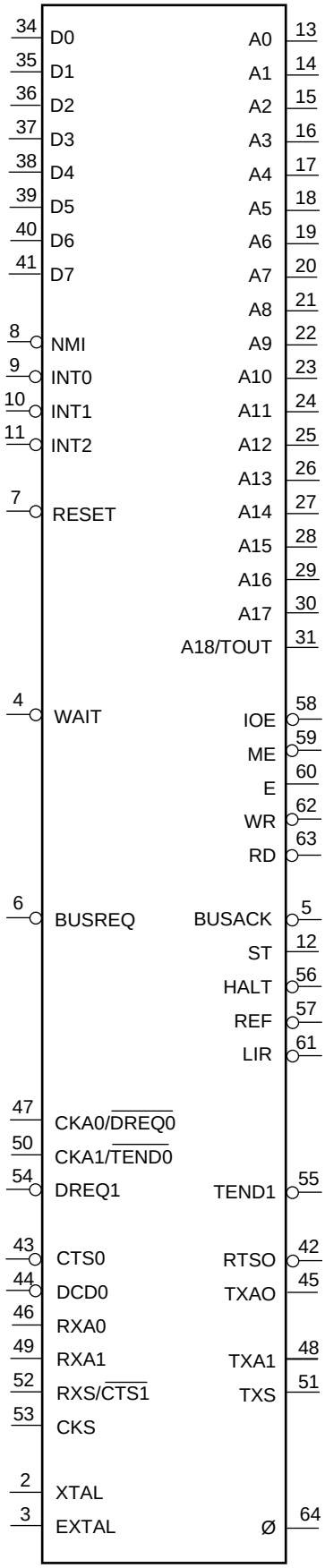
C-MOS 8-BIT MICROPROCESSOR

-TOP VIEW-



(V_{DD} = +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	33	—	GND
2	I	XTAL	34	I/O	D_0
3	I	EXTAL	35	I/O	D_1
4	I	$\overline{WAIT}$	36	I/O	D_2
5	O	$\overline{BUSACK}$	37	I/O	D_3
6	I	$\overline{BUSREQ}$	38	I/O	D_4
7	I	$\overline{RESET}$	39	I/O	D_5
8	I	$\overline{NMI}$	40	I/O	D_6
9	I	$\overline{INT_0}$	41	I/O	D_7
10	I	$\overline{INT_1}$	42	O	$\overline{RTS_0}$
11	I	$\overline{INT_2}$	43	I	$\overline{CTS_0}$
12	O	ST	44	I	$\overline{DCD_0}$
13	O	A_0	45	O	TXA_0
14	O	A_1	46	I	RXA_0
15	O	A_2	47	I/O	$CKA_0/\overline{DREQ_0}$
16	O	A_3	48	O	TXA_1
17	O	A_4	49	I	RXA_1
18	O	A_5	50	I/O	$CKA_1/\overline{TEND_0}$
19	O	A_6	51	O	TXS
20	O	A_7	52	I	$RXS/\overline{CTS_1}$
21	O	A_8	53	I/O	CKS
22	O	A_9	54	I	$\overline{DREQ_1}$
23	O	A_{10}	55	O	$\overline{TEND_1}$
24	O	A_{11}	56	O	$\overline{HALT}$
25	O	A_{12}	57	O	$\overline{REF}$
26	O	A_{13}	58	O	$\overline{IOE}$
27	O	A_{14}	59	O	$\overline{ME}$
28	O	A_{15}	60	O	E
29	O	A_{16}	61	O	$\overline{LIR}$
30	O	A_{17}	62	O	$\overline{WR}$
31	O	A_{18}/T OUT	63	O	$\overline{RD}$
32	—	V_{DD} (+5V)	64	O	Ø



INPUT

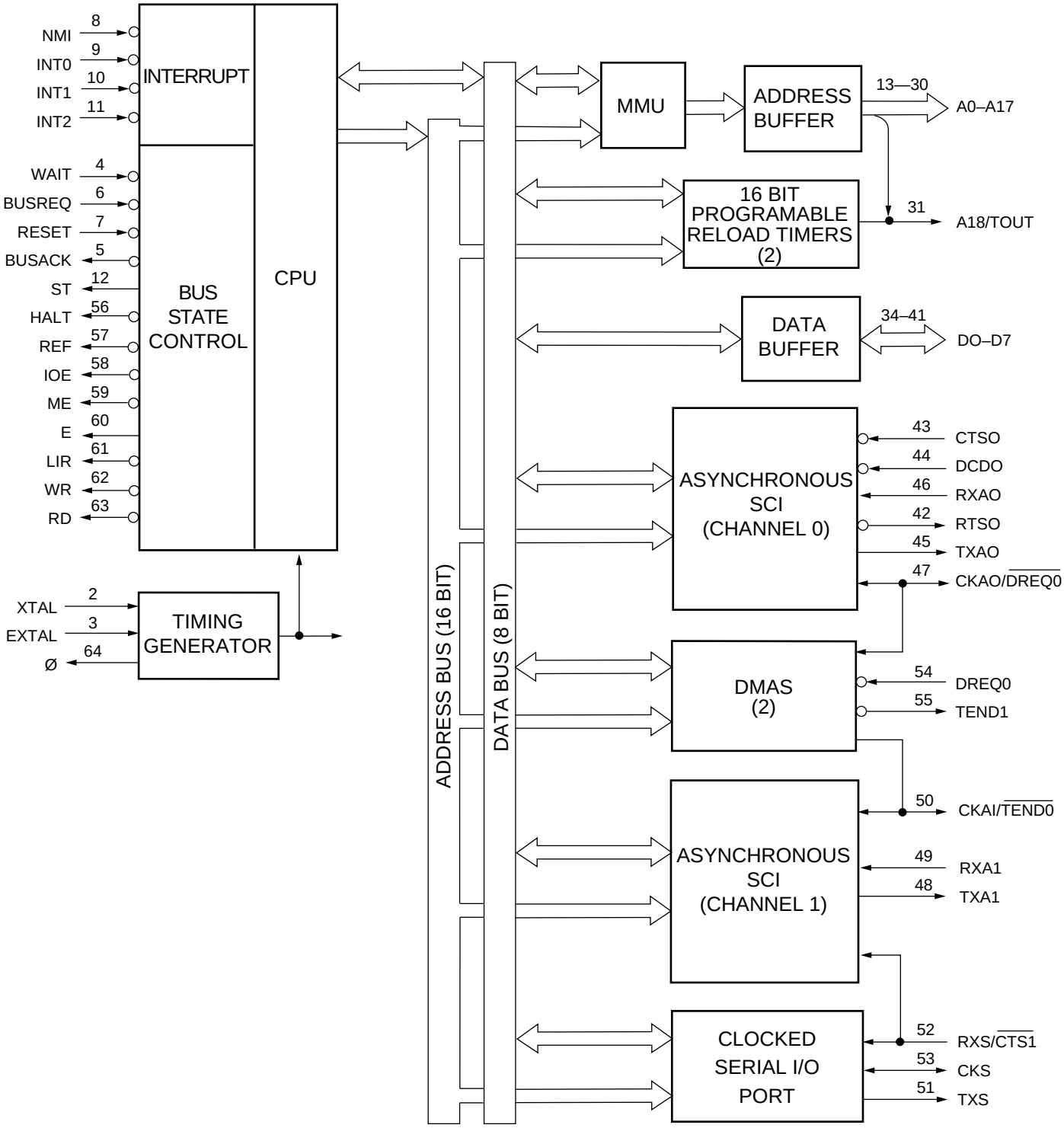
BUSREQ	; BUS REQUEST
CTS0, 1	; CLEAR TO SEND FOR ASYNCHRONOUS SCI CHANNEL 0, 1
DCD0	; DATA CARRIER DETECT FOR ASYNCHRONOUS SCI CHANNEL 0, 1
DREQ0, 1	; DMA REQUEST FOR CHANNEL 0, 1
EXTAL	; EXTERNAL CLOCK
INT0–2	; INTERRUPT
NMI	; NON–MASKABLE INTERRUPT
RXA0, 1	; RECEIVE DATA FOR ASYNCHRONOUS SCI CHANNEL 0, 1
RXS	; RECEIVE DATA FOR SERIAL I/O PORT
XTAL	; CLOCK

OUTPUT

AO–A18	; ADDRESS BUS
BUSACK	; BUS ACKNOWLEDGE
E	; ENABLE
IOE	; I/O ENABLE
LIR	; LOAD INSTRUCTION REGISTER
ME	; MEMORY ENABLE
RD	; READ
REF	; REFRESH
RTS0	; REQUEST TO SEND FOR ASYNCHRONOUS SCI CHANNEL 0, 1
ST	; STATUS
TEND0, 1	; TRANSFER END FOR CHANNEL 0, 1
TXA0, 1	; TRANSFER DATA FOR ASYNCHRONOUS SCI CHANNEL 0, 1
TXS	; TRANSFER DATA FOR SERIAL I/O PORT
WR	; WRITE
Ø	; SYSTEM CLOCK

INPUT/OUTPUT

CKA0, 1	; CLOCK FOR ASYNCHRONOUS SCI CHANNEL 0,1
CKS	; CLOCK FOR SERIAL I/O PORT


NMI
INT0
INT1
INT2
8
9
10
11
INTERRUPT
WAIT
BUSREQ
RESET
BUSACK
ST
HALT
REF
IOE
ME
E
LIR
WR
RD
4
6
7
5
12
56
57
58
59
60
61
62
63
BUS STATE CONTROL
CPU
XTAL
EXTAL
Ø
2
3
64
TIMING GENERATOR
ADDRESS BUS (16 BIT)
DATA BUS (8 BIT)
MMU
ADDRESS BUFFER
13—30
A0–A17
16 BIT PROGRAMABLE RELOAD TIMERS (2)
31
A18/TOUT
DATA BUFFER
34–41
DO–D7
ASYNCHRONOUS SCI (CHANNEL 0)
43
CTSO
44
DCDO
46
RXAO
42
RTSO
45
TXAO
47
CKAO/DREQ0
DMAS (2)
54
DREQ0
55
TEND1
50
CKAI/TEND0
ASYNCHRONOUS SCI (CHANNEL 1)
49
RXA1
48
TXA1
CLOCKED SERIAL I/O PORT
52
RXS/CTS1
53
CKS
51
TXS