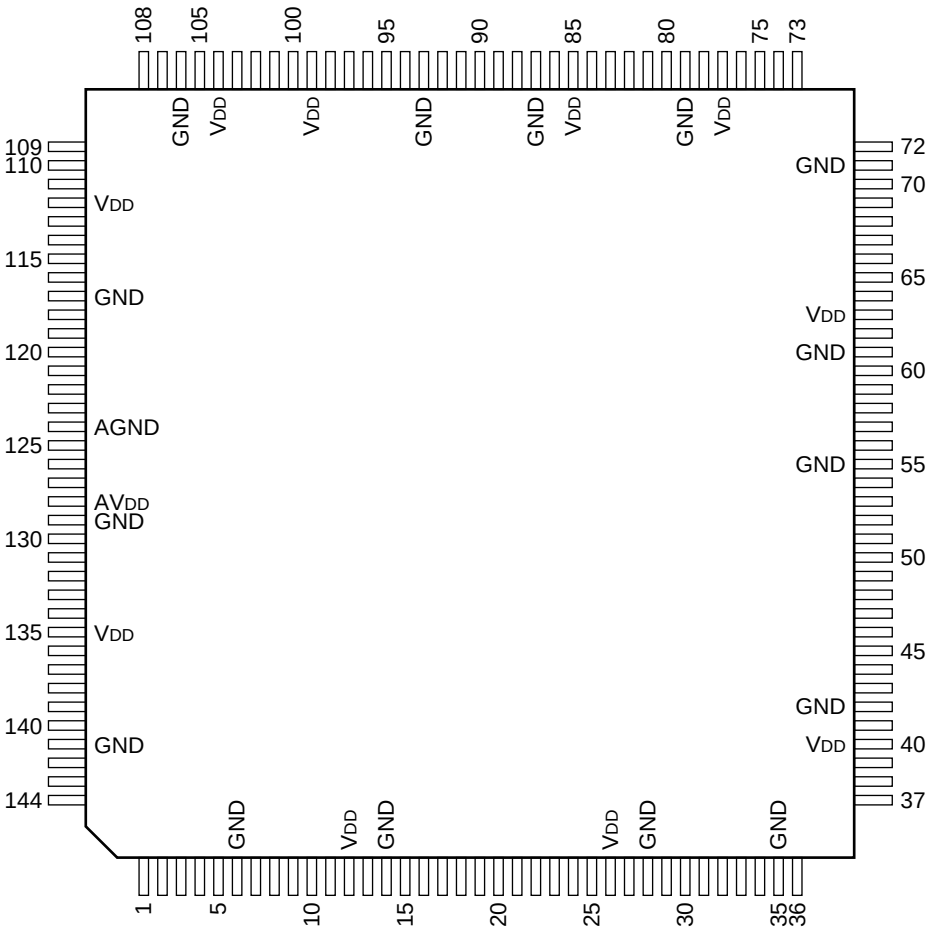
C-MOS SINGLE CHIP MICROCOMPUTER

—TOP VIEW—



FUNCTION OVER VIEWS

- CASH MEMORY (1K BYTE)
- COMPARE MATCH TIMER (2 CHANNEL)
- WATCH DOG TIMER
- SERIAL COMMUNICATION I/F (2 CHANNEL)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I/O	PA23/$\overline{\text{WRHH}}$	37	I/O	PB6/$\overline{\text{IRQ4}}$/A18/$\overline{\text{BACK}}$	73	I/O	PD15/D15	109	I/O	PE0/TIOC0A/$\overline{\text{DREQ0}}$
2	I/O	PE14/TIOC4C/DACK0/$\overline{\text{AH}}$	38	I/O	PB7/$\overline{\text{IRQ5}}$/A19/$\overline{\text{BREQ}}$	74	I/O	PD14/D14	110	I/O	PE1/TIOC0B/DRAK0
3	I/O	PA22/$\overline{\text{WRHL}}$	39	I/O	PB8/$\overline{\text{IRQ6}}$/A20/$\overline{\text{WAIT}}$	75	I/O	PD13/D13	111	I/O	PE2/TIOC0C/$\overline{\text{DREQ1}}$
4	I/O	PA21/$\overline{\text{CASHH}}$	40	—	V_{DD}	76	I/O	PD12/D12	112	—	V_{DD}
5	I/O	PE15/TIOC4D/DACK1/$\overline{\text{IRQOUT}}$	41	I/O	PB9/$\overline{\text{IRQ7}}$/A21/$\overline{\text{ADTRG}}$	77	—	V_{DD}	113	I/O	PE3/TIOC0D/DRAK1
6	—	GND	42	—	GND	78	I/O	PD11/D11	114	I/O	PE4/TIOC1A
7	I/O	PC0/A0	43	I/O	PA14/$\overline{\text{RD}}$	79	—	GND	115	I/O	PE5/TIOC1B
8	I/O	PC1/A1	44	O	$\overline{\text{WDTOVF}}$	80	I/O	PD10/D10	116	I/O	PE6/TIOC2A
9	I/O	PC2/A2	45	I/O	PD31/D31/$\overline{\text{ADTRG}}$	81	I/O	PD9/D9	117	—	GND
10	I/O	PC3/A3	46	I/O	PD30/D30/$\overline{\text{IRQOUT}}$	82	I/O	PD8/D8	118	I	PF0/AN0
11	I/O	PC4/A4	47	I/O	PA13/$\overline{\text{WRH}}$	83	I/O	PD7/D7	119	I	PF1/AN1
12	—	V_{DD}	48	I/O	PA12/$\overline{\text{WRL}}$	84	I/O	PD6/D6	120	I	PF2/AN2
13	I/O	PC5/A5	49	I/O	PA11/$\overline{\text{CS1}}$	85	—	V_{DD}	121	I	PF3/AN3
14	—	GND	50	I/O	PA10/$\overline{\text{CS0}}$	86	I/O	PD5/D5	122	I	PF4/AN4
15	I/O	PC6/A6	51	I/O	PA9/TCLKD/$\overline{\text{IRQ3}}$	87	—	GND	123	I	PF5/AN5
16	I/O	PC7/A7	52	I/O	PA8/TCLKC/$\overline{\text{IRQ2}}$	88	I/O	PD4/D4	124	—	AGND
17	I/O	PC8/A8	53	I/O	PA7/TCLKB/$\overline{\text{CS3}}$	89	I/O	PD3/D3	125	I	PF6/AN6
18	I/O	PC9/A9	54	I/O	PA6/TCLKA/$\overline{\text{CS2}}$	90	I/O	PD2/D2	126	I	PF7/AN7
19	I/O	PC10/A10	55	—	GND	91	I/O	PD1/D1	127	—	AV_{REF}
20	I/O	PC11/A11	56	I/O	PD29/D29/$\overline{\text{CS3}}$	92	I/O	PD0/D0	128	—	AV_{DD}
21	I/O	PC12/A12	57	I/O	PD28/D28/$\overline{\text{CS2}}$	93	—	GND	129	—	GND
22	I/O	PC13/A13	58	I/O	PD27/D27/DACK1	94	I	XTAL	130	I/O	PA0/RXD0
23	I/O	PC14/A14	59	I/O	PD26/D26/DACK0	95	I	MD3	131	I/O	PA1/TXD0
24	I/O	PC15/A15	60	I/O	PD25/D25/$\overline{\text{DREQ1}}$	96	I	EXTAL	132	I/O	PA2/SCK0/$\overline{\text{DREQ0}}$/$\overline{\text{IRQ0}}$
25	I/O	PB0/A16	61	—	GND	97	I	MD2	133	I/O	PA3/RXD1
26	—	V_{DD}	62	I/O	PD24/D24/$\overline{\text{DREQ0}}$	98	I	NMI	134	I/O	PA4/TXD1
27	I/O	PB1/A17	63	—	V_{DD}	99	—	V_{DD}	135	—	V_{DD}
28	—	GND	64	I/O	PD23/D23/$\overline{\text{IRQ7}}$	100	I/O	PA16/$\overline{\text{AH}}$	136	I/O	PA5/SCK1/$\overline{\text{DREQ1}}$/$\overline{\text{IRQ1}}$
29	I/O	PA20/$\overline{\text{CASHL}}$	65	I/O	PD22/D22/$\overline{\text{IRQ6}}$	101	I/O	PA17/$\overline{\text{WAIT}}$	137	I/O	PE7/TIOC2B
30	I/O	PA19/$\overline{\text{BACK}}$/DRAK1	66	I/O	PD21/D21/$\overline{\text{IRQ5}}$	102	I	MD1	138	I/O	PE8/TIOC3A
31	I/O	PB2/$\overline{\text{IRQ0}}$/$\overline{\text{POE0}}$/$\overline{\text{RAS}}$	67	I/O	PD20/D20/$\overline{\text{IRQ4}}$	103	I	MD0	139	I/O	PE9/TIOC3B
32	I/O	PB3/$\overline{\text{IRQ1}}$/$\overline{\text{POE1}}$/$\overline{\text{CASL}}$	68	I/O	PD19/D19/$\overline{\text{IRQ3}}$	104	—	$PLLV_{DD}$	140	I/O	PE10/TIOC3C
33	I/O	PA18/$\overline{\text{BREQ}}$/DRAK0	69	I/O	PD18/D18/$\overline{\text{IRQ2}}$	105	I	PLLCAP	141	—	GND
34	I/O	PB4/$\overline{\text{IRQ2}}$/$\overline{\text{POE2}}$/$\overline{\text{CASH}}$	70	I/O	PD17/D17/$\overline{\text{IRQ1}}$	106	—	PLLGND	142	I/O	PE11/TIOC3D
35	—	GND	71	—	GND	107	I/O	PA15/CK	143	I/O	PE12/TIOC4A
36	I/O	PB5/$\overline{\text{IRQ3}}$/$\overline{\text{POE3}}$/RDWR	72	I/O	PD16/D16/$\overline{\text{IRQ0}}$	108	I	$\overline{\text{RES}}$/(V_{PP})	144	I/O	PE13/TIOC4B/$\overline{\text{MRES}}$

INPUT

AN0 - AN7	:	ANALOG SIGNAL
$\overline{\text{ADTRG}}$	:	A/D CONVERSION TRIGGER
$\overline{\text{BREQ}}$	:	BUS REQUEST
$\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$	:	DMA TRANSFER REQUEST
EXTAL	:	EXTERNAL CRYSTAL OSCILLATOR
$\overline{\text{IRQ0}}$ - $\overline{\text{IRQ7}}$	:	INTERRUPT REQUEST
MD0 - MD3	:	OPERATION MODE SET
$\overline{\text{MRES}}$	:	MANUAL RESET
NMI	:	NON-MASKABLE INTERRUPT REQUEST
PF0 - PF7	:	PORT F
PLLCAP	:	PLL CAPACITOR
$\overline{\text{POE0}}$ - $\overline{\text{POE3}}$	:	PORT OUTPUT ENABLE
$\overline{\text{RES}}$	:	POWER ON RESET
RDWR	:	READ/WRITE
RXD0, RXD1	:	RECEIVE DATA
TCLKA - TCLKD	:	MTU TIMER CLOCK
$\overline{\text{WAIT}}$	:	WAIT
XTAL	:	EXTERNAL CRYSTAL OSCILLATOR

OUTPUT

A0 - A21	:	ADDRESS BUS
$\overline{\text{AH}}$	:	ADDRESS HOLD
$\overline{\text{BACK}}$	:	BUS ACKNOWLEDGE
$\overline{\text{CASH}}$	:	UPPER COLUMN ADDRESS STROBE
$\overline{\text{CASHH}}$	:	HH COLUMN ADDRESS STROBE
$\overline{\text{CASHL}}$	:	HL COLUMN ADDRESS STROBE
$\overline{\text{CASL}}$	:	LOWER COLUMN ADDRESS STROBE
CK	:	SYSTEM CLOCK
$\overline{\text{CS0}}$ - $\overline{\text{CS3}}$	:	CHIP SELECT
DACK0, DACK1	:	DMA TRANSFER STROBE
DRAK0, DRAK1	:	DMA REQUEST ACKNOWLEDGMENT
$\overline{\text{IRQOUT}}$	:	INTERRUPT REQUEST
$\overline{\text{RAS}}$	:	ROW ADDRESS STROBE
$\overline{\text{RD}}$	:	READ
TXD0, TXD1	:	TRANSMIT DATA
$\overline{\text{WDTOVF}}$	:	WATCHDOG TIMER OVERFLOW
$\overline{\text{WRH}}$	:	UPPER 8-BIT WRITE
$\overline{\text{WRHH}}$	:	HH WRITE
$\overline{\text{WRHL}}$	:	HL WRITE
$\overline{\text{WRL}}$	:	LOWER 8-BIT WRITE

INPUT/OUTPUT

D0 - D31	:	DATA BUS
PA0 - PA23	:	PORT A
PB0 - PB9	:	PORT B
PC0 - PC15	:	PORT C
PD0 - PD31	:	PORT D
PE0 - PE15	:	PORT E
SCK0, SCK1	:	SERIAL CLOCK
TIOC0A - TIOC4A	:	MTU CAPTURE INPUT/COMPARE OUTPUT
TIOC0B - TIOC4B	:	MTU CAPTURE INPUT/COMPARE OUTPUT
TIOC0C, TIOC3C, TIOC4C	:	MTU CAPTURE INPUT/COMPARE OUTPUT
TIOC0D, TIOC3D, TIOC4D	:	MTU CAPTURE INPUT/COMPARE OUTPUT