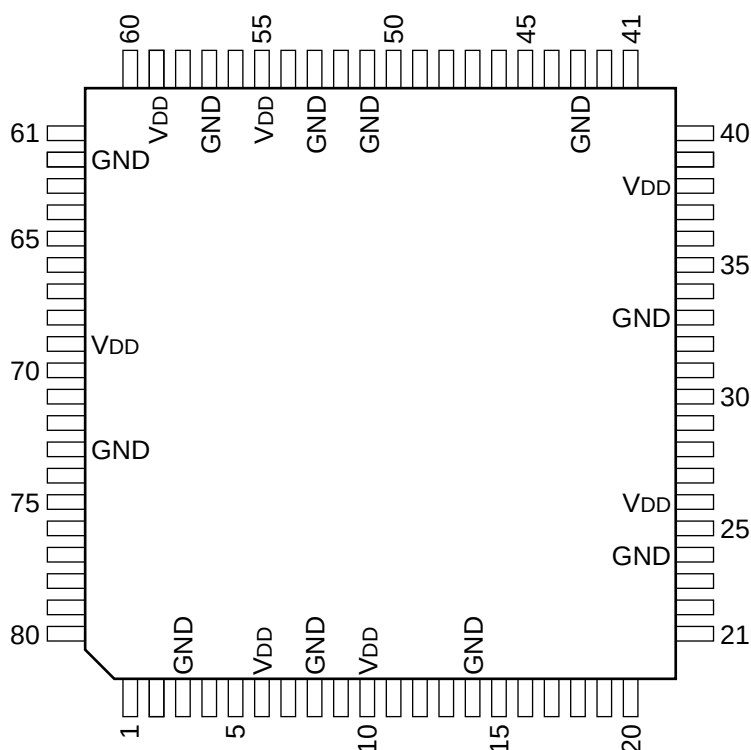


C-MOS 16-BIT GRAPHIC PROCESSOR

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I/O	D13	17	I/O	D2	33	—	GND	49	O	MCYC	65	O	FBS1
2	I/O	D12	18	I/O	D1	34	I/O	MAD11	50	O	SCLK	66	O	FBS2
3	—	GND	19	I/O	D0	35	I/O	MAD10	51	—	GND	67	O	DISP1
4	I/O	D11	20	O	MA22	36	I/O	MAD9	52	I/O	EXVSYNC/VSYNC	68	O	DISP2/CUD
5	I/O	D10	21	O	MA21	37	I/O	MAD8	53	—	GND	69	—	VDD
6	—	VDD	22	O	MA20	38	—	VDD	54	I/O	EXHSYNC/HSYNC	70	O	IRQO
7	I/O	D9	23	O	MA19	39	I/O	MAD7	55	—	VDD	71	O	DREQ
8	—	GND	24	—	GND	40	I/O	MAD6	56	I	CLKIN	72	O	READY
9	I/O	D8	25	O	MA18	41	I/O	MAD5	57	—	GND	73	—	GND
10	—	VDD	26	—	VDD	42	I/O	MAD4	58	I	RES	74	I	DACK
11	I/O	D7	27	O	MA17	43	—	GND	59	—	VDD	75	I	CS
12	I/O	D6	28	O	MA16	44	I/O	MAD3	60	I	RUN	76	I	RD
13	I/O	D5	29	I/O	MAD15	45	I/O	MAD2	61	I	HALT/IRQI	77	I	WR
14	—	GND	30	I/O	MAD14	46	I/O	MAD1	62	—	GND	78	I	RS
15	I/O	D4	31	I/O	MAD13	47	I/O	MAD0	63	O	HALT/IRQIA	79	I/O	D15
16	I/O	D3	32	I/O	MAD12	48	O	CYSTRT	64	O	FBS0	80	I/O	D14

79	D15	MA22	20	INPUT	
80	D14	MA21	21	CLKIN	; CLOCK
1	D13	MA20	22	CS	; CHIP SELECT
2	D12	MA19	23	DACK	; DMA TRANSLATE REQUEST ACKNOWLEDGE
4	D11	MA18	25	EXHSYNC	; EXTERNAL HORIZONTAL SYNC
5	D10	MA17	27	EXVSYNC	; EXTERNAL VERTICAL SYNC
7	D9	MA16	28	HALT	; HALT
9	D8			IRQI	; INTERRUPT REQUEST
11	D7	MAD15	29	RD	; READ
12	D6	MAD14	30	RES	; RESET
13	D5	MAD13	31	RS	; REGISTER SELECT
15	D4	MAD12	32	RUN	; RUN
16	D3	MAD11	34	WR	; WRITE
17	D2	MAD10	35		
18	D1	MAD9	36	OUTPUT	
19	D0	MAD8	37	CUD	; CURSOR DISPLAY TIMING
		MAD7	39	CYSTRT	; CYCLE START
		MAD6	40	DISP1, DISP2	; DISPLAY TIMING
		MAD5	41	DREQ	; DMA TRANSLATE REQUEST
		MAD4	42	FBS0-FBS2	; FRAME BUFFER STATUS
		MAD3	44	HALTA	; HALT ACKNOWLEDGE
		MAD2	45	HSYNC	; HORIZONTAL SYNC
		MAD1	46	IRQIA	; INTERRUPT REQUEST INPUT ACKNOWLEDGE
		MAD0	47	IRQO	; INTERRUPT REQUEST
				MA16 - MA22	; FRAME BUFFER ADDRESS BUS
			48	MCYC	; MEMORY CYCLE
		CYSTRT	49	READY	; READY
56	CLKIN	MCYC	50	SCLK	; S CLOCK
58	RES	SCLK	63	VSYNC	; VERTICAL SYNC
60	RUN	HALTA/IRQIA	64		
61	HALT/IRQI	FBS0	65	INPUT/OUTPUT	
74	DACK	FBS1	66	D0 - D15	; DATA BUS
75	CS	DISP1	67	MAD0 - MAD15	; FRAME BUFFER ADDRESS/DATA BUS
76	RD	DISP2/CUD	68		
77	WR	IRQO	70		
78	RS	DREQ	71		
		READY	72		
52	EXVSYNC/VSYNC				
54	EXHSYNC/HSYNC				

