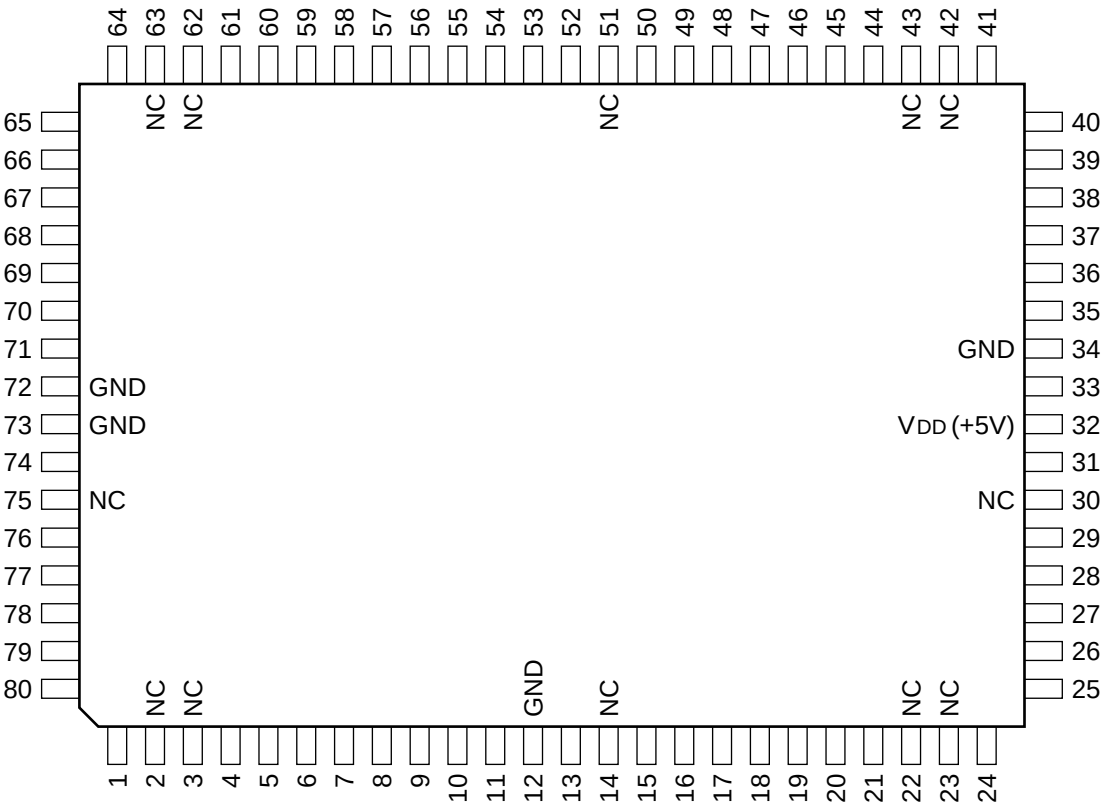
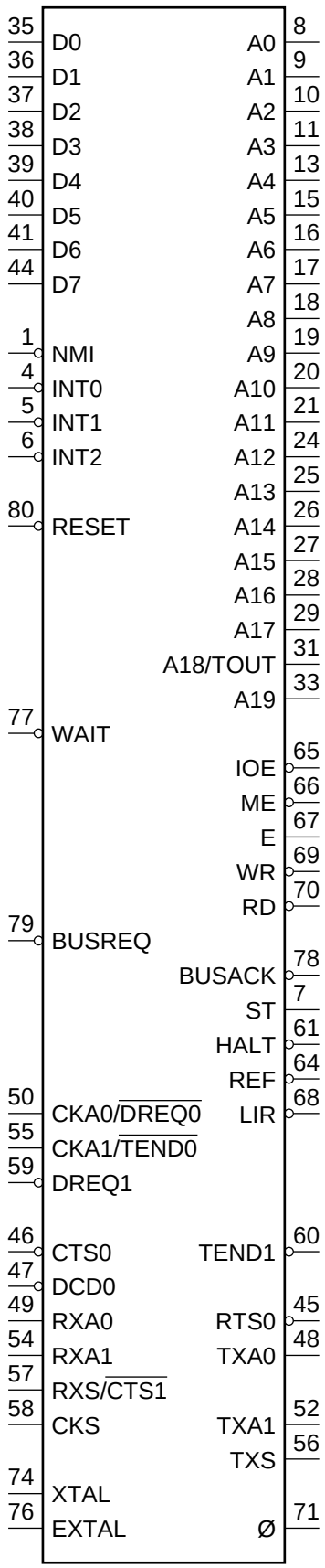
C-MOS 8-BIT MICROPROCESSOR

- TOP VIEW -

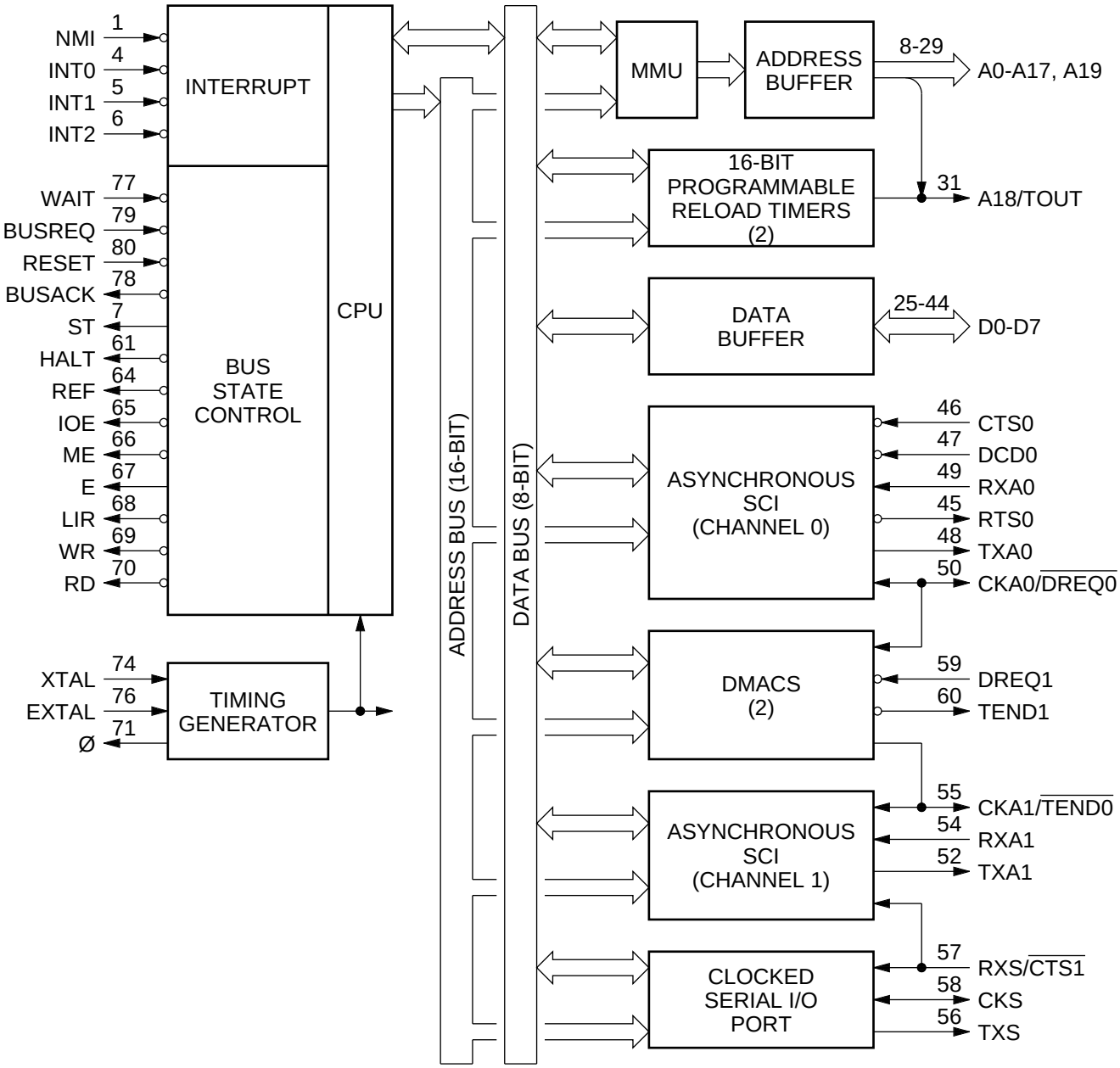


(VDD =+5V)

PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	$\overline{\text{NMI}}$	21	O	A11	41	I/O	D6	61	O	$\overline{\text{HALT}}$
2	–	NC	22	–	NC	42	–	NC	62	–	NC
3	–	NC	23	–	NC	43	–	NC	63	–	NC
4	I	$\overline{\text{INT0}}$	24	O	A12	44	I/O	D7	64	O	$\overline{\text{REF}}$
5	I	$\overline{\text{INT1}}$	25	O	A13	45	O	$\overline{\text{RTS0}}$	65	O	$\overline{\text{IOE}}$
6	I	$\overline{\text{INT2}}$	26	O	A14	46	I	$\overline{\text{CTS0}}$	66	O	$\overline{\text{ME}}$
7	O	ST	27	O	A15	47	I	$\overline{\text{DCD0}}$	67	O	E
8	O	A0	28	O	A16	48	O	TXA0	68	O	$\overline{\text{LIR}}$
9	O	A1	29	O	A17	49	I	RXA0	69	O	$\overline{\text{WR}}$
10	O	A2	30	–	NC	50	I/O	CKA0/$\overline{\text{DREQ0}}$	70	O	$\overline{\text{RD}}$
11	O	A3	31	O	A18/TOUT	51	–	NC	71	O	Ø
12	–	GND	32	–	VDD	52	O	TXA1	72	–	GND
13	O	A4	33	O	A19	53	–	TEST	73	–	GND
14	–	NC	34	–	GND	54	I	RXA1	74	I	XTAL
15	O	A5	35	I/O	D0	55	I/O	CKA1/$\overline{\text{TEND0}}$	75	–	NC
16	O	A6	36	I/O	D1	56	O	TXS	76	I	EXTAL
17	O	A7	37	I/O	D2	57	I	RXS/$\overline{\text{CTS1}}$	77	I	$\overline{\text{WAIT}}$
18	O	A8	38	I/O	D3	58	I/O	CKS	78	O	$\overline{\text{BUSACK}}$
19	O	A9	39	I/O	D4	59	I	$\overline{\text{DREQ1}}$	79	I	$\overline{\text{BUSREQ}}$
20	O	A10	40	I/O	D5	60	O	$\overline{\text{TEND1}}$	80	I	$\overline{\text{RESET}}$



A0-A19	; ADDRESS BUS (3-STATE)
BUSACK	; BUS ACKNOWLEDGE
BUSREQ	; BUS REQUEST
CKA0, 1	; CLOCK FOR ASYNCHRONOUS SCI CHANNEL 0, 1
CKS	; CLOCK FOR SERIAL I/O PORT
CTS0, 1	; CLEAR TO SEND FOR ASYNCHRONOUS SCI CHANNEL 0, 1
D0-D7	; DATA BUS
DCD0	; DATA CARRIER DETECT FOR ASYNCHRONOUS SCI CHANNEL 0
DREQ0,1	; DMA REQUEST FOR CHANNEL 0, 1
E	; ENABLE
EXTAL	; EXTERNAL CLOCK
INT0-2	; INTERRUPT 0-2
IOE	; I/O ENABLE (3-STATE)
LIR	; LOAD INSTRUCTION REGISTER
ME	; MEMORY ENABLE (3-STATE)
NMI	; NON-MASKABLE INTERRUPT
RD	; READ
REF	; REFRESH
RTS0	; REQUEST TO SEND FOR ASYNCHRONOUS SCI CHANNEL 0
RXA0, 1	; RECEIVE DATA FOR ASYNCHRONOUS SCI CHANNEL 0, 1
RXS	; RECEIVE DATA FOR SERIAL I/O PORT
ST	; STATUS
TEND0, 1	; TRANSFER END FOR CHANNEL 0, 1
TOUT	; TIMER OUT
TXA0,1	; TRANSFER DATA FOR ASYNCHRONOUS SCI CHANNEL 0, 1
TXS	; TRANSFER DATA FOR SERIAL I/O PORT
WR	; WRITE (3-STATE)
Ø	; SYSTEM CLOCK


NMI
INT0
INT1
INT2
1
4
5
6
INTERRUPT
WAIT
BUSREQ
RESET
BUSACK
ST
HALT
REF
IOE
ME
E
LIR
WR
RD
77
79
80
78
7
61
64
65
66
67
68
69
70
BUS STATE CONTROL
CPU
XTAL
EXTAL
Ø
74
76
71
TIMING GENERATOR
ADDRESS BUS (16-BIT)
DATA BUS (8-BIT)
MMU
ADDRESS BUFFER
8-29
A0-A17, A19
16-BIT PROGRAMMABLE RELOAD TIMERS (2)
31
A18/TOUT
DATA BUFFER
25-44
D0-D7
ASYNCHRONOUS SCI (CHANNEL 0)
46
CTS0
47
DCD0
49
RXA0
45
RTS0
48
TXA0
50
CKA0/DREQ0
DMACS (2)
59
DREQ1
60
TEND1
ASYNCHRONOUS SCI (CHANNEL 1)
55
CKA1/TEND0
54
RXA1
52
TXA1
CLOCKED SERIAL I/O PORT
57
RXS/CTS1
58
CKS
56
TXS