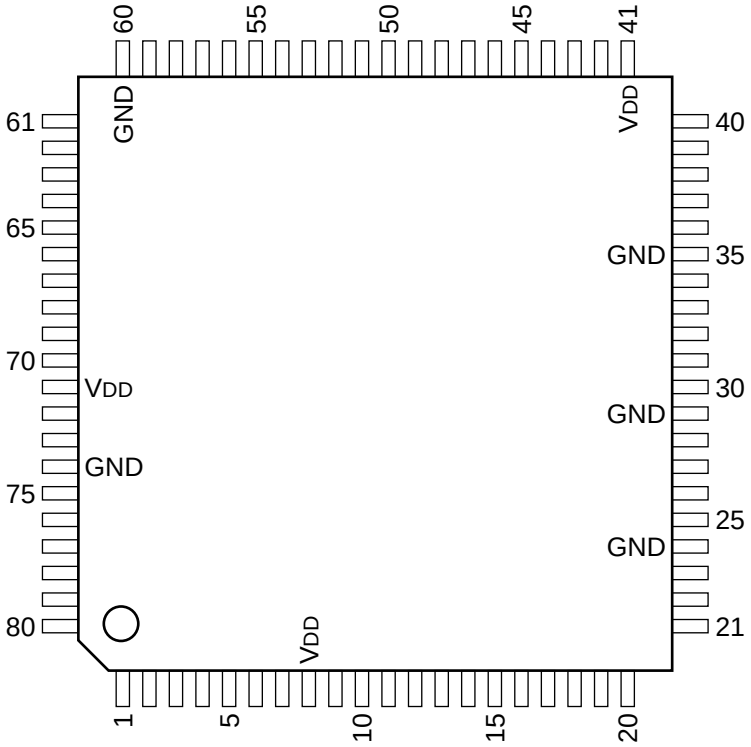
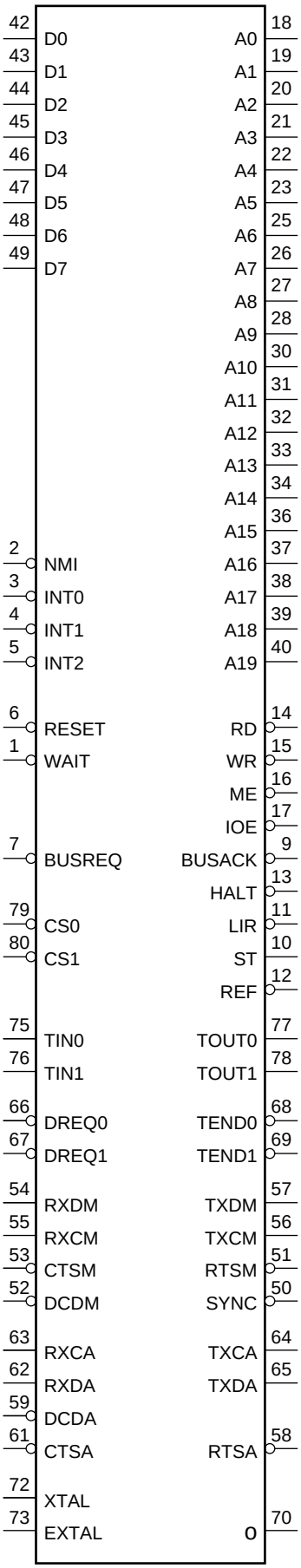
C-MOS 8-BIT MICROPROCESSOR

—TOP VIEW—



PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL	PIN No.	I/O	SIGNAL
1	I	$\overline{\text{WAIT}}$	17	O	$\overline{\text{IOE}}$	33	O	A13	49	I/O	D7	65	O	TXDA
2	I	$\overline{\text{NMI}}$	18	O	A0	34	O	A14	50	I/O	$\overline{\text{SYNC}}$	66	I	$\overline{\text{DREQ0}}$
3	I	$\overline{\text{INT0}}$	19	O	A1	35	—	GND	51	O	$\overline{\text{RTSM}}$	67	I	$\overline{\text{DREQ1}}$
4	I	$\overline{\text{INT1}}$	20	O	A2	36	O	A15	52	I	$\overline{\text{DCDM}}$	68	O	$\overline{\text{TEND0}}$
5	I	$\overline{\text{INT2}}$	21	O	A3	37	O	A16	53	I	$\overline{\text{CTSM}}$	69	O	$\overline{\text{TEND1}}$
6	I	$\overline{\text{RESET}}$	22	O	A4	38	O	A17	54	I	RXDM	70	O	o
7	I	$\overline{\text{BUSREQ}}$	23	O	A5	39	O	A18	55	I/O	RXCM	71	—	VDD
8	—	VDD	24	—	GND	40	O	A19	56	I/O	TXCM	72	I	XTAL
9	O	$\overline{\text{BUSACK}}$	25	O	A6	41	—	VDD	57	O	TXDM	73	I	EXTAL
10	O	ST	26	O	A7	42	I/O	D0	58	O	$\overline{\text{RTSA}}$	74	—	GND
11	O	$\overline{\text{LIR}}$	27	O	A8	43	I/O	D1	59	I	$\overline{\text{DCDA}}$	75	I	TIN0
12	O	$\overline{\text{REF}}$	28	O	A9	44	I/O	D2	60	—	GND	76	I	TIN1
13	O	$\overline{\text{HALT}}$	29	—	GND	45	I/O	D3	61	I	$\overline{\text{CTSA}}$	77	O	TOUT0
14	O	$\overline{\text{RD}}$	30	O	A10	46	I/O	D4	62	I	RXDA	78	O	TOUT1
15	O	$\overline{\text{WR}}$	31	O	A11	47	I/O	D5	63	I/O	RXCA	79	O	$\overline{\text{CS0}}$
16	O	$\overline{\text{ME}}$	32	O	A12	48	I/O	D6	64	I/O	TXCA	80	O	$\overline{\text{CS1}}$



INPUT

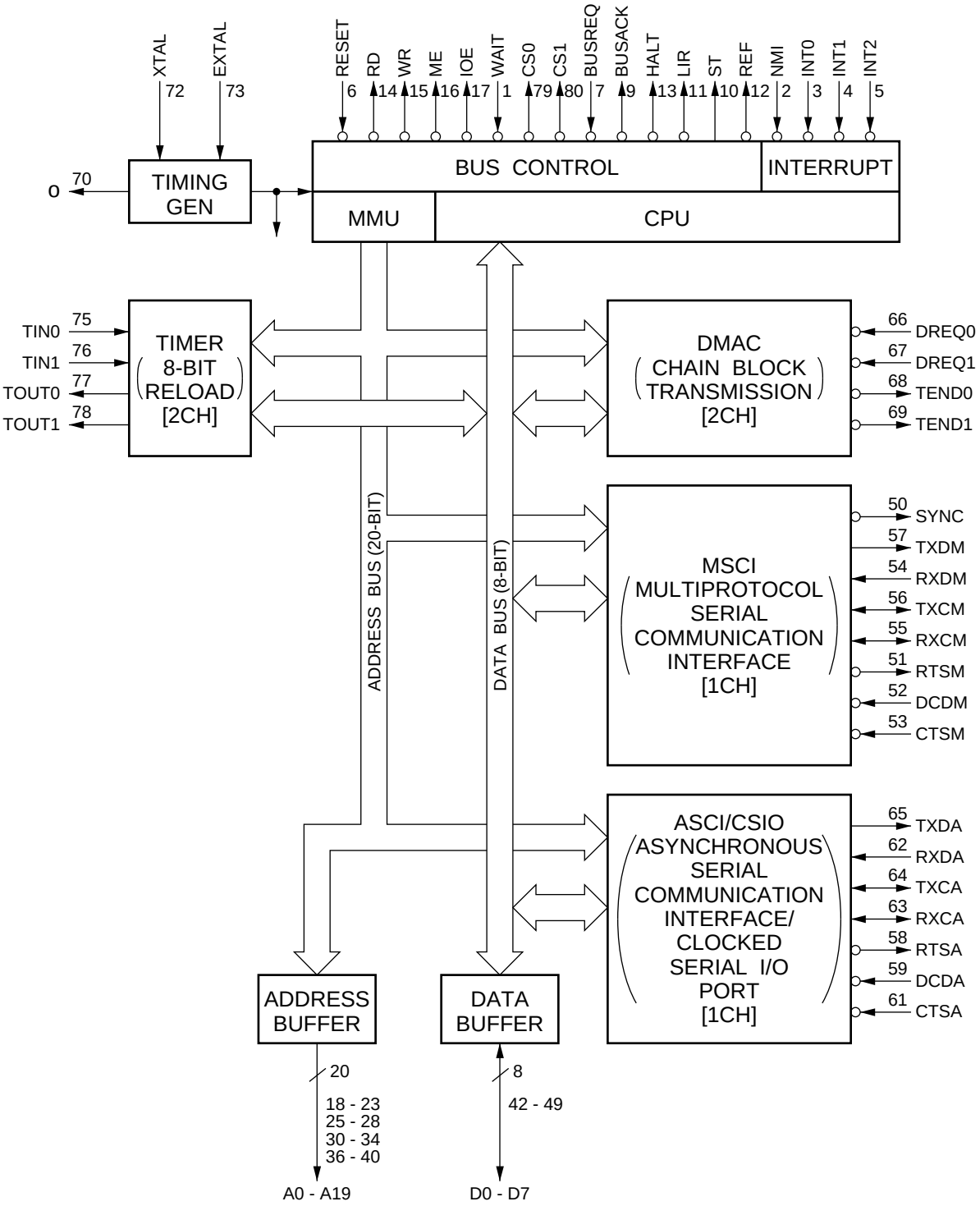
$\overline{\text{BUSREQ}}$; BUS REQUEST
$\overline{\text{CTSA}}$; CLEAR TO SEND FOR ASCI/CSIO
$\overline{\text{CTSM}}$; CLEAR TO SEND FOR MSCI
$\overline{\text{DCDA}}$; DATA CARRIER DETECT FOR ASCI/CSIO
$\overline{\text{DCDM}}$; DATA CARRIER DETECT FOR MSCI
$\overline{\text{DREQ0}}$, $\overline{1}$; DMA REQUEST FOR CHANNEL
EXTAL ; EXTERNAL CLOCK INPUT/CRYSTAL CONNECTION
$\overline{\text{INT0}}$, $\overline{1}$, $\overline{2}$; INTERRUPT 0, 1, 2
$\overline{\text{NMI}}$; NON-MASKABLE INTERRUPT
$\overline{\text{RESET}}$; RESET
RXDA ; RECEIVE DATA FOR ASCI/CSIO
RXDM ; RECEIVE DATA FOR MSCI
$\overline{\text{TIN0}}$, 1 ; TIMER INPUT FOR CHANNEL 0, 1
$\overline{\text{WAIT}}$; WAIT
XTAL ; CRYSTAL CONNECTION

OUTPUT

A0 - A19 ; ADDRESS BUS
$\overline{\text{BUSACK}}$; BUS ACKNOWLEDGE
$\overline{\text{CS0}}$, $\overline{1}$; CHIP SELECT 0, 1
$\overline{\text{HALT}}$; HALT
$\overline{\text{IOE}}$; I/O ENABLE
$\overline{\text{LIR}}$; LOAD INSTRUCTION REGISTER
$\overline{\text{ME}}$; MEMORY ENABLE
$\overline{\text{RD}}$; READ
$\overline{\text{REF}}$; REFRESH
$\overline{\text{RTSA}}$; REQUEST TO SEND FOR ASCI/CSIO
$\overline{\text{RTSM}}$; REQUEST TO SEND FOR MSCI
ST ; STATUS
$\overline{\text{TEND0}}$, $\overline{1}$; TRANSFER END FOR CHANNEL 0, 1
TOUT0, 1 ; TIMER OUTPUT FOR CHANNEL 0, 1
TXDA ; TRANSMIT DATA FOR ASCI/CSIO
TXDM ; TRANSMIT DATA FOR MSCI
$\overline{\text{WR}}$; WRITE
O ; SYSTEM CLOCK

INPUT/OUTPUT

D0 - D7 ; DATA BUS
RXCA ; RECEIVE CLOCK FOR ASCI/CSIO
RXCM ; RECEIVE CLOCK FOR MSCI
$\overline{\text{SYNC}}$; SYNCHRONIZATION FOR MSCI
TXCA ; TRANSMIT CLOCK FOR ASCI/CSIO
TXCM ; TRANSMIT CLOCK FOR MSCI


XTAL
72
EXTAL
73
RESET
6
RD
14
WR
15
ME
16
IOE
17
WAIT
1
CS0
79
CS1
80
BUSREQ
7
BUSACK
9
HALT
13
LIR
11
ST
10
REF
12
NMI
2
INT0
3
INT1
4
INT2
5
70
TIMING GEN
BUS CONTROL
INTERRUPT
MMU
CPU
TIN0
75
TIN1
76
TOUT0
77
TOUT1
78
TIMER 8-BIT RELOAD [2CH]
DMAC CHAIN BLOCK TRANSMISSION [2CH]
66
DREQ0
67
DREQ1
68
TEND0
69
TEND1
ADDRESS BUS (20-BIT)
DATA BUS (8-BIT)
MSCI MULTIPROTOCOL SERIAL COMMUNICATION INTERFACE [1CH]
50
SYNC
57
TXDM
54
RXDM
56
TXCM
55
RXCM
51
RTSM
52
DCDM
53
CTSM
ASCI/CSIO ASYNCHRONOUS SERIAL COMMUNICATION INTERFACE/ CLOCKED SERIAL I/O PORT [1CH]
65
TXDA
62
RXDA
64
TXCA
63
RXCA
58
RTSA
59
DCDA
61
CTSA
ADDRESS BUFFER
DATA BUFFER
20
18 - 23
25 - 28
30 - 34
36 - 40
A0 - A19
8
42 - 49
D0 - D7