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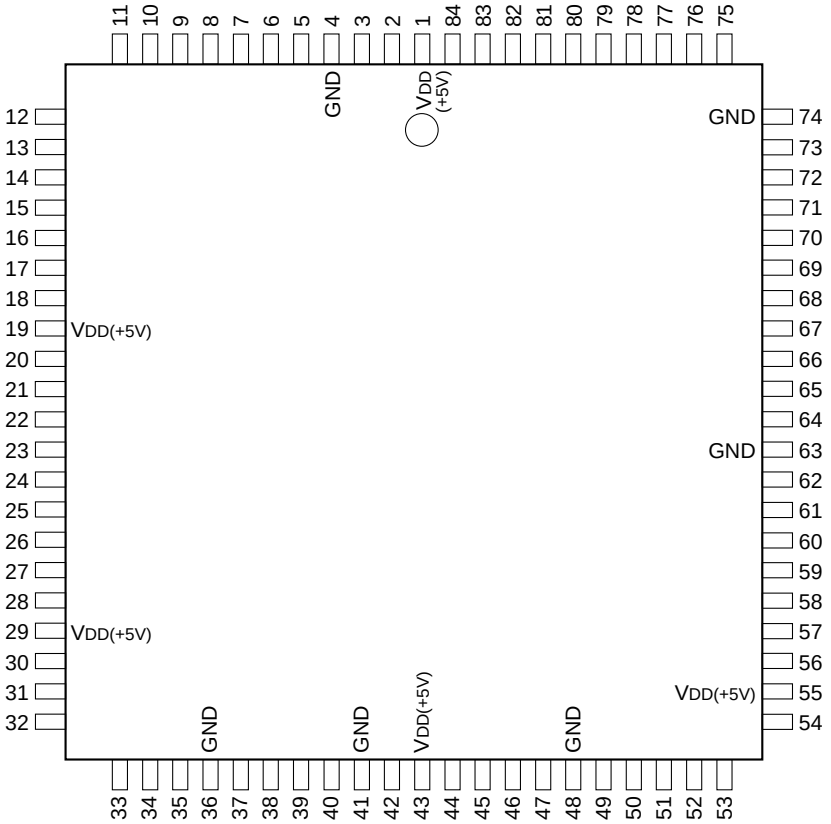
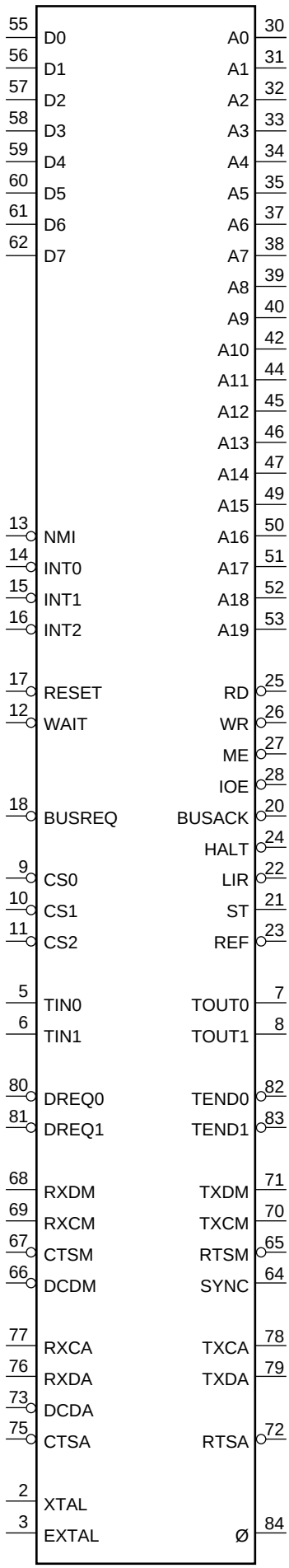
C-MOS 8-BIT MICROPROCESSOR

–TOP VIEW–



(VDD= +5V)

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VDD	22	O	$\overline{\text{LIR}}$	43	—	VDD	64	I/O	$\overline{\text{SYNC}}$
2	I	XTAL	23	O	$\overline{\text{REF}}$	44	O	A11	65	O	$\overline{\text{RTSM}}$
3	I	EXTAL	24	O	$\overline{\text{HALT}}$	45	O	A12	66	I	$\overline{\text{DCDM}}$
4	—	GND	25	O	$\overline{\text{RD}}$	46	O	A13	67	I	$\overline{\text{CTSM}}$
5	I	TIN0	26	O	$\overline{\text{WR}}$	47	O	A14	68	I	RXDM
6	I	TIN1	27	O	$\overline{\text{ME}}$	48	—	GND	69	I/O	RXCM
7	O	TOUT0	28	O	$\overline{\text{IOE}}$	49	O	A15	70	I/O	TXCM
8	O	TOUT1	29	—	VDD	50	O	A16	71	O	TXDM
9	O	$\overline{\text{CS0}}$	30	O	A0	51	O	A17	72	O	$\overline{\text{RTSA}}$
10	O	$\overline{\text{CS1}}$	31	O	A1	52	O	A18	73	I	$\overline{\text{DCDA}}$
11	O	$\overline{\text{CS2}}$	32	O	A2	53	O	A19	74	—	GND
12	I	$\overline{\text{WAIT}}$	33	O	A3	54	—	VDD	75	I	$\overline{\text{CTSA}}$
13	I	$\overline{\text{MNI}}$	34	O	A4	55	I/O	D0	76	I	RXDA
14	I	$\overline{\text{INT0}}$	35	O	A5	56	I/O	D1	77	I/O	RXCA
15	I	$\overline{\text{INT1}}$	36	—	GND	57	I/O	D2	78	I/O	TXCA
16	I	$\overline{\text{INT2}}$	37	O	A6	58	I/O	D3	79	O	TXDA
17	I	$\overline{\text{RESET}}$	38	O	A7	59	I/O	D4	80	I	$\overline{\text{DREQ0}}$
18	I	$\overline{\text{BUSREQ}}$	39	O	A8	60	I/O	D5	81	I	$\overline{\text{DREQ1}}$
19	—	VDD	40	O	A9	61	I/O	D6	82	O	$\overline{\text{TEND0}}$
20	O	$\overline{\text{BUSACK}}$	41	—	GND	62	I/O	D7	83	O	$\overline{\text{TEND1}}$
21	O	ST	42	O	A10	63	—	GND	84	O	Ø



INPUT

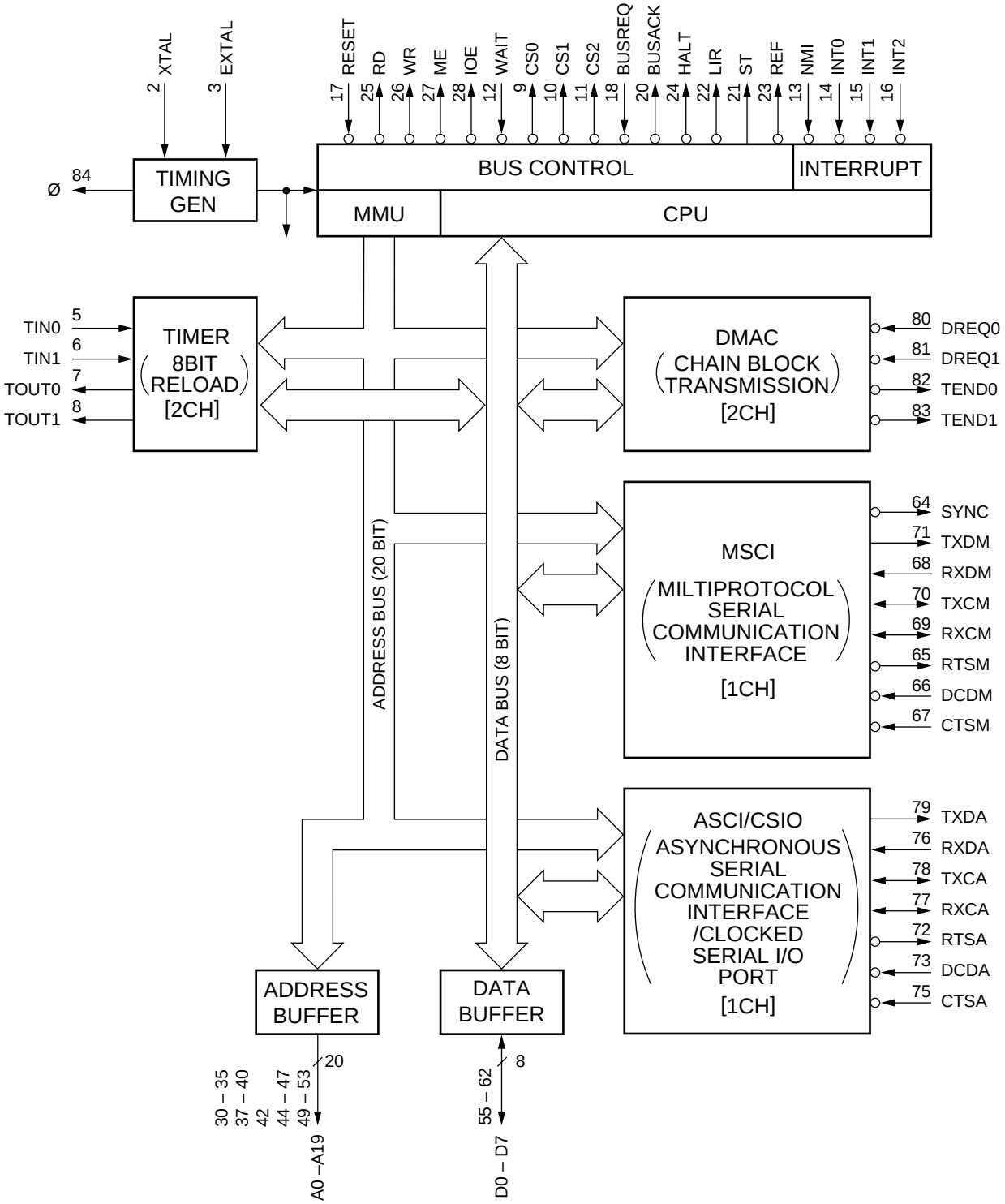
$\overline{\text{BUSREQ}}$	;	BUS REQUEST
$\overline{\text{CTSA}}$	;	CLEAR TO SEND FOR ASCI/CSIO
$\overline{\text{CTSM}}$	;	CLEAR TO SEND FOR MSCI
$\overline{\text{DCDA}}$	;	DATA CARRIER DETECT FOR ASCI/CSIO
$\overline{\text{DCDM}}$	;	DATA CARRIER DETECT FOR MSCI
$\overline{\text{DREQ0}}$, $\overline{1}$	;	DMA REQUEST FOR CHANNEL
EXTAL	;	EXTERNAL CLOCK INPUT/CRYSTAL CONNECTION
$\overline{\text{INT0}}$, $\overline{1}$, $\overline{2}$	;	INTERRUPT 0, 1, 2
$\overline{\text{NMI}}$	;	NON-MASKABLE INTERRUPT
$\overline{\text{RESET}}$	;	RESET
RXDA	;	RECEIVE DATA FOR ASCI/CSIO
RXDM	;	RECEIVE DATA FOR MSCI
TIN0, 1	;	TIMER INPUT FOR CHANNEL 0, 1
$\overline{\text{WAIT}}$	;	WAIT
XTAL	;	CRYSTAL CONNECTION

OUTPUT

A0 – A19	;	ADDRESS BUS
$\overline{\text{BUSACK}}$	;	BUS ACKNOWLEDGE
$\overline{\text{CS0}}$, $\overline{1}$, $\overline{2}$	;	CHIP SELECT 0, 1, 2
$\overline{\text{HALT}}$	;	HALT
$\overline{\text{IOE}}$	;	I/O ENABLE
$\overline{\text{LIR}}$	;	LOAD INSTRUCTION REGISTER
$\overline{\text{ME}}$	;	MEMORY ENABLE
$\overline{\text{RD}}$	;	READ
$\overline{\text{REF}}$	;	REFRESH
$\overline{\text{RTSA}}$	;	REQUEST TO SEND FOR ASCI/CSIO
$\overline{\text{RTSM}}$	;	REQUEST TO SEND FOR MSCI
ST	;	STATUS
$\overline{\text{TEND0}}$, $\overline{1}$	;	TRANSFER END FOR CHANNEL 0, 1
TOUT0, 1	;	TIMER OUTPUT FOR CHANNEL 0, 1
TXDA	;	TRANSMIT DATA FOR ASCI/CSIO
TXDM	;	TRANSMIT DATA FOR MSCI
$\overline{\text{WR}}$	;	WRITE
Ø	;	SYSTEM CLOCK

INPUT/OUTPUT

D0 – D7	;	DATA BUS
RXCA	;	RECEIVE CLOCK FOR ASCI/CSIO
RXCM	;	RECEIVE CLOCK FOR MSCI
SYNC	;	SYNCHRONIZATION FOR MSCI
TXCA	;	TRANSMIT CLOCK FOR ASCI/CSIO
TXCM	;	TRANSMIT CLOCK FOR MSCI


2 XTAL
3 EXTAL
17 RESET
25 RD
26 WR
27 ME
28 IOE
12 WAIT
9 CS0
10 CS1
11 CS2
18 BUSREQ
20 BUSACK
24 HALT
22 LIR
21 ST
23 REF
13 NMI
14 INT0
15 INT1
16 INT2
Ø 84
TIMING GEN
BUS CONTROL
INTERRUPT
MMU
CPU
TIN0 5
TIN1 6
TOUT0 7
TOUT1 8
TIMER (8BIT RELOAD) [2CH]
DMAC (CHAIN BLOCK TRANSMISSION) [2CH]
80 DREQ0
81 DREQ1
82 TEND0
83 TEND1
ADDRESS BUS (20 BIT)
DATA BUS (8 BIT)
MSCI (MILTIPROTOCOL SERIAL COMMUNICATION INTERFACE) [1CH]
64 SYNC
71 TXDM
68 RXDM
70 TXCM
69 RXCM
65 RTSM
66 DCDM
67 CTSM
ASCI/CSIO (ASYNCHRONOUS SERIAL COMMUNICATION INTERFACE /CLOCKED SERIAL I/O PORT) [1CH]
79 TXDA
76 RXDA
78 TXCA
77 RXCA
72 RTSA
73 DCDA
75 CTSA
ADDRESS BUFFER
DATA BUFFER
20
8
30 – 35
37 – 40
42
44 – 47
49 – 53
A0 –A19
55 – 62
D0 – D7