Addendum to
MC68HC705P6
HCMOS Microcontroller Unit
Technical Data

This addendum provides corrections and additions to the *MC68HC705P6 Technical Data*, Rev. 1 (Motorola document number MC68HC705P6/D).

1. Page 1-1, section **1.1 Features** — Change the third bulleted item as follows:

   From:

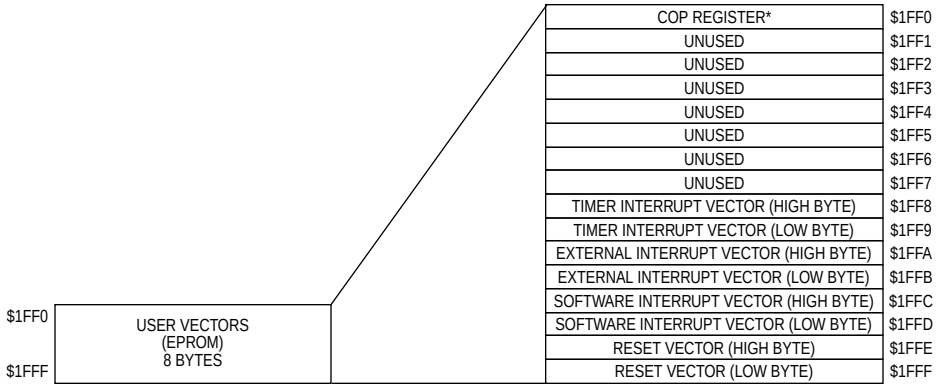
   - 4672 Bytes of User EPROM/OTPROM Including 48 Bytes of Page Zero EPROM/OTPROM and 16 User Vector Locations

   To:

   - 4672 Bytes of User EPROM/OTPROM Including 48 Bytes of Page Zero EPROM/OTPROM and 8 User Vector Locations

2. Page 2-2, **Figure 2-1. Memory Map** — Change the USER VECTORS portion at the bottom of the map as follows:

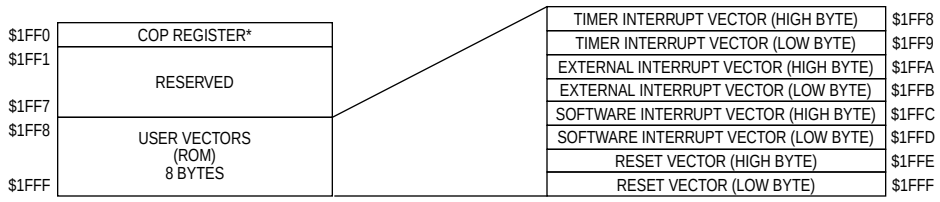
From:



*Writing zero to bit 0 of $1FF0 clears the COP watchdog timer. Reading $1FF0 returns user ROM data.

Figure 2-1. Memory Map

To:



*Writing zero to bit 0 of $1FF0 clears the COP watchdog timer.

Figure 2-1. Memory Map

3. Page 2-4, section **2.4 ROM** — Change the third bulleted item as follows:

   From:

   - Addresses $1FF0–$1FFF contain 16 bytes of EPROM/OTPROM reserved for vectors.

   To:

   - Addresses $1FF8–$1FFF contain 8 bytes of EPROM/OTPROM for user vectors.

4. Page 5-2, section **5.1.3 Computer Operating Properly (COP) Watchdog Reset** — Change the last sentence in the first paragraph as follows:

   From:

   A timeout of the 18-stage ripple counter in the COP watchdog generates a COP reset. The COP watchdog is part of a software error detection system and must be cleared periodically to start a new timeout period. With a 4-MHz oscillator, the COP timeout period is 65.5 ms. To clear the COP watchdog and prevent a COP reset, write a logic zero to bit 0 (COPC) of the COP register at location $1FF0. The COP register, shown in Figure 5-3, is a write-only register that returns the contents of an EPROM location when read.

   To:

   A timeout of the 18-stage ripple counter in the COP watchdog generates a COP reset. The COP watchdog is part of a software error detection system and must be cleared periodically to start a new timeout period. With a 4-MHz oscillator, the COP timeout period is 65.5 ms. To clear the COP watchdog and prevent a COP reset, write a logic zero to bit 0 (COPC) of the COP register at location $1FF0. The COP register, shown in Figure 5-3, is a write-only register that returns the contents of EPROM location $1FF0 when read.

5. Page 5-2, section **5.1.3 Computer Operating Properly (COP) Watchdog Reset** — Add the following note after the first paragraph:

   Use the following formula to calculate the COP timeout period:

$$\text{COP Timeout Period} = \frac{131{,}072}{f_{BUS}}$$

   where

$$f_{BUS} = \frac{\text{crystal frequency}}{2}$$

6. Page 5-3, section **5.2.2 I/O Port Registers** — Change the first paragraph and the first bulleted item as follows:

   From:

   A reset has the following effects on I/O port registers:

   - Clears data direction registers A, B, C, and D so that all I/O port pins are inputs (PD7/TCAP remains an input-only pin.)

   To:

   A reset has the following effects on I/O port registers (even if the system clock is absent):

   - Clears data direction registers A, B, C, and D so that all I/O port pins are inputs (PD7/TCAP remains an input-only pin and TCMP remains an output-only pin.)

7. Page 7-5, **Figure 7-5. Data Direction Register B (DDRB)** — Change the abbreviation DDRC to DDRB as follows:

   From:

   DDRC — Data Direction Register B **$0005**

   To:

   DDRB — Data Direction Register B **$0005**

8. Page 7-7, section **7-4 Port C** — Change the paragraph as follows:

From:

Port C is an 8-bit general-purpose bidirectional I/O port that shares five of its pins with the analog-to-digital converter (ADC) subsystem. The five shared pins are available for general-purpose I/O functions when the ADC is disabled. While the ADC is enabled, writing to bits PC7–3 of the port C data register or to bits DDRC7–3 of data direction register C can produce unpredictable ADC results. **(See 10.2.1 ADC Status and Control Register (ADSCR)**.)

To:

Port C is an 8-bit general-purpose bidirectional I/O port that shares five of its pins with the analog-to-digital converter (ADC). The five shared pins are available for general-purpose I/O functions when the ADC is disabled.

When the ADC is turned on, the PC7/V_{RH} pin is the positive reference voltage pin for the ADC. Pins PC6/AN0, PC5/AN1, PC4/AN2, and PC3/AN3 become analog inputs. Software can select one of these four pins as the input channel to the ADC.

Unused analog input pins can be used as digital inputs, but no analog input pin can be used as a digital output while the ADC is on. Only pins PC0–PC2 can be used as digital outputs when the ADC is on.

The port C data register reads normally while the ADC is on, except that the bit corresponding to the currently selected ADC input pin reads as logic zero. Writing to bits PC7–PC3 or to bits DDRC7–DDRC3 while the ADC is on can produce unpredictable ADC results.

9. Page 8-6, **Figure 8-5. Timer Status Register (TSR)** — Correct the address of the timer status register as follows:

From:

TSR — Timer Status Register **$0012**

	Bit 7	6	5	4	3	2	1	Bit 0
	ICF	OCF	TOF	0	0	0	0	0
RESET:	U	U	U	0	0	0	0	0

U = UNAFFECTED

Figure 8-5. Timer Status Register (TSR)

To:

TSR — Timer Status Register **$0013**

	Bit 7	6	5	4	3	2	1	Bit 0
	ICF	OCF	TOF	0	0	0	0	0
RESET:	U	U	U	0	0	0	0	0

U = UNAFFECTED

Figure 8-5. Timer Status Register (TSR)

10. Page 9-2, section **9.1.1 SIOP Pin Functions** — Replace the two paragraphs as follows:

From:

The SIOP uses the three port B I/O pins. Setting the SPE bit in the SIOP control register enables the SIOP. When the SPE bit is set, the PB7/SCK, PB6/SDI, and PB5/SDO pins are dedicated to SIOP functions. When the SPE bit is clear, the PB7/SCK, PB6/SDI, and PB5/SDO are bidirectional port B I/O pins.

Setting the MSTR bit in the SIOP control register configures the SIOP for master mode. In master mode, the PB7/SCK pin is the serial clock output. PB6/SDI is the serial data input pin, and PB5/SDO is the serial data output pin. The master MCU initiates and controls the transmission of data to and from one or more slave peripheral devices. In master mode, a transmission is initiated by writing to the SIOP data register. Data written to the SIOP data register is parallel-loaded and shifted out serially to the slave device(s).

To:

PB7/SCK, PB6/SDI, and PB5/SDO form the three-bit shared-function I/O port B. The port B pins can be either the SIOP I/O pins or general-purpose I/O pins.

NOTE

Do not use port B for general-purpose I/O while the SIOP is enabled.

When bit 6 (SPE) of the SIOP control register (SCR) is set, the SIOP is enabled and port B is dedicated to SIOP functions. Clearing SPE disables the SIOP and port B reverts to standard parallel I/O.

NOTE

Enabling and then disabling the SIOP configures data direction register B for SIOP operation and can also change the port B data register. After disabling the SIOP, initialize data direction register B and the port B data register as your application requires.

When the master mode select bit (MSTR) in the SIOP control register is set, the SIOP is configured for master mode. The PB7/SCK pin is an output whose signal is derived from the internal clock. PB6/SDI is the serial input, and PB5/SDO is the serial output. The master MCU initiates and controls the transfer of data to and from one or more slave peripheral devices. In master mode, a transmission is initiated by writing to the SIOP data register (SDR). Data written to the SDR is parallel-loaded and shifted out serially to the slave device(s).

After SPE is set, the PB5/SDO output driver can be disabled by writing a zero to DDRB5, configuring PB5/SDO as a high-impedance input.

When MSTR is a clear, the SIOP is configured for slave mode. PB6/SDI and PB5/SDO have the same functions as they do in master mode, but PB7/SCK is configured as an input.

11. Page 9-5. Replace the description of the SPE bit as follows:

From:

SPE — SIOP Enable

This read/write bit enables the SIOP. Clearing the SPE bit during a transmission aborts the transmission and returns port B to its normal I/O function. After clearing the SPE bit, be sure to initialize the port B data direction register for the intended port B I/O use. Resets clear SPE.

1 = SIOP enabled
0 = SIOP disabled

To:

SPE — SIOP Enable

This read/write bit enables the SIOP. Setting SPE initializes data direction register B as follows:

- PB6/SDI is an input.
- PB5/SDO is an output.
- PB7/SCK is an input in slave mode or an output in master mode.

Clearing SPE disables the SIOP and returns port B to its normal I/O functions. Data direction register B and the port B data register remain in their SIOP-initialized state. After clearing SPE, be sure to initialize port B for its intended I/O use.

Clearing SPE during a transmission aborts the transmission, resets the bit counter, and returns port B to its normal I/O function. Reset clears SPE.

1 = SIOP enabled
0 = SIOP disabled

12. Page 9-6. Replace the descriptions for the SPIF bit and the DCOL bit as follows:

From:

SPIF — SIOP Interrupt Flag

This clearable, read-only bit is set automatically at the end of a transmission. Clear the SPIF bit by reading the SIOP status register with SPIF set, and then reading or writing the SIOP data register. Resets clear the SPIF bit.

1 = Serial transmission complete
0 = Serial transmission not complete

DCOL — Data Collision

This clearable, read-only bit is set if the SIOP data register is read or written during a transmission. Clear the DCOL bit by reading the SIOP status register with the SPIF bit set, and then reading or writing the SIOP data register. Resets clear the DCOL bit.

1 = Invalid access of SIOP data register
0 = No invalid access of SIOP data register

To:

SPIF — SIOP Interrupt Flag

This clearable, read-only bit is set automatically on the eighth rising edge of SCK and indicates that a data transfer took place. SPIF does not inhibit further transmissions. Clear SPIF by reading the SIOP status register while SPIF is set and then reading or writing the SIOP data register. Reset clears SPIF.

DCOL — Data Collision Flag

This clearable, read-only bit is automatically set if the SIOP data register is accessed while a data transfer is in progress. Reading or writing the SIOP data register while a transfer is in progress results in invalid data being transmitted or read. Clear DCOL by reading the SIOP status register with SPIF set and then accessing the SIOP data register. Because the clearing sequence accesses the SIOP data register, the sequence has to be completed before another transmission starts or DCOL is set again.

To clear DCOL when SPIF is not set, turn off the SIOP by writing a zero to SPE and then turn it back on by writing a one to SPE. Reset clears DCOL.

13. Page 9-6, **Figure 9-6. SIOP Data Register (SDR)** — Change the reset states as follows:

From:

SDR — SIOP Data Register **$000C**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	0	0	0	0	0	0	0	0

Figure 9-6. SIOP Data Register (SDR)

To:

SDR — SIOP Data Register **$000C**

	Bit 7	6	5	4	3	2	1	Bit 0
RESET:	UNAFFECTED BY RESET							

Figure 9-6. SIOP Data Register (SDR)

14. Page 10-2, section **10.1 ADC Operation** — Change the second paragraph as follows:

From:

A comparator makes successive comparisons to the selected analog input and the output of a precision digital-to-analog converter (DAC). Control logic changes the input to the DAC one bit at a time, starting with the MSB, until the DAC output matches the selected analog input. The conversion is monotonic and has no missing codes. At the end of 32 internal clock cycles, the conversion complete (CC) flag becomes set, and the digital conversion is readable in the ADC data register (ADDR).

To:

Each conversion takes 32 cycles. In the first 12 cycles the ADC samples the voltage on the selected input pin by charging an internal capacitor. In the next 20 cycles, a comparator successively compares the input voltage to the output of a precision internal digital-to-analog converter (DAC). Control logic changes the input to the DAC one bit at a time, starting with the MSB, until the DAC output matches the selected analog input. The conversion is monotonic and has no missing codes. At the end of the conversion, the conversion complete flag (CC) becomes set, and the CPU takes 2 cycles to move the result to the ADC data register (ADDR).

15. Page 10-4. Add the following material to the end of the ADRC bit description:

    When the internal RC oscillator is being used as the ADC clock, two limitations apply:

    - Because of the frequency tolerance of the RC oscillator and its asynchronism with the internal clock, the conversion complete flag must be used to determine when a conversion sequence is complete.
    - The RC oscillator drives the conversion process at the nominal frequency of 1.5 MHz, but the slower internal clock transfers conversion results to the A/D data register.

16. Page 11-2, add the following note after the EPROM/OTPROM programming procedure:

    NOTE

    When programming the MOR, set the MPGM bit in step 4 instead of the EPGM bit. (See **11.3 Mask Option Register (MOR)**.)

17. Page 11-6, **Figure 11-3. Mask Option Register (MOR)**, change bit 6 and bit 7 as follows:

From:

MOR — Mask Option Register **$1F00**

	Bit 7	6	5	4	3	2	1	Bit 0
	1	1	SWAIT	SPR1	SPR0	LSBF	LEVEL	COPE
RESET:	UNAFFECTED BY RESET							
ERASED:	0	0	0	0	0	0	0	0

Figure 11-3. Mask Option Register (MOR)

Bits 7 and 6 — Unused

Program bits 7 and 6 to logic zero.

To:

MOR — Mask Option Register **$1F00**

	Bit 7	6	5	4	3	2	1	Bit 0
			SWAIT	SPR1	SPR0	LSBF	LEVEL	COPE
RESET:	UNAFFECTED BY RESET							
ERASED:			0	0	0	0	0	0

Figure 11-3. Mask Option Register (MOR)

Bits 7 and 6 — Unused. Bits 7 and 6 have no effect on MCU operation.

NOTE

Bit seven always reads as logic zero. Bit 6 reads zero or one, depending on how it is programmed.

18. Page 11-8, add the following procedure after **Table 11-2. COP Watchdog Recommendations**:

    Take the following steps to program the MOR:

    1. Apply V_{PP} to the $\overline{IRQ}/V_{PP}$ pin.
    2. Set the ELAT bit.
    3. Write to $1F00.
    4. Set MPGM for a time, t_{EPGM}, to apply the programming voltage.
    5. Clear the ELAT bit.

19. Page 12-13, section **12.3 Instruction Set Summary**, correct the first sentence of the paragraph as follows:

    From:

    Table 12-12 shows all MC68HC705P9 instructions in all possible addressing modes.

    To:

    Table 12-12 shows all MC68HC705P6 instructions in all possible addressing modes.

20. Page 13-7, **Table 13-5. A/D Converter Characteristics** — Change the **Max** column in the second row of Table 13-5 as follows

    From:

Table 13-5. A/D Converter Characteristics

Characteristic	Min	Max	Unit
Absolute Accuracy ($4.0 > V_{RH} > V_{DD}$) (NOTE 2)	—	± 1-1/2	LSB

    To:

Table 13-5. A/D Converter Characteristics

Characteristic	Min	Max	Unit
Absolute Accuracy ($4.0 > V_{RH} > V_{DD}$) (NOTE 2)	—	± 1.5	LSB

21. Page 13-9, **Figure 13-4. TCAP Timing** — Change the t_{TLTL} parameter to t_{ILIL} as follows:

From:

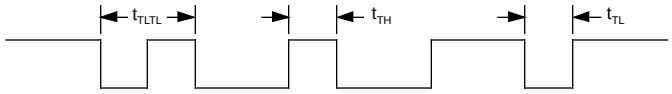


Figure 13-4. TCAP Timing

To:

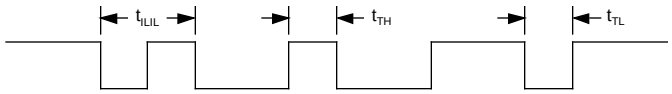


Figure 13-4. TCAP Timing

22. Page 13-12, **Table 13-8. SIOP Timing (V_{DD} = 5.0 Vdc)** — Change the first row as follows:

From:

Table 13-8. SIOP Timing (V_{DD} = 5.0 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	0.25 dc	0.25 525	f_{OP} kHz

To:

Table 13-8. SIOP Timing (V_{DD} = 5.0 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	f_{OSC}/64 dc	f_{OSC}/8 525	MHz kHz

Change NOTE 2 at the bottom of the table as follows:

From:

2. $f_{OP} = f_{OSC} \div 2$ = 2.1 MHz maximum; $t_{CYC} = 1 \div f_{OP}$

To:

2. f_{OSC} = crystal frequency; $f_{OP} = f_{OSC} \div 2$; $t_{CYC} = 1 \div f_{OP}$ (See Table 13-6. Control Timing (V_{DD} = 5.0 Vdc).)

Delete NOTE 3 at the bottom of the table.

23. Page 13-13, **Table 13-9. SIOP Timing (V_{DD} = 3.3 Vdc)** — Change the first row as follows:

From:

Table 13-9. SIOP Timing (V_{DD} = 3.3 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	0.25 dc	0.25 250	f_{OP} kHz

To:

Table 13-9. SIOP Timing (V_{DD} = 3.3 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	f_{OSC}/64 dc	f_{OSC}/8 250	MHz kHz

Change NOTE 2 at the bottom of the table as follows:

From:

2. f_{OP} = 1.0 MHz maximum

To:

2. f_{OSC} = crystal frequency; $f_{OP} = f_{OSC} \div 2$; $t_{CYC} = 1 \div f_{OP}$ (See Table 13-7. Control Timing (V_{DD} = 3.3 Vdc).)

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