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Rev. 1.0

Motorola Semiconductor Technical Data

MC68HC05L5

Technical Summary
8-Bit Microcontroller Unit

Table of Contents

Introduction

The MC68HC05L5 is a member of Motorola's high-density, complementary metal-oxide semiconductor (HCMOS) M68HC05 Family of 8-bit microcontrollers (MCUs). The M68HC05 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the popular M68HC05 central processor unit (CPU), and the family includes a selection of subsystems, memory sizes and types, and package types.

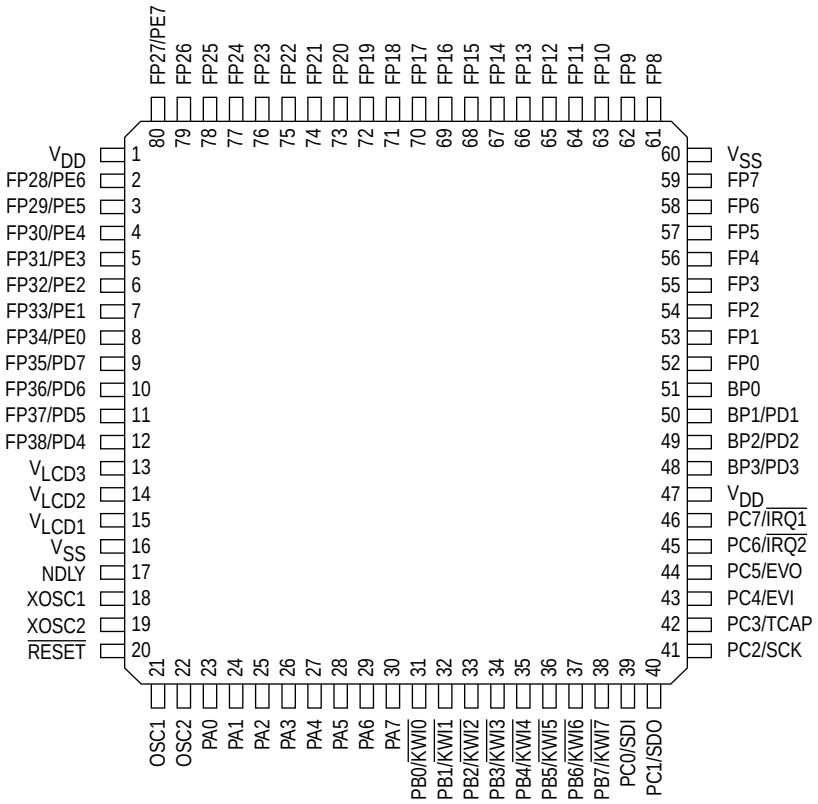
Features

- Popular M68HC05 CPU
- Memory-Mapped Input/Output (I/O) Registers
- 8208 Bytes of User ROM
- 256 Bytes of User Static RAM (SRAM)
- General-Purpose Data Pins: 14 Bidirectional Pins, 10 Input/Output-Only Pins, and 15 Output-Only Pins
- Full-Duplex Serial Peripheral Interface (SPI)
- Liquid Crystal Display (LCD) Driver with Four Backplane Outputs and 39 Frontplane Outputs
- Fully Static Operation, No Minimum Clock Speed
- Two On-Chip Oscillators with Crystal/Ceramic Resonator Connections
- 16-Bit Capture/Compare Timer
- 8-Bit Event Counter
- Key Wakeup Interrupt Circuit with Eight Inputs
- Two External Interrupt Input Pins
- Real-Time Interrupt Circuit
- Self-Check Mode

- Power-Saving Stop and Wait Modes
- Single 2.2–5.5-Volt Power Requirement
- 8 x 8 Unsigned Multiply Instruction
- Programmable Ports A, B, and C Pullup Resistors
- Programmable Ports A, C, D, and E Open-Drain Outputs
- Programmable Edge-Sensitive or Edge- and Level-Sensitive Interrupt Trigger
- Programmable COP Timer
- $\overline{\text{RESET}}$ Pin Pullup Resistor (Mask Option)
- OSC1 Pin/OSC2 Pin Feedback Resistor (Mask Option)
- XOSC1 Pin/XOSC2 Pin Feedback and Damping Resistors (Mask Option)
- 80-Pin Quad Flat Pack (QFP)

Pin Assignments

Figure 1 shows the pinout of the 80-pin quad flat pack (QFP).



NOTE: Pin 17 is used for factory testing and should be connected to V_{DD} during normal use.

Figure 1. Pin Assignments

Order Numbers

Use the following number when ordering this package type.

Package Type	Order Number
80-Pin QFP	MC68HC05L5FU

MCU Structure

Figure 2 shows the organization of the MC68HC05L5.

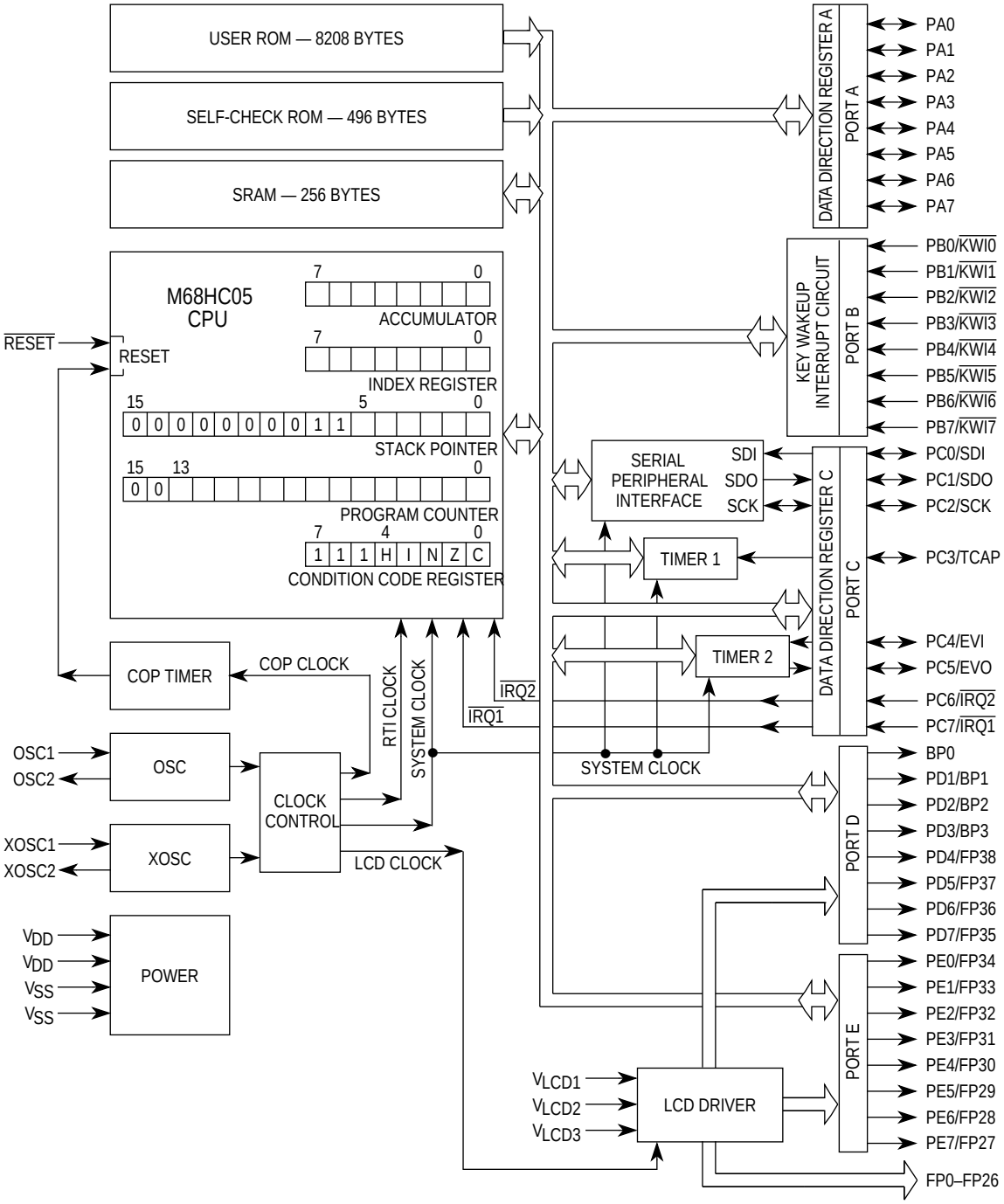


Figure 2. MCU Structure

Central Processor Unit Registers

As shown in **Figure 3**, five CPU registers are available to the programmer.

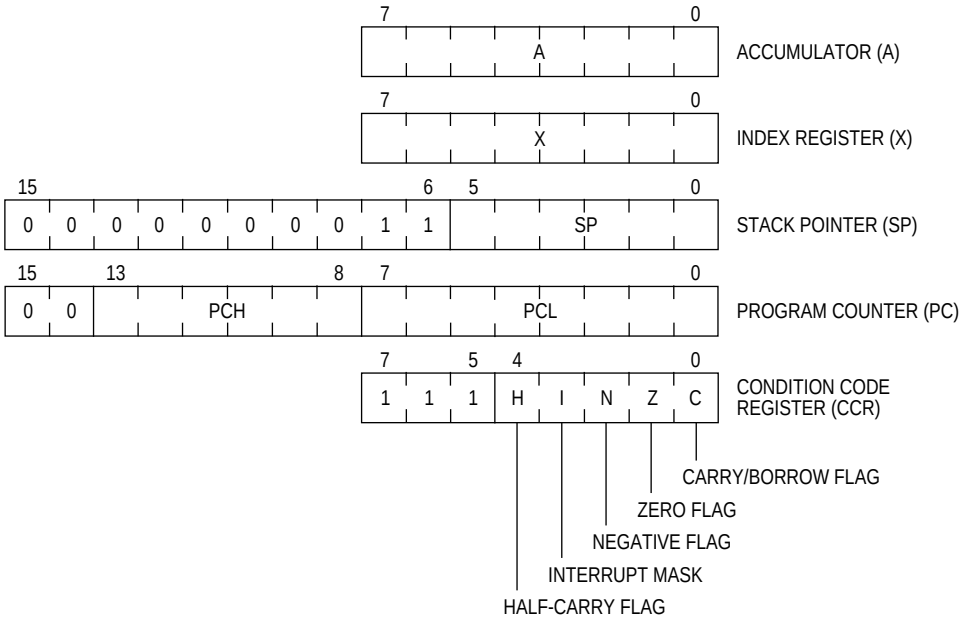


Figure 3. CPU Registers

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and results of arithmetic and nonarithmetic operations.

The index register contains a value that indicates an operand address in the indexed addressing modes. The index register can aso be used as an auxiliary accumulator for temporary storage.

The stack pointer contains the address of the next free location on the stack. The stack pointer decrements as data is pushed onto the stack and increments as data is pulled from the stack.

The program counter contains the address of the next byte for the CPU to fetch.

The condition code register has four status flags that indicate the results of the instruction just executed. A fifth bit is the interrupt mask.

Memory Map

The MC68HC05L5 can address 16 Kbytes of memory space. **Figure 4** and **Figure 5** show the organization of the on-chip memory and the function of the I/O registers.

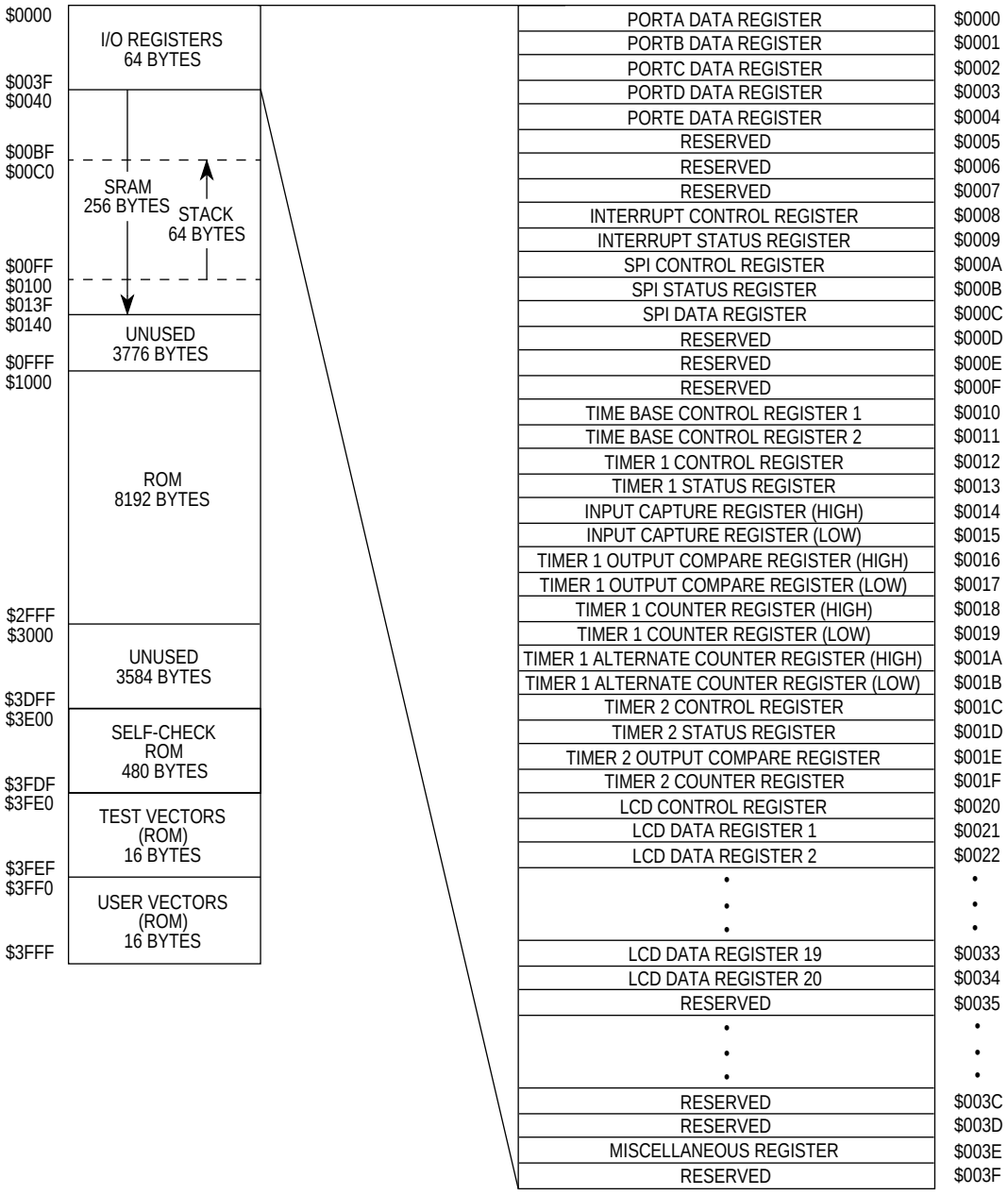


Figure 4. Memory Map (Sheet 1 of 2)

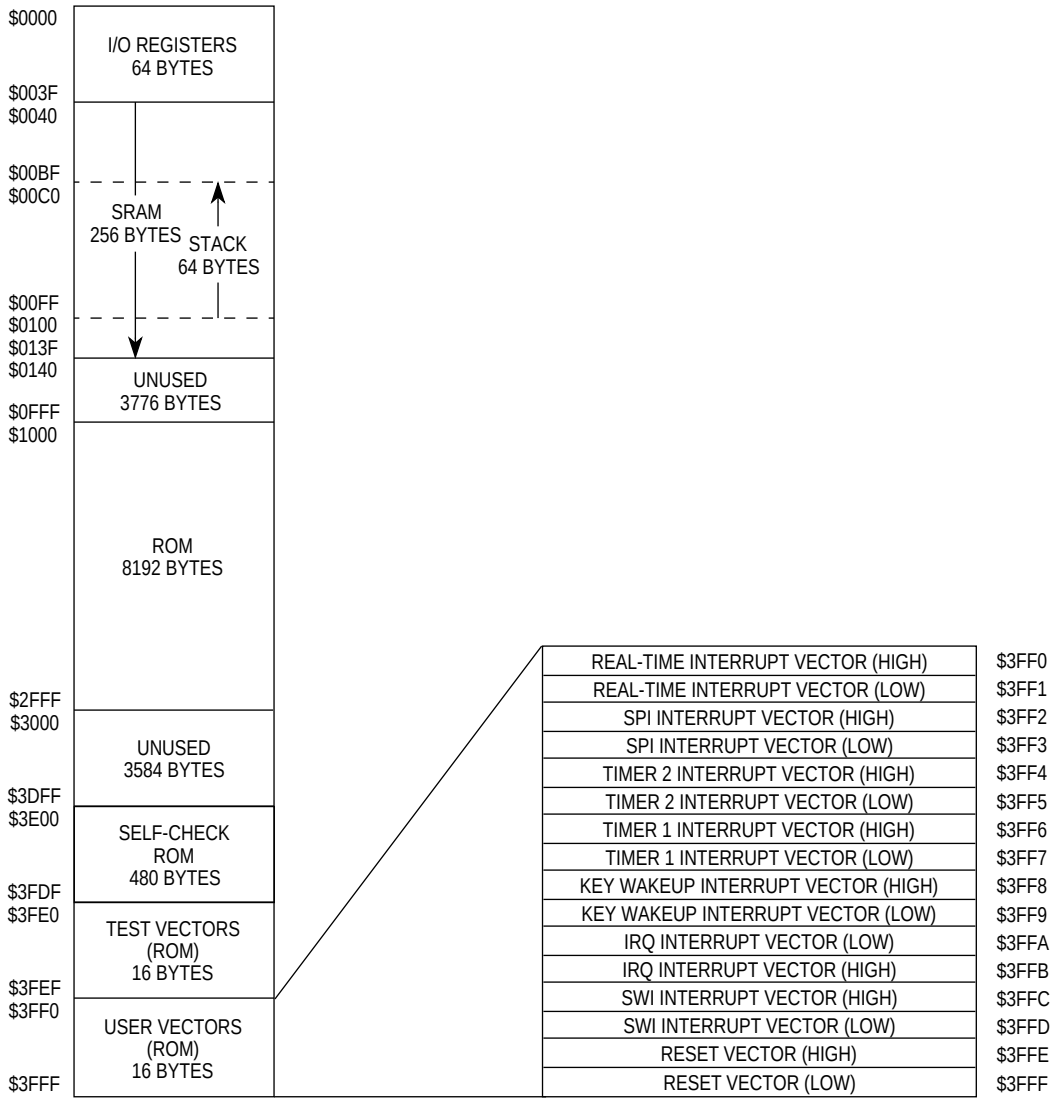


Figure 4. Memory Map (Sheet 2 of 2)

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
$0001	Port B Data Register (PORTB)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
$0002	Port C Data Register (PORTC)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
$0003	Port D Data Register (Port D)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	1
$0004	Port E Data Register (Port E)	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
$0005	Reserved	R	R	R	R	R	R	R	R
$0006	Reserved	R	R	R	R	R	R	R	R
$0007	Reserved	R	R	R	R	R	R	R	R
$0008	Interrupt Control Register (INTCR)	IRQ1E	IRQ2E	0	KWIE	IRQ1S	IRQ2S	0	0
$0009	Interrupt Status Register (INTSR)	IRQ1F	IRQ2F	0	KWIF	RIRQ1	RIRQ2	0	RKWIF
$000A	Serial Peripheral Interface Control Register (SPCR)	SPIE	SPE	DORD	MSTR	0	0	0	SPR
$000B	Serial Peripheral Interface Status Register (SPSR)	SPIF	DCOL	0	0	0	0	0	0
$000C	Serial Peripheral Interface Data Register (SPDR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$000D	Reserved	R	R	R	R	R	R	R	R
$000E	Reserved	R	R	R	R	R	R	R	R
$000F	Reserved	R	R	R	R	R	R	R	R
$0010	Time Base Control Register 1 (TBCR1)	TBCLK	0	LCLK	0	0	0	T2R1	T2R0
$0011	Time Base Control Register 2 (TBCR2)	RTIF	RTIE	RTR1	RTR0	RRTIF	0	COPE	COPC
$0012	Timer 1 Control Register (T1CR)	ICIF	T1OCIE	TOIE	0	0	0	IEDG	0
$0013	Timer 1 Status Register (T1SR)	ICF	T1OCIF	TOF	0	0	0	0	0
$0014	Input Capture Register (ICR) High	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Figure 5. I/O Registers (Sheet 1 of 3)

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$0015	Input Capture Register (ICR) Low	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0016	Timer 1 Output Compare Register (T1OCR) High	Bit 15	Bit 13	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
$0017	Timer 1 Output Compare Register (T1OCR) Low	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0018	Timer 1 Counter Register (T1CNTR) High	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
$0019	Timer 1 Counter Register (T1CNTR) Low	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001A	Timer 1 Alternate Counter Register (T1ALTCNTR) High	Bit 15	Bit 13	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
$001B	Timer 1 Alternate Counter Register (T1ALTCNTR) Low	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001C	Timer 2 Control Register (T2CR)	T2IE	T2OCIE	0	T2CLK	T2IM	T2IL	T2OE	T2OS
$001D	Timer 2 Status Register (T2SR)	T2IF	T2OCIF	0	0	RT2IF	RT2OCIF	0	0
$001E	Timer 2 Output Compare Register (T2OCR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$001F	Timer 2 Counter Register (T2CNTR)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0020	LCD Control Register (LCDCR)	LCDE	DUTY1	DUTY0	0	PEH	PEL	PDH	0
$0021	LCD Data Register (LCDDR1)	F1B3	F1B2	F1B1	F1B0	F0B3	F0B2	F0B1	F0B0
$0022	LCD Data Register 2 (LCDDR2)	F3B3	F3B2	F3B1	F3B0	F2B3	F2B2	F2B1	F2B0
$0023	LCD Data Register 3 (LCDDR3)	F5B3	F5B2	F5B1	F5B0	F4B3	F4B2	F4B1	F4B0
$0024	LCD Data Register 4 (LCDDR4)	F7B3	F7B2	F7B1	F7B0	F6B3	F6B2	F6B1	F6B0
$0025	LCD Data Register 5 (LCDDR5)	F9B3	F9B2	F9B1	F9B0	F8B3	F8B2	F8B1	F8B0
$0026	LCD Data Register 6 (LCDDR6)	F11B3	F11B2	F11B1	F11B0	F10B3	F10B2	F10B1	F10B0
$0027	LCD Data Register 7 (LCDDR7)	F13B3	F13B2	F13B1	F13B0	F12B3	F12B2	F12B1	F12B0

Figure 5. I/O Registers (Sheet 2 of 3)

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$0028	LCD Data Register 8 (LCDDR8)	F15B3	F15B2	F15B1	F15B0	F14B3	F14B2	F14B1	F14B0
$0029	LCD Data Register 9 (LCDDR9)	F17B3	F17B2	F17B1	F17B0	F16B3	F16B2	F16B1	F16B0
$002A	LCD Data Register 10 (LCDDR10)	F19B3	F19B2	F19B1	F19B0	F18B3	F18B2	F18B1	F18B0
$002B	LCD Data Register 11 (LCDDR11)	F21B3	F21B2	F21B1	F21B0	F20B3	F20B2	F20B1	F20B0
$002C	LCD Data Register 12 (LCDDR12)	F23B3	F23B2	F23B1	F23B0	F22B3	F22B2	F22B1	F22B0
$002D	LCD Data Register 13 (LCDDR13)	F25B3	F25B2	F25B1	F25B0	F24B3	F24B2	F24B1	F24B0
$002E	LCD Data Register 14 (LCDDR14)	F27B3	F27B2	F27B1	F27B0	F26B3	F26B2	F26B1	F26B0
$002F	LCD Data Register 15 (LCDDR15)	F29B3	F29B2	F29B1	F29B0	F28B3	F28B2	F28B1	F28B0
$0030	LCD Data Register 16 (LCDDR16)	F31B3	F31B2	F31B1	F31B0	F30B3	F30B2	F30B1	F30B0
$0031	LCD Data Register 17 (LCDDR17)	F33B3	F33B2	F33B1	F33B0	F32B3	F32B2	F32B1	F32B0
$0032	LCD Data Register 18 (LCDDR18)	F35B3	F35B2	F35B1	F35B0	F34B3	F34B2	F34B1	F34B0
$0033	LCD Data Register 19 (LCDDR19)	F37B3	F37B2	F37B1	F37B0	F36B3	F36B2	F36B1	F36B0
$0034	LCD Data Register 20 (LCDDR20)	R	R	R	R	F38B3	F38B2	F38B1	F38B0
$0035	Reserved	R	R	R	R	R	R	R	R
↓	↓					↓			
$003C	Reserved	R	R	R	R	R	R	R	R
$003D	Reserved	R	R	R	R	R	R	R	R
$003E	Miscellaneous Register (MR)	FTUP	STUP	0	0	SYS1	SYS0	FOSCE	OPTM
$003F	Reserved	R	R	R	R	R	R	R	R

R = Reserved

Figure 5. I/O Registers (Sheet 3 of 3)

Option Memory Map

The option memory map contains control registers to implement functions that otherwise would be mask options. The two data direction registers, DDRA and DDRC, are also in the option memory map. When the OPTM bit in the miscellaneous register (MR) is set, the option memory map appears. The option memory map replaces addresses $0000–$000F in the memory map and controls the following options:

In the resistor control register 1 (RCR1) at $0008:

1. Port B pullup resistors (RAH and RAL bits)
2. Port A pullup resistors (RBH and RBL bits)

In the resistor control register 2 (RCR2) at $0009:

3. Port C pullup resistors (RC7–RC0 bits)

In the wired-OR mode register 1 (WOM1) at $000A:

4. Port D open-drain mode (DWOMH and DWOML bits)
5. Port E open-drain mode (EWOMH and EWOML bits)
6. Port A open-drain mode (AWOMH and AWOML bits)

In the wired-OR mode register 2 (WOM2) at $000B:

7. Port C open-drain mode (CWOM5–CWOM0 bits)

In the key wakeup input enable register (KWIEN) at $000E:

8. Key wakeup input enable (KWIE7–KWIE0 bits)

The mask option status register (MOSR) at $000F shows the status of the following mask options:

1. $\overline{\text{RESET}}$ pin pullup resistor (RSTR bit)
2. OSC1/OSC2 feedback resistor (OSCR bit)
3. XOSC1/XOSC2 feedback resistor and damping resistor at XOSC2 (XOSCR bit)

Figure 6 and **Figure 7** show the organization of the option memory map and the function of the option map registers.

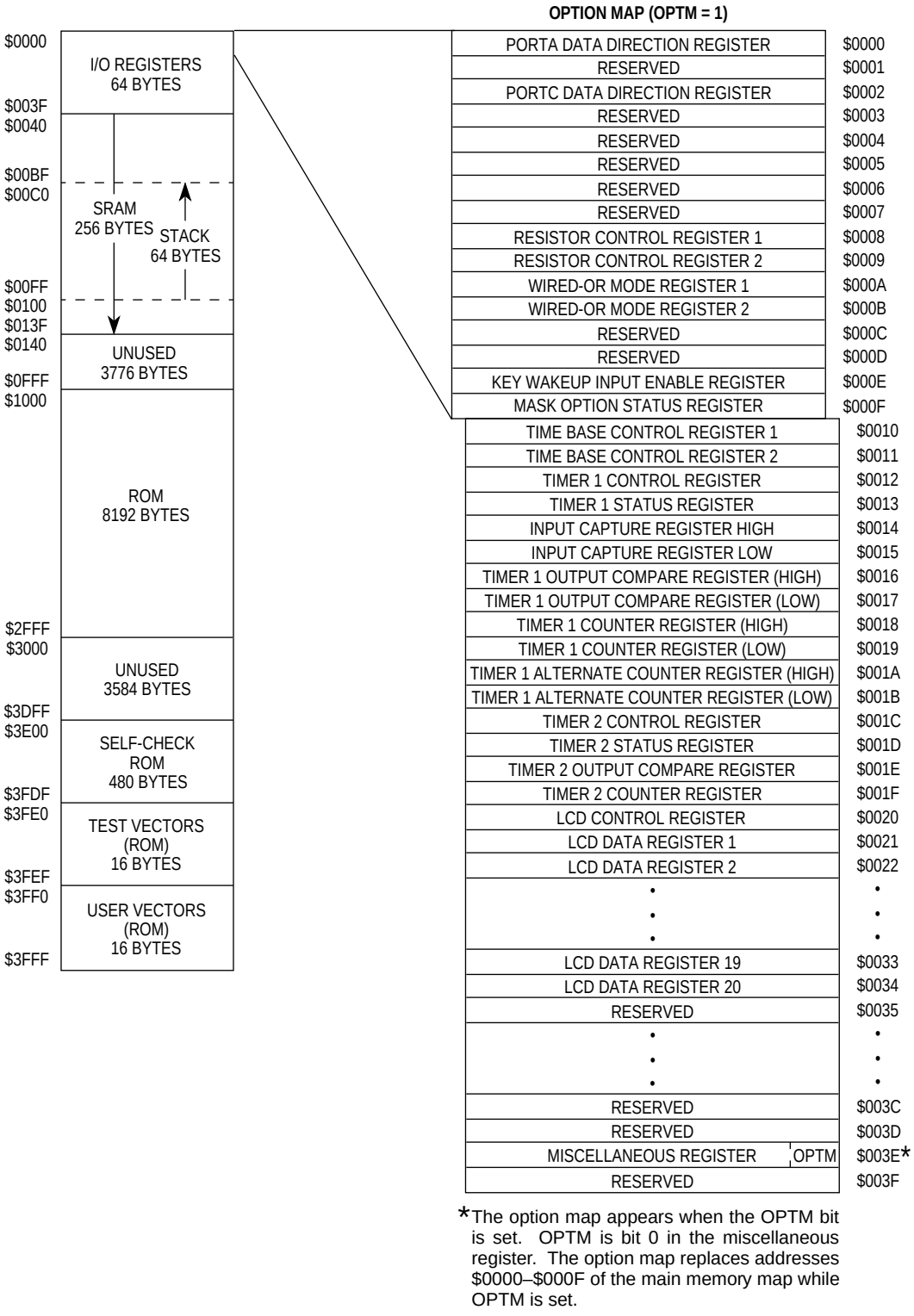


Figure 6. Option Memory Map

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Direction Register (DDRA)	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
$0001	Reserved	R	R	R	R	R	R	R	R
$0002	Port C Data Direction Register (DDRC)	0	0	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
$0003	Reserved	R	R	R	R	R	R	R	R
$0004	Reserved	R	R	R	R	R	R	R	R
$0005	Reserved	R	R	R	R	R	R	R	R
$0006	Reserved	R	R	R	R	R	R	R	R
$0007	Reserved	R	R	R	R	R	R	R	R
$0008	Resistor Control Register 1 (RCR1)	0	0	0	0	RBH	RBL	RAH	RAL
$0009	Resistor Control Register 2 (RCR2)	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
$000A	Wired-OR Mode Register 1 (WOM1)	DWOMH	DWOML	EWOMH	EWOML	0	0	AWOMH	AWOML
$000B	Wired-OR Mode Register 2 (WOM2)	0	0	CWOM5	CWOM4	CWOM3	CWOM2	CWOM1	CWOM0
$000C	Reserved	R	R	R	R	R	R	R	R
$000D	Reserved	R	R	R	R	R	R	R	R
$000E	Key Wakeup Input Enable Register (KWIEN)	KWIE7	KWIE6	KWIE5	KWIE4	KWIE3	KWIE2	KWIE1	KWIE0
$000F	Mask Option Status Register (MOSR)	RSTR	OSCR	XOSCR	0	0	0	0	0

R = Reserved

Figure 7. Option Map I/O Register

Port A Data Direction Register (DDRA)

Option Map Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

DDRA7–DDRA0 — Port A Data Direction Bits

These read/write bits determine whether the PA7–PA0 are inputs or outputs.

1 = Corresponding port pin configured as output
0 = Corresponding port pin configured as input

Port C Data Direction Register (DDRC)

Option Map Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
Reset:	0	0	0	0	0	0	0	0

DDRC5–DDRC0 — Port C Data Direction Bits

These read/write bits determine whether pins PC5–PC0 are inputs or outputs.

1 = Corresponding port pin configured as output
0 = Corresponding port pin configured as input

Resistor Control Register 1 (RCR1)

Option Map Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	0	0	RBH	RBL	RAH	RAL
Reset:	0	0	0	0	0	0	0	0

RBH — Resistors B High

This read/write bit connects internal pull-up resistors to the upper four port B pins.

1 = Pullup resistors connected to pins PB7–PB4
0 = No pullup resistors connected to pins PB7–PB4

RBL — Resistors B Low

This read/write bit connects internal pullup resistors to the lower four port B pins.

0 = Pullup resistors connected to pins PB3–PB0
0 = No pullup resistors connected to pins PB3–PB0

RAH — Resistors A High

This read/write bit connects internal pullup resistors to the upper four port A pins.

1 = Pullup resistors connected to pins PA7–PA4
0 = No pullup resistors connected to pins PA7–PA4

RAL — Resistors A Low

This read/write bit connects internal pullup resistors to the lower four port A pins.

1 = Pullup resistors connected to pins PA3–PA0
0 = No pullup resistors connected to pins PA3–PA0

Resistor Control Register 2 (RCR2)

Option Map Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
Reset:	0	0	0	0	0	0	0	0

RC7–RC0 — Resistors C

These read/write bits connect internal pullup resistors to the port C pins.

1 = Pullup resistor connected to the corresponding pin
0 = No pullup resistor connected to the corresponding pin

Wired-OR Mode Register 1 (WOM1)

Option Map Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DWOMH	DWOML	EWOMH	EWOML	0	0	AWOMH	AWOML
Reset:	0	0	0	0	0	0	0	0

DWOMH — Port D Wired-OR Mode (High Bits)

This read/write bit configures the upper four port D pins as open-drain outputs. The PDH bit in the LCD control register must be set, configuring PD7–PD4 as general-purpose outputs.

1 = PD7–PD4 configured as open-drain outputs
0 = PD7–PD4 configured as normal outputs

DWOML — Port D Wired-OR Mode (Low Bits)

This read/write bit configures port D pins PD3–PD1 as open-drain outputs. The DUTY1 and DUTY0 bits in the LCD control register must be programmed to configure the PDx pin as a general-purpose output.

1 = PD3–PD1 configured as open-drain outputs
0 = PD3–PD1 configured as normal outputs

EWOMH — Port E Wired-OR Mode (High Bits)

This read/write bit configures the upper four port E pins as open-drain outputs. The PEH bit in the LCD control register must be set, configuring PE7–PE4 as general-purpose outputs.

1 = PE7–PE4 configured as open-drain outputs
0 = PE7–PE4 configured as normal outputs

EWOML — Port E Wired-OR Mode (Low Bits)

This read/write bit configures the lower four port E pins as open-drain outputs. The PEL bit in the LCD control register must be set, configuring PE3–PE0 as general-purpose outputs.

1 = PE3–PE0 configured as open-drain outputs
0 = PE3–PE0 not configured as open-drain outputs

AWOMH — Port A Wired-OR Mode (High Bits)

This read/write bit configures the upper four port A pins as open-drain outputs. The DDRAx bit in port A data direction register must be set, configuring the PAx pin as an output.

1 = PA7–PA4 configured as open-drain outputs
0 = PA7–PA4 not configured as open-drain outputs

AWOML — Port A Wired-Or Mode (Low Bits)

This read/write bit configures the lower four port A pins as open-drain outputs. The DDRAx bit in the port A data direction register must be set, configuring the PAx pin as an output.

1 = PA3–PA0 configured as open-drain outputs
0 = PA3–PA0 configured as normal outputs

Wired-OR Mode Register 2 (WOM2)

Option Map Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	CWOM5	CWOM4	CWOM3	CWOM2	CWOM1	CWOM0
Reset:	0	0	0	0	0	0	0	0

CWOM5–CWOM0 — Port C Wired-OR Mode

These read/write bits configure the port C pins PC5–PC0 as open-drain outputs. The DDRCx bit in the port C data direction register must be set, configuring PCx pin as an output.

1 = PCx configured as open-drain output
0 = PCx configured as normal output

Key Wakeup Input Enable Register (KWIEN)

Option Map Address: $000E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	KWIE7	KWIE6	KWIE5	KWIE4	KWIE3	KWIE2	KWIE1	KWIE0
Reset:	0	0	0	0	0	0	0	0

KWIE7–KWIE0 — Key Wakeup Enable

These read/write bits enable the $\overline{\text{KWI7}}$–$\overline{\text{KWI0}}$ pins to function as key wakeup interrupt inputs.

1 = $\overline{\text{KWIx}}$ input enabled
0 = $\overline{\text{KWIx}}$ input disabled

Mask Option Status Register (MOSR)

Option Map Address: $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RSTR	OSCR	XOSCR	0	0	0	0	0
Reset:	U	U	U	0	0	0	0	0

U = Unaffected

RSTR — Reset Resistor

This flag is set when the mask-optional internal pullup resistor is connected to the $\overline{\text{RESET}}$ pin.

1 = Pullup resistor connected to $\overline{\text{RESET}}$ pin
0 = No pullup resistor on $\overline{\text{RESET}}$ pin

OSCR — OSC Resistor

This flag is set when the mask-optional internal feedback resistor, R_f, is connected between OSC1 and OSC2.

1 = Feedback resistor connected
0 = No feedback resistor connected

XOSCR — XOSC Resistor

This flag is set when the mask-optional internal feedback resistor, R_f, is connected between XOSC1 and XOSC2, and the mask-optional damping resistor, R_d, is connected to XOSC2. (See **Figure 8**.)

1 = Feedback and damping resistors connected
0 = No feedback or damping resistors connected

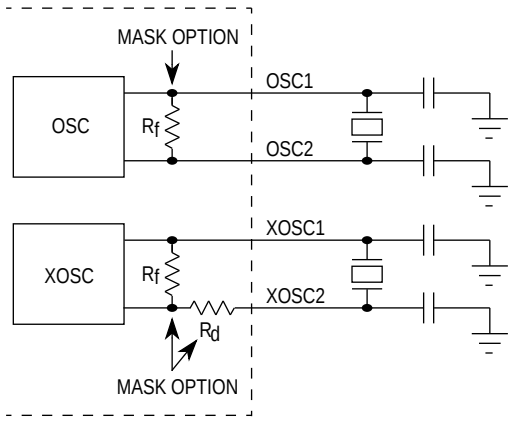
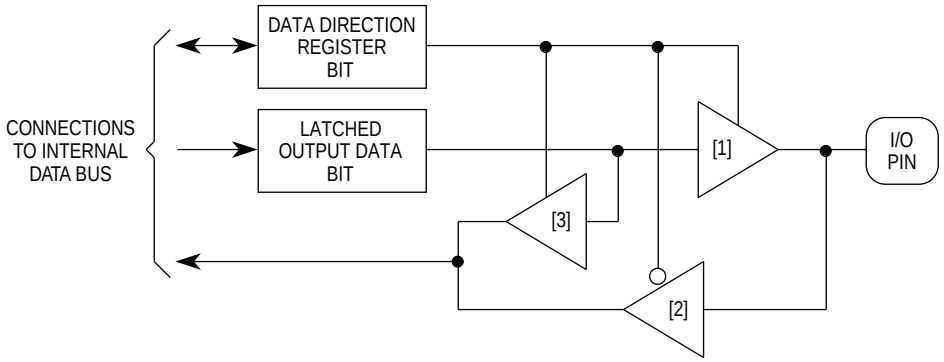


Figure 8. OSC/XOSC Resistor Mask Options

I/O Ports

The MC68HC05L5 has 14 bidirectional I/O pins, 10 input-only pins, and 15 output-only pins. The contents of the data direction registers (DDRs) determine whether each bidirectional I/O pin is an input or an output. (See **Figure 9**.)

When an I/O pin is programmed as an output, reading the associated port bit actually reads the value of the output data latch and not the logic level on the pin itself. When a pin is programmed as in input, reading the port bit reads the logic level on the I/O pin. The output data latch can always be written, regardless of the state of its DDR bit. (See **Table 1**.)



[1] This output buffer enables the latched data to drive the pin when DDR bit is 1 (output mode).
[2] This input buffer is enabled when DDR bit is 0 (input mode).
[3] This input buffer is enabled when DDR bit is 1 (output mode).

Figure 9. Parallel I/O Circuit

Table 1. I/O Pin Functions

R/$\overline{W}$*	DDR	I/O Pin Functions
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch, which drives the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in output mode. The output data latch is read.

* R/$\overline{W}$ is an internal signal.

The following subsections detail the four I/O port data registers.

Port A Data Register (PORTA)

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset:	Unaffected by Reset							

Port A is an 8-bit bidirectional port. The DDRA7–DDRA0 bits in the port A data direction register in the option map determine the data direction of pins PA7–PA0. At power-up, all eight pins are configured as inputs.

On-chip port A pullup resistors are selectable in resistor control register 1 in the option memory map.

Port A outputs are configurable as open-drain outputs in wired-OR mode register 1 in the option memory map.

Port B Data Register (PORTB)

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Reset:	Unaffected by Reset							
Alternate Function:	KWI7	KWI6	KWI5	KWI4	KWI3	KWI2	KWI1	KWI0

Port B is an 8-bit input-only port that shares its pins with the key wakeup interrupt system.

On-chip port B pullup resistors are selectable in resistor control register 1 in the option memory map.

Port C Data Register (PORTC)

Address: $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Reset:	Unaffected by Reset							
Alternate Function:	IRQ1	IRQ2	EVO	EVI	TCAP	SCK	SDO	SDI

Port C is an 8-bit port that shares its pins with several subsystems. PC7 and PC6 are input-only pins that function as external interrupt inputs when external interrupts are enabled by the IRQ1E and IRQ2E bits in the interrupt control register.

PC5 is a bidirectional pin that functions as the timer 2 output (EVO) when the EVO is enabled by the T2OE bit in the timer 2 control register.

PC4 and PC3 are bidirectional pins that can function as the timer 2 input (EVI) and the timer 1 input (TCAP).

PC2–PC0 are bidirectional pins that function as serial peripheral interface (SPI) pins when the SPI is enabled by the SPE bit in the SPI control register.

On-chip port C pullup resistors are selectable in resistor control register 2 in the option memory map.

Port C outputs are configurable as open-drain outputs in wired-OR mode register 2 in the option memory map.

Port D Data Register (PORTD)

Address: $0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Reset:	1	1	1	1	1	1	1	1
Alternate Function:	FP35	FP36	FP37	FP38	BP3	BP2	BP1	

Port D is a 7-bit general-purpose output-only port that shares its pins with the LCD drivers.

Port D outputs are configurable as open-drain outputs in wired-OR mode register 1 in the option memory map.

Port E Data Register (PORTE)

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Reset:	1	1	1	1	1	1	1	1
Alternate Function:	FP27	FP28	FP29	FP30	BP31	BP32	BP33	FP34

Port E is an 8-bit general-purpose output port that shares its pins with the LCD frontplane drivers.

Port E outputs are configurable as open-drain outputs in wired-OR mode register 1 in the option memory map.

Resets and Interrupts

There are three reset conditions that force the CPU to a user-defined starting address. There are also seven ways to interrupt normal processing to service an external or subsystem event.

Resets

A reset occurs under the following conditions:

- Power-on reset (POR) — A POR is generated when a positive transition occurs on the V_{DD} pin.
- External reset — A reset is generated when a logical zero is applied to the $\overline{\text{RESET}}$ pin.
- Computer operating properly (COP) timer reset — The COP timer resets the CPU if not cleared by a program sequence within a specific period of time. The COP timer system is used to detect software errors.

The following internal actions occur on reset:

- All implemented data direction bits are cleared, making all I/O pins inputs.
- The stack pointer is loaded with $FF.
- The global interrupt mask (I bit) in the condition code register is set, inhibiting interrupts.
- The timer clock divider stages are reset. Timer 1 is loaded with $FFFC.
- Timer 2 is loaded with $01.
- All local interrupt enable bits are cleared to disable interrupts.
- The STOP latch is cleared to enable MCU clocks.
- The WAIT latch is cleared to wake the CPU from wait mode.
- The program counter is loaded with the reset vector.
- The SYS1 and SYS0 bits in the miscellaneous register are preset to 0 and 1, selecting OSC Ö64 as the system clock.

Interrupts

The CPU can be interrupted in the following ways:

- Software interrupt (SWI) — The SWI instruction causes a nonmaskable interrupt to be executed.
- External interrupt — An interrupt signal on either the $\overline{\text{IRQ1}}$ pin or the $\overline{\text{IRQ2}}$ pin causes an external interrupt if the corresponding interrupt enable bit (IRQ1E or IRQ2E) is set. Both external interrupts use the same interrupt vector. The interrupt signal can be either of the following conditions:
  - A falling edge
  - Either a falling edge or a low level

  The states of the IRQ1S and IRQ2S bits determine which condition on the $\overline{\text{IRQ}}$ pins the CPU recognizes as an interrupt signal. The IRQ1E and the IRQ2E bits enable external interrupts.
- Key wakeup interrupt — The key wakeup enable register ($000E in the option memory map) enables the key wakeup pins, $\overline{\text{KWI7}}$–$\overline{\text{KWI0}}$. See **Figure 7**. A falling edge on one of the enabled key wakeup pins sets the KWIF flag. If the KWIE bit is also set, a key wakeup interrupt is requested.
- Timer 1 interrupt — The CPU recognizes a timer 1 interrupt if one of the three timer 1 interrupt flags (IC1F, OCIF, or TOF) is set while its corresponding timer 1 interrupt enable bit (IC1IE, OC1IE, or TOIE) is set.
- Timer 2 interrupt — The CPU recognizes a timer 2 interrupt if one of the two timer 2 interrupt flags (T2IF or T2OCIF) is set while its corresponding timer 2 interrupt enable bit (T2IE or T2OCIE) is set.
- Serial peripheral interface (SPI) interrupt — After each one-byte data transfer, the SPI sets the SPIF flag. If the SPI interrupt enable bit (SPIE) is also set, an interrupt is requested.
- Real-time interrupt — The real-time interrupt circuit sets the RTIF flag at the end of the selected real-time interrupt period. If the RTIE bit is also set, a real-time interrupt is requested.

The following actions occur as the result of an interrupt:

- CPU registers are stored in the stack in the order PCL, PCH, X, A, CCR.
- The interrupt mask (I bit) in the condition code register is set to prevent additional interrupts.
- The program counter is loaded with the appropriate interrupt vector.
- The RTI (return from interrupt) instruction causes the CPU registers to be recovered from the stack in the order CCR, A, X, PCH, PCL. Normal processing resumes.

Table 2. Reset/Interrupt Vector Assignments

Type	Source	Local Mask	Global Mask	Priority (1 = High)	Vector Address
Reset	COP Timer Reset Pin POR	COPE None None	None None None	1 1 1	$3FFE–$3FFF $3FFE–$3FFF $3FFE–$3FFF
SWI	None	None	None	*	$3FFC–$3FFD
External	IRQ1 Pin IRQ2 Pin	IRQ1E IRQ2E	I I	2 2	$3FFA–$3FFB $3FFA–$3FFB
KWI	KWIF	KWIE	I	3	$3FF8–$3FF9
Timer 1	ICF T1OCIF TOF	ICIE T1OCIE TOIE	I I I	4 4 4	$3FF6–$3FF7 $3FF6–$3FF7 $3FF6–$3FF7
Timer 2	T2IF T2OCIF	T2IE T2OCIE	I I	5 5	$3FF4–$3FF5 $3FF4–$3FF5
SPI	SPIF	SPIE	I	6	$3FF2–$3FF3
RTI	RTIF	RTIE	I	7	$3FF0–$3FF1

* Same level as an instruction

INTCR — Interrupt Control Register

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IRQ1E	IRQ2E	0	KWIE	IRQ1S	IRQ2S	0	0
Reset:	0	0	0	0	0	0	0	0

IRQ1E — IRQ1 Enable

This read/write bit enables IRQ1 interrupts.

1 = IRQ1 interrupts enabled
0 = IRQ1 interrupts disabled

IRQ2E — IRQ2 Enable

This read/write bit enables IRQ2 interrupts.

1 = IRQ2 interrupts enabled
0 = IRQ2 interrupts disabled

KWIE — Key Wakeup Interrupt Enable

This read/write bit enables key wakeup interrupts.

1 = Key wakeup interrupts enabled
0 = Key wakeup interrupts disabled

IRQ1S — IRQ1 Sensitivity

This read/write bit determines the $\overline{\text{IRQ1}}$ pin interrupt trigger sensitivity.

1 = Negative edge on $\overline{\text{IRQ1}}$ pin triggers interrupt request
0 = Negative edge or low level on $\overline{\text{IRQ1}}$ pin triggers interrupt request

IRQ2S — IRQ2 Sensitivity

This read/write bit determines the $\overline{\text{IRQ2}}$ pin interrupt trigger sensitivity.

1 = Negative edge on $\overline{\text{IRQ2}}$ pin triggers interrupt request
0 = Negative edge or low level on $\overline{\text{IRQ2}}$ pin triggers interrupt request

INTSR — Interrupt Status Register

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IRQ1F	IRQ2F	0	KWIF	RIRQ1	RIRQ2	0	RKWIF
Reset:	0	0	0	0	0	0	0	0

IRQ1F — IRQ1 Flag

This read-only bit is set when an interrupt signal occurs on the IRQ1 pin. Clear the IRQ1F flag by writing a one to the RIRQ1 bit.

IRQ2F — IRQ2 Flag

This read-only bit is set when an interrupt signal occurs on the IRQ2 pin. Clear the IRQ2F flag by writing a one to the RIRQ2 bit.

KWIF — Key Wakeup Interrupt Flag

This read-only bit is set when a key wakeup interrupt signal occurs on one of the KWI7–KWI0 pins. Clear the KWIF bit by writing a one to the RKWIF bit.

RIRQ1 — Reset IRQ1 Flag

Setting this write-only bit clears the IRQ1F bit. Writing a zero to RIRQ1 has no effect. RIRQ1 always reads as zero.

RIRQ2 — Reset IRQ2 Flag

Setting this write-only bit clears the IRQ2F bit. Writing a zero to RIRQ2 has no effect. RIRQ2 always reads as zero.

RKWIF — Reset Key Wakeup Interrupt Flag

Setting this write-only bit clears the KWIF bit. Writing a zero to RKWIF has no effect. RKWIF always reads as zero.

Clock Distribution and Control

Figure 10 shows how the oscillator inputs are prescaled and selected to provide the internal clock signals.

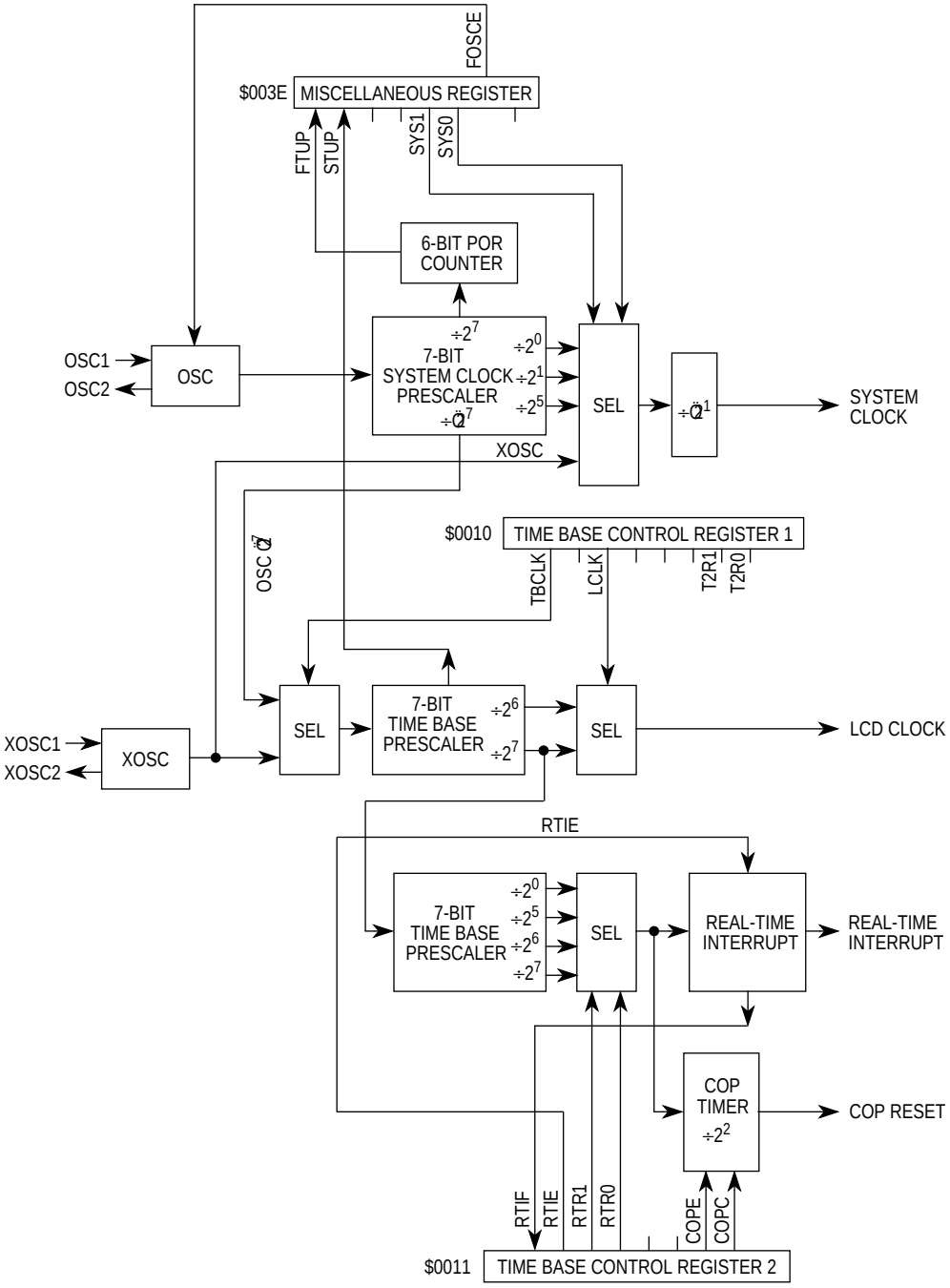


Figure 10. Clock Distribution

OSC and XOSC

OSC is the main oscillator. OSC divided by 2, 4, or 64 can be selected as the clock source for the system clock. OSC divided by 128 can be selected as the clock source for the time base. Clearing the FOSCE bit in the miscellaneous register turns off OSC and presets the 7-bit system clock prescaler and the 6-bit power-on reset (POR) counter to $0078. Setting FOSCE starts OSC again, and the POR counter overflow sets the FTUP bit after 8072 counts.

XOSC is the alternate oscillator. It runs as long as the MCU is powered up. XOSC can be selected as the clock source for the system clock and the time base.

System Clock

A 7-bit divider prescales the OSC clock to produce the system clock. The system clock drives the CPU, the serial peripheral interface subsystem, and the two timers. The SYS1 and SYS0 bits in the miscellaneous register select either OSC divided by 2, 4, or 64 or XOSC divided by 2 to drive the system clock. Reset automatically selects OSC divided by 64.

Miscellaneous Register (MR)

Address: $003E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	FTUP	STUP	0	0	SYS1	SYS0	FOSCE	OPTM
Reset:	U	U	0	0	1	0	1	0

U = Unaffected

FTUP — OSC Time Up

This read-only flag is cleared by power-on reset or by shutting down the OSC oscillator (clearing the FOSCE bit). If the FOSCE bit is set, the POR counter overflow sets the RTUP bit again after 8072 counts.

1 = OSC clock available for the system clock

0 = Power-on reset or OSC disabled (FOSCE = 0)

STUP — XOSC Time Up

This read-only flag is cleared at power-on and is set after 8072 counts of the time base prescaler. The STUP bit then stays set until power-down.

1 = XOSC clock available for the system clock
0 = XOSC not stabilized or no connection on XOSC1 and XOSC2 pins

SYS1–SYS0 — System Clock

These read/write bits select one of four system clock sources as shown in **Table 3**.

Table 3. System Clock Frequency Selection

SYS1: SYS0	Divide Ratio	System Clock Frequency		
		OSC = 4.0 MHz	OSC = 4.1943 MHz	XOSC = 32.768 kHz
00	OSC ÷ 2	2.0 MHz	2.0972 MHz	—
01	OSC ÷ 4	1.0 MHz	1.0486 MHz	—
10	OSC ÷ 64	62.5 kHz	65.536 kHz	—
11	XOSC ÷ 2	—	—	16.384 kHz

FOSCE — OSC Enable

This read/write bit turns on OSC. After 8072 clocks, an overflow from the POR counter sets the FTUP bit in the miscellaneous register. When OSC turns off, the FTUP bit is cleared, and the 7-bit OSC divider and the 6-bit POR counter are preset to $0078.

1 = OSC enabled
0 = OSC disabled

OPTM — Option Map

This read/write bit selects the option memory map.

1 = Option memory map selected
0 = Option memory map not selected

Time Base

Time base produces the LCD clock, real-time interrupt clock, and COP clock. OSC divided by 128 or XOSC can drive the time base. At power-on, the 14-bit time base prescaler is initialized to $0078. After 8072 counts, it sets the STUP bit in the miscellaneous register.

Time Base Control Register 1 (TBCR1)

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TBCLK	0	LCLK	0	0	0	T2R1	T2R0
Reset:	0	0	0	0	0	0	0	0

TBCLK — Time Base Clock

This read/write bit selects the clock source for the time base. After reset, a write to this bit is permitted only once.

1 = OSC divided by 128 selected
0 = XOSC selected

LCLK — LCD Clock

This read/write bit selects the clock source for the LCD driver.

1 = OSC divided by 16384 or XOSC divided by 128
0 = OSC divided by 8192 or XOSC divided by 64

Table 4 shows how TBCLK and LCLK control the LCD clock.

Table 4. LCD Clock Frequency Selection

TBCLK	LCLK	Divide Ratio	LCD Clock Frequency (Hz)		
			OSC = 4.0 MHz	OSC = 4.1943 MHz	XOSC = 32.768 kHz
1	0	OSC ÷ 2^{13}	488	512	—
1	1	OSC ÷ 2^{14}	244	256	—
0	0	XOSC ÷ 2^{6}	—	—	512
0	1	XOSC ÷ 2^{7}	—	—	256

T2R1–T2R0 — Timer 2 Rate Bits 1–0

These read/write bits control the timer prescaler, as shown in **Table 5**. They select the system clock divided by 1, 4, 32, or 256 to produce CLK2. CLK2 may be used to gate the EVI input to timer 2.

Table 5. Timer Prescaler Control

T2R1:T2R0	CLK2 Frequency
0 0	System Clock ÷ 1
0 1	System Clock ÷ 4
1 0	System Clock ÷ 32
1 1	System Clock ÷ 256

Time Base Control Register 2 (TBCR2)

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RTIF	RTIE	RTR1	RTR0	RRTIF	0	COPE	COPC
Reset:	0	0	1	1	0	0	0	0

RTIF — Real-Time Interrupt Flag

This read-only flag is set by every timeout of the real-time clock.

1 = RTI request
0 = No RTI request

RTIE — Real-Time Interrupt Enable

This read/write bit enables real-time interrupts.

1 = RTI interrupts enabled
0 = RTI interrupts disabled

RTR1–RTR0 — Real-Time Interrupt Rate

These read/write bits select one of four real-time interrupt rates, as shown in **Table 6**. The RT1 and RT0 bits also determine the COP reset period, as shown in **Table 7**.

Table 6. Real-Time Interrupt Clock Frequency Selection

TBCLK	RTR1:RTR0	Divide Ratio	Real-Time Interrupt Frequency (Hz)		
			OSC = 4.0 MHz	OSC = 4.1943 MHz	XOSC = 32.768 kHz
1	0 0	OSC ÷ 2^{14}	244	256	—
1	0 1	OSC ÷ 2^{19}	7.63	8.00	—
1	1 0	OSC ÷ 2^{20}	3.81	4.00	—
1	1 1	OSC ÷ 2^{21}	1.91	2.00	—
0	0 0	XOSC ÷ 2^{7}	—	—	256
0	0 1	XOSC ÷ 2^{12}	—	—	8.00
0	1 0	XOSC ÷ 2^{13}	—	—	4.00
0	1 1	XOSC ÷ 2^{14}	—	—	2.00

Table 7. COP Timeout Period Selection

TBCLK	RTR1:RTR0	Divide Ratio	COP Timeout Period (ms)					
			OSC = 4.0 MHz		OSC = 4.1943 MHz		XOSC = 32.768 kHz	
			Min	Max	Min	Max	Min	Max
1	0 0	OSC ÷ 2^{16}	12.3	16.4	11.7	15.6	—	—
1	0 1	OSC ÷ 2^{21}	393	524	375	500	—	—
1	1 0	OSC ÷ 2^{22}	786	1048	750	1000	—	—
1	1 1	OSC ÷ 2^{23}	1573	2097	1500	2000	—	—
0	0 0	XOSC ÷ 2^{9}	—	—	—	—	11.7	15.6
0	0 1	XOSC ÷ 2^{14}	—	—	—	—	375	500
0	1 0	XOSC ÷ 2^{15}	—	—	—	—	750	1000
0	1 1	XOSC ÷ 2^{16}	—	—	—	—	1500	2000

RRTIF — Reset Real-Time Interrupt Flag

RRTIF is a write-only bit and always reads as zero. Setting the RRTIF bit clears the RTIF bit. Writing zero to RRTIF has no effect.

COPE — COP Enable

This read/write-once bit enables COP resets. Writing to COPE is allowed only once after a reset. COPE is cleared by a reset (including a COP reset).

1 = COP resets enabled
0 = COP resets disabled

COPC — COP Clear

This write-only bit clears the COP divider and prevents a COP timeout. COP always reads as zero.

Timers

The two MC68HC05L5 timers provide two timer input pins and one timer output pin. **Figure 11** shows the structure of the timer system.

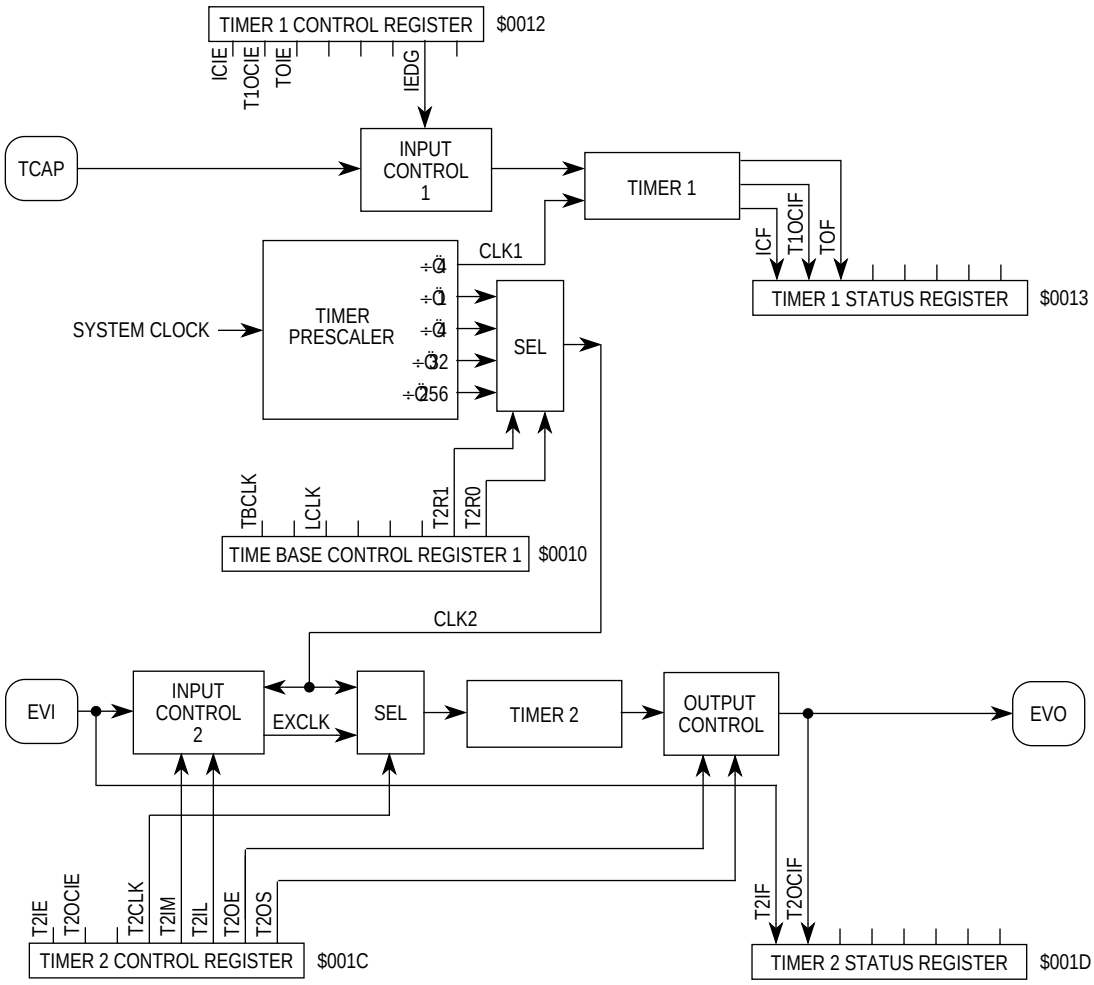


Figure 11. Timer 1 and Timer 2

Timer 1

Timer 1 is a 16-bit free-running up counter with 16-bit input capture and 16-bit output compare functions. The input capture function latches the counter value and generates an interrupt request when a selected edge

(either rising or falling) occurs on the TCAP input pin. Software can later read this counter value to determine when the edge occurred.

The output compare function generates an interrupt request when the counter value matches the value programmed in the timer 1 output compare register.

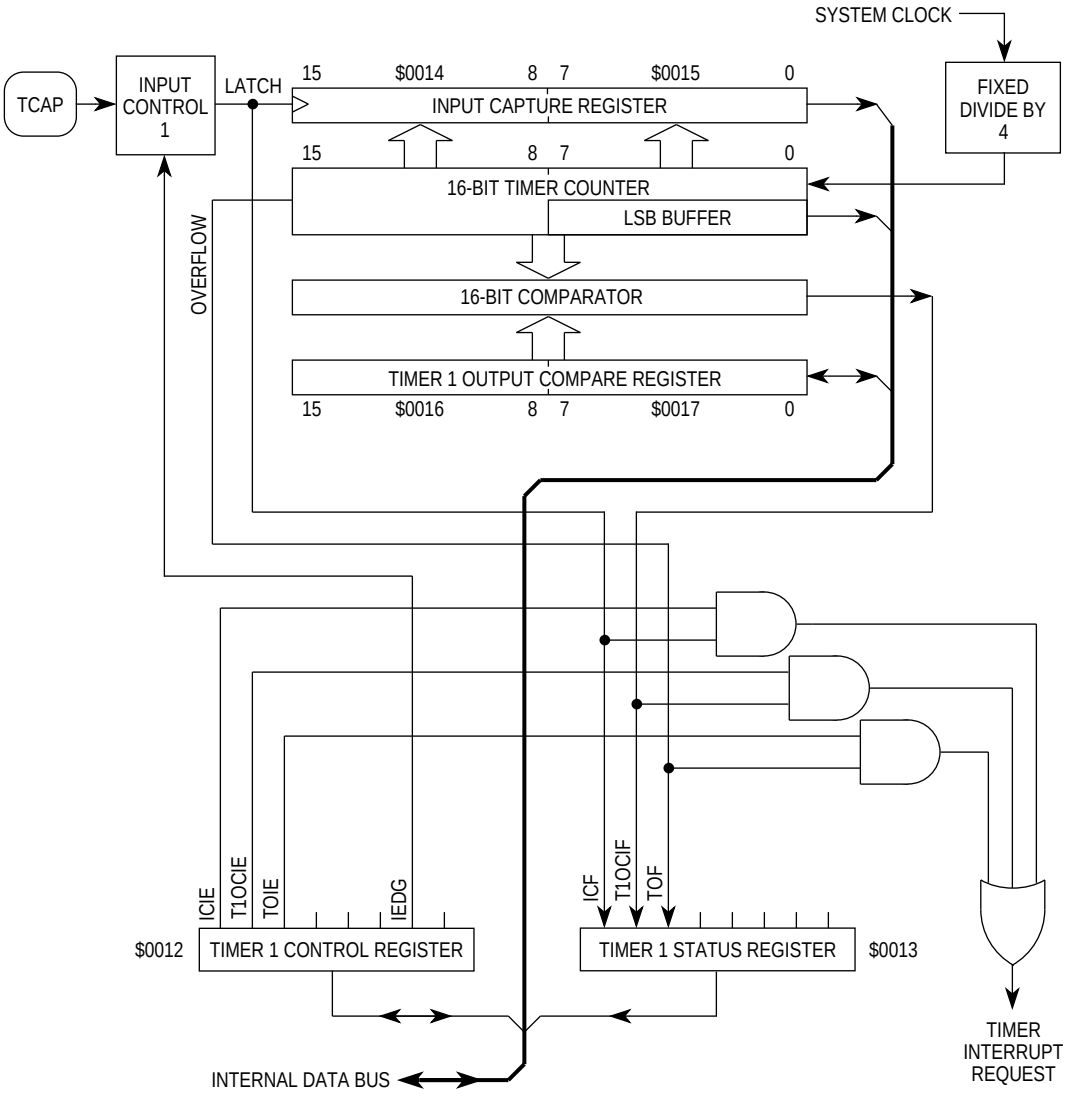


Figure 12. Timer 1

Timer 1 Control Register (T1CR)

Address: $0012

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ICIE	T1OCIE	TOIE	0	0	0	IEDG	0
Reset:	0	0	0	0	0	0	U	0

U = Unaffected

ICIE — Input Capture Interrupt Enable

This read/write bit enables timer 1 input capture interrupts.

1 = Timer 1 input capture interrupts enabled
0 = Timer 1 input capture interrupts disabled

T1OCIE — Timer 1 Output Compare Interrupt Enable

This read/write bit enables timer 1 output compare interrupts.

1 = Timer 1 output compare interrupts enabled
0 = Timer 1 output compare interrupts disabled

TOIE — Overflow Interrupt Enable

This read/write bit enables timer 1 overflow interrupts.

1 = Timer 1 overflow interrupts enabled
0 = Timer 1 overflow interrupts disabled

IEDG — Input Edge

This read/write bit determines whether a rising or a falling edge on the TCAP pin causes a transfer of the counter contents to the input capture register.

1 = Rising edge transfers counter contents
0 = Falling edge transfers counter contents

Timer 1 Status Register (T1SR)

Address: $0013

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ICF	T1OCIF	TOF	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

ICF — Input Capture Flag

This read-only bit is set when a selected edge occurs on the TCAP pin. Clear the ICF bit by reading the timer 1 status register with ICF set, and then reading the low byte of the input capture register.

T1OCIF — Timer 1 Output Compare Interrupt Flag

This read-only bit is set when the counter value matches the contents of the timer 1 output compare register. Clear the T1OCIF bit by reading the timer 1 status register with T1OCIF set, and then reading the low byte of the timer 1 output compare register.

TOF — Timer Overflow Flag

This read-only bit is set when the counter rolls over from $FFFF to $0000. Clear the TOF bit by reading the timer 1 status register with TOF set, and then reading the low byte of the timer 1 counter register.

Input Capture Register (ICR)

Address: $0014 — ICR High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	Unaffected by Reset							

Address: $0015 — ICR Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Unaffected by Reset							

When a selected edge occurs on the TCAP pin, the current value of the counter is latched into the input capture register. Reading the high byte of the input capture register inhibits further captures until the low byte is read. Writing to the input capture register has no effect. (See **Figure 13**.)

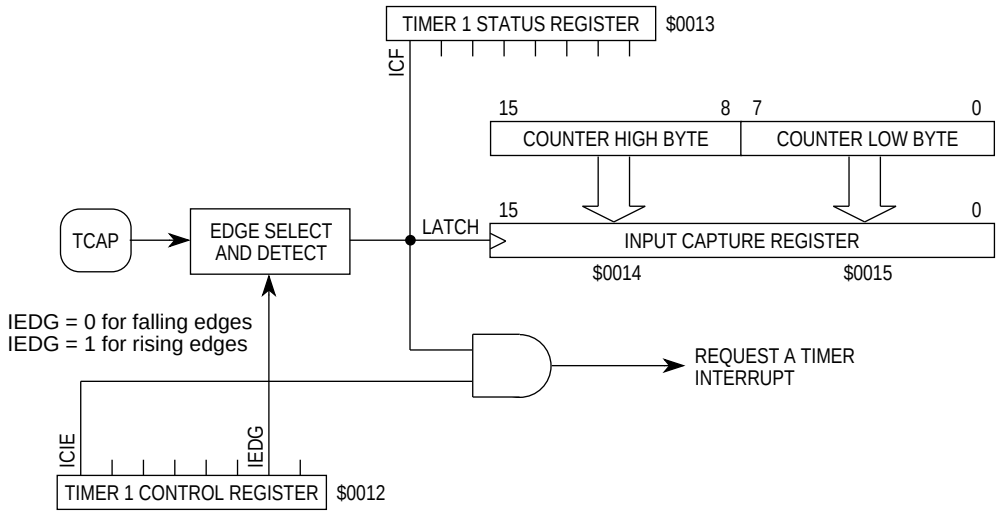


Figure 13. Input Capture Operation

Timer 1 Output Compare Register (T1OCR)

Address: $0016 — T1OCR High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	Unaffected by Reset							

Address: $0017 — T1OCR Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Unaffected by Reset							

When the value of the counter matches the value in the timer 1 output compare register, the T1OCIF bit in the timer 1 status register is set. If the T1OCIE bit in the timer 1 control register is also set, an interrupt is generated. Writing to the high byte of the timer 1 output compare register inhibits timer compares until the low byte is written.

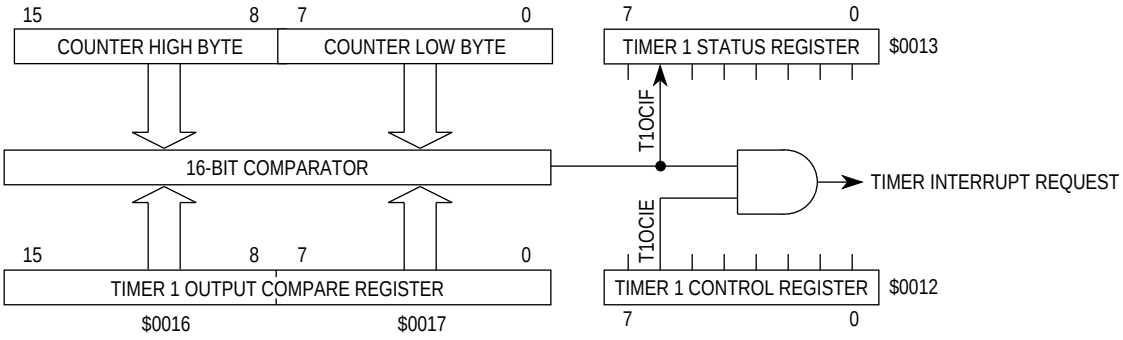


Figure 14. Output Compare Operation

Timer 1 Counter Register (T1CNTR)

Address: $0018 — T1CNTR High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	On reset, T1CNTR is preset to $FFFC.							

Address: $0019 — T1CNTR Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	On reset, T1CNTR is preset to $FFFC.							

The timer 1 counter register contains the current counter value. Reading the high byte causes the low byte to be latched into a buffer. Reading the low byte after reading the timer 1 status register clears the TOF bit. Writing to the timer 1 counter register has no effect.

Timer 1 Alternate Counter Register (T1ALTCNTR)

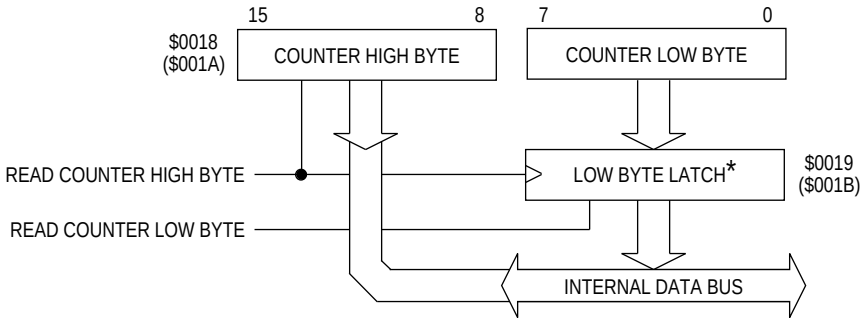
Address: $001A — T1ALTCNTR High

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset:	On reset, T1ALTCNTR is preset to $FFFC.							

Address: $001B — T1ALTCNTR Low

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	On reset, T1ALTCNTR is preset to $FFFC.							

The timer 1 alternate counter register contains the current counter value. Reading the high byte causes the low byte to be latched into a buffer. Reading the timer 1 alternate counter register does not affect the TOF bit. Writing to this register has no effect. (See **Figure 15**.)



*The low byte latch is normally transparent. It latches when the high byte of the counter is read and becomes transparent again when the low byte of the counter is read.

Figure 15. 16-Bit Counter Reads

Timer 2

Timer 2 (see **Figure 16**) is an 8-bit up counter with an 8-bit output compare function, an event input pin, and an event output pin. The output compare function presets the timer 2 counter to $01 and generates an interrupt request when the counter reaches the value programmed into the output compare register.

Either the EVI input or the prescaled system clock (CLK2) can drive timer 2. In event mode, the EVI input drives timer 2 directly. In gated mode, the EVI input gated by CLK2 drives timer 2.

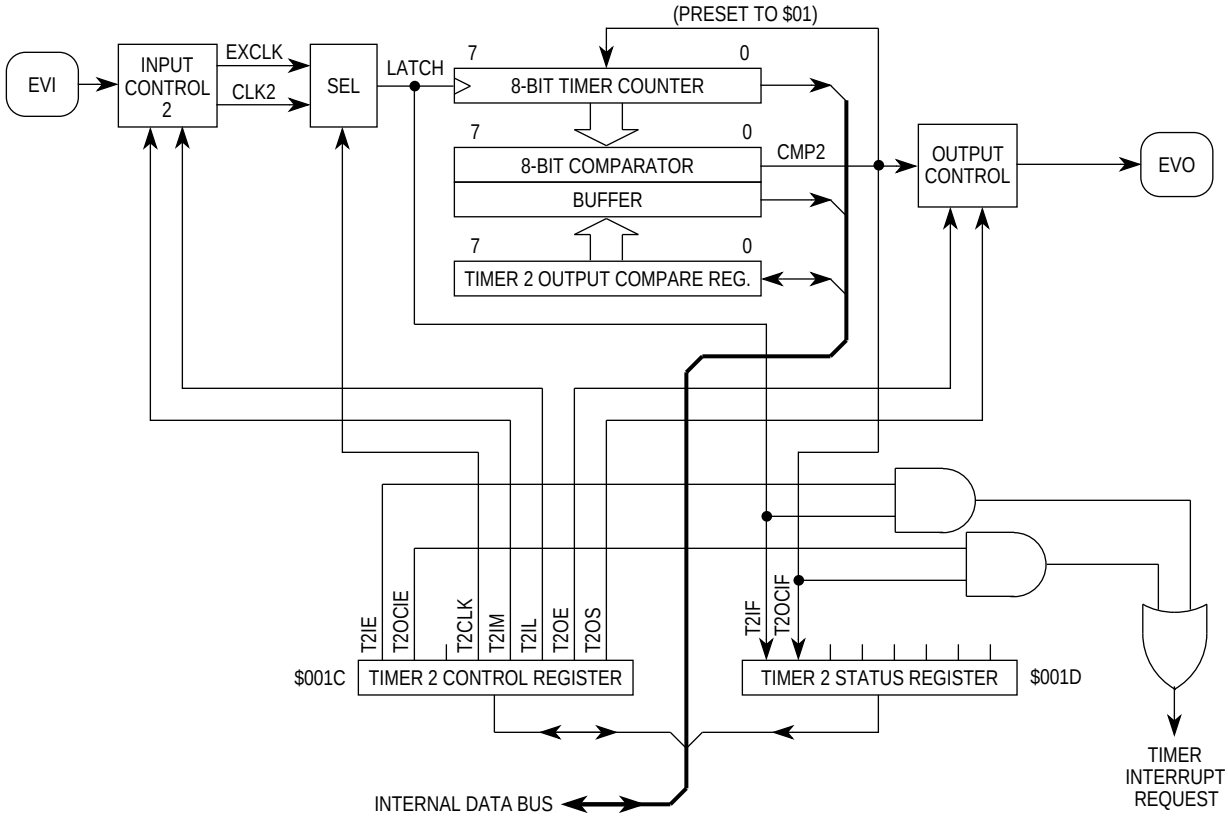


Figure 16. Timer 2

Timer 2 Control Register (T2CR)

Address: $001C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	T2IE	T2OCIE	0	T2CLK	T2IM	T2IL	T2OE	T2OS
Reset:	0	0	0	0	0	0	0	0

T2IE — Timer 2 Interrupt Enable

This read/write bit enables timer 2 interrupts when the T2IF bit in the timer 2 status register is set.

1 = Timer 2 interrupts enabled
0 = Timer 2 interrupts disabled

T2OCIE — Timer 2 Output Compare Interrupt Enable

This read/write bit enables timer 2 interrupts when the T2OCIF bit in the timer 2 status register is set.

1 = Timer 2 output compare interrupts enabled
0 = Timer 2 output compare interrupts disabled

T2CLK — Timer 2 Clock

This read/write bit selects the clock source for timer 2.

1 = EXCLK from EVI is selected
0 = CLK2 from timer prescaler is selected

T2IM — Timer 2 Input Mode

This read/write bit selects prescaled system clock (CLK2) gating of the EVI input.

1 = Timer 2 driven by CLK2-gated EVI input (gated mode)
0 = Timer 2 driven by EVI input directly (event mode)

T2IL — Timer 2 Input Level

This read/write bit selects the active edge (rising or falling) of EVI in event mode, and the gate enable level of EVI in gated mode. (See **Table 8**.)

1 = Rising edge on EVI increments counter (event mode)
High level on EVI enables counting (gated mode)
0 = Falling edge on EVI increments counter (event mode)
Low level on EVI enables counting (gated mode)

Table 8. EVI Mode Selection

T2IM:T2IL	Mode	Action on Counter
0 0	Event	EVI Falling Edge Increments Counter
0 1	Event	EVI Rising Edge Increments Counter
1 0	Gated	EVI Low Level Enables Counting
1 1	Gated	EVI High Level Enables Counting

T2OE — Timer 2 Output Enable

This read/write bit determines whether the PC5/EVO pin is a bidirectional I/O pin (PC5) or the timer 2 output pin (EVO). Changing the T2OE bit does not change the PC5/EVO pin function immediately. A synchronization delay occurs until a rising or falling edge occurs on the PC5/EVO pin as selected by the T2OS bit.

1 = EVO output enabled
0 = PC5 bidirectional I/O enabled

T2OS — Timer 2 Output Synchronize

This read/write bit selects either a falling or a rising edge on the PC5/EVO pin to change the function of the PC5/EVO pin.

1 = Rising edge on PC5/EVO pin changes pin function
0 = Falling edge on PC5/EVO pin changes pin function

The timer 2 input control circuit synchronizes the EVI input with the falling edge of the system clock (see **Figure 17**). The minimum external clock pulse width should be larger than one system clock pulse width.

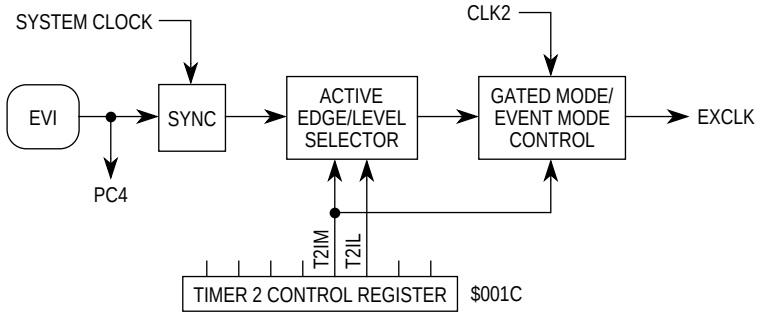


Figure 17. EVI Input Control

The T2IM bit determines whether the EVI pin drives timer 2 directly (event mode) or is gated by CLK2 (gated mode). In event mode the T2IL bit determines which EVI edge increments timer 2. In gated mode, the T2IL bit determines which EVI level enables timer 2 to count.

To avoid an illegal timer 2 count, software should preset the timer 2 counter register after changing the T2IM bit.

The timer 2 output control circuit enables and synchronizes the EVO output (see **Figure 18**). A divide-by-two prescaler divides the timer 2 output compare signal, CMP2, to produce a 50% duty output. The prescaler is initialized to the state of the T2OS bit in the timer 2 control register when the CPU writes to the timer 2 counter register.

The T2OE bit enables the EVO. To avoid an incomplete EVO pulse, T2OE must be changed synchronously with the EVO signal. The T2OS bit selects a synchronizing EVO edge.

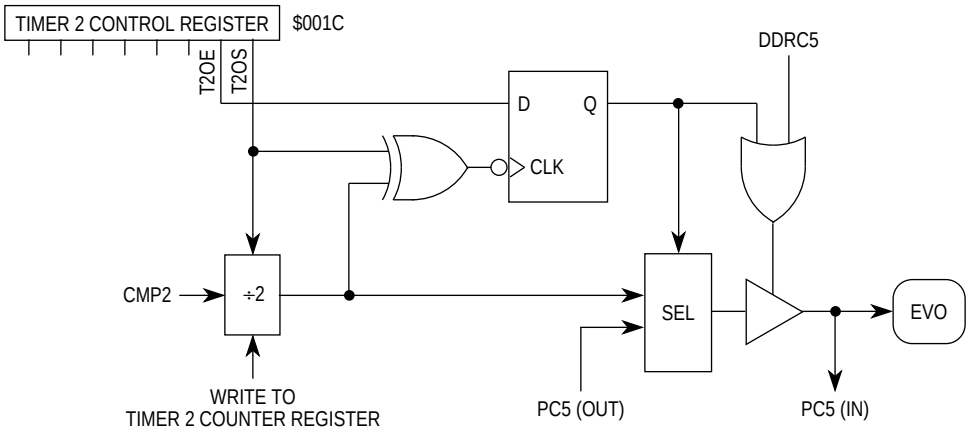


Figure 18. EVO Output Control

Timer 2 Status Register (T2SR)

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	T2IF	T2OCIF	0	0	RT2IF	RT2OCIF	0	0
Reset:	0	0	0	0	0	0	0	0

T2IF — Timer 2 Input Flag

In event mode this read-only bit is set when the event edge occurs on the EVI pin. In gated mode the T2IF bit is set when the trailing edge of the gating signal occurs on EVI.

T2OCIF — Timer 2 Output Compare Interrupt Flag

This read-only bit is set when a timer 2 output compare occurs.

RT2IF — Reset Timer 2 Input Flag

This write-only bit always reads as zero. Setting RT2IF clears the T2IF bit. Clearing RT2IF has no effect.

RT2OCIF — Reset Timer 2 Output Compare Interrupt Flag

This write-only bit always reads as zero. Setting RT2OCIF clears the T2OCIF flag. Clearing RT2OCIF has no effect.

Timer 2 Output Compare Register (T2OCR)

Address: $001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	1	1	1	1	1	1	1	1

This read/write register contains a user-supplied value that is continuously compared with the value in the timer 2 counter. When the two values match, a comparator presets the timer 2 counter to $01, and sets the T2OCIF bit in the timer 2 status register.

Timer 2 Counter Register (T2CNTR)

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	0	0	0	0	0	0	0	1

This read/write register contains the current timer 2 counter value. Writing any value to the timer 2 counter register presets the counter to $01.

Liquid Crystal Display Driver

The features of the programmable liquid crystal display (LCD) driver subsystem include the following:

- Four backplane (BP) output pins and up to 39 frontplane (FP) output pins
- 20 data registers
- Three power supply pins

The following figures detail the LCD control register and the LCD data registers.

LCD Control Register (LCDCR)

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LCDE	DUTY1	DUTY0	0	PEH	PEL	PDH	0
Reset:	0	0	0	0	0	0	0	0

LCDE — LCD Enable

This read/write bit enables the LCD driver outputs. The LCDE bit does not affect port D and port E pins that are programmed as general-purpose outputs.

1 = BP and FP pins enabled to carry LCD waveforms
0 = BP and FP outputs disabled; V_{DD} appears on all implemented BP and FP pins

DUTY1–DUTY0 — Duty Select

These read/write bits determine how many BP outputs are used, as the following table shows. Unused BP pins are general-purpose port D pins.

Table 9. LCD Duty Selection

Duty	LCD Control	Pin Function			
	DUTY1:DUTY0	BP3/PD3	BP2/PD2	BP1/PD1	BP0
1/1	0 1	PD3	PD2	PD1	BP0
1/2	1 0	PD3	PD2	BP1	BP0
1/3	1 1	PD3	BP2	BP1	BP0
1/4	0 0	BP3	BP2	BP1	BP0

PEH — Port E High

This read/write bit enables the upper four bits of port E as general-purpose outputs.

1 = PE7–PE4 selected
0 = FP27–FP30 selected

PEL — Port E Low

This read/write bit enables the lower four bits of port E as general-purpose outputs.

1 = PE3–PE0 selected
0 = FP31–FP34 selected

PDH — Port D High

This read/write bit enables the upper four bits of port D as general-purpose outputs.

1 = PD7–PD4 selected
0 = FP35–FP38 selected

LCD Data Registers 1–20 (LCDDR1–LCDDR20)

Address: $0021–$0034

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	FyB3	FyB2	FyB1	FyB0	FxB3	FxB2	FxB2	FxB0
Reset:	Unaffected by Reset							

Each nibble in an LCD data register controls the waveform of a frontplane driver.

BP3–BP0 — Backplane 3–0

1 = Backplane output selected

0 = Backplane output deselected

Figure 19, **Figure 20**, **Figure 21**, and **Figure 22** show example LCD driver waveforms.

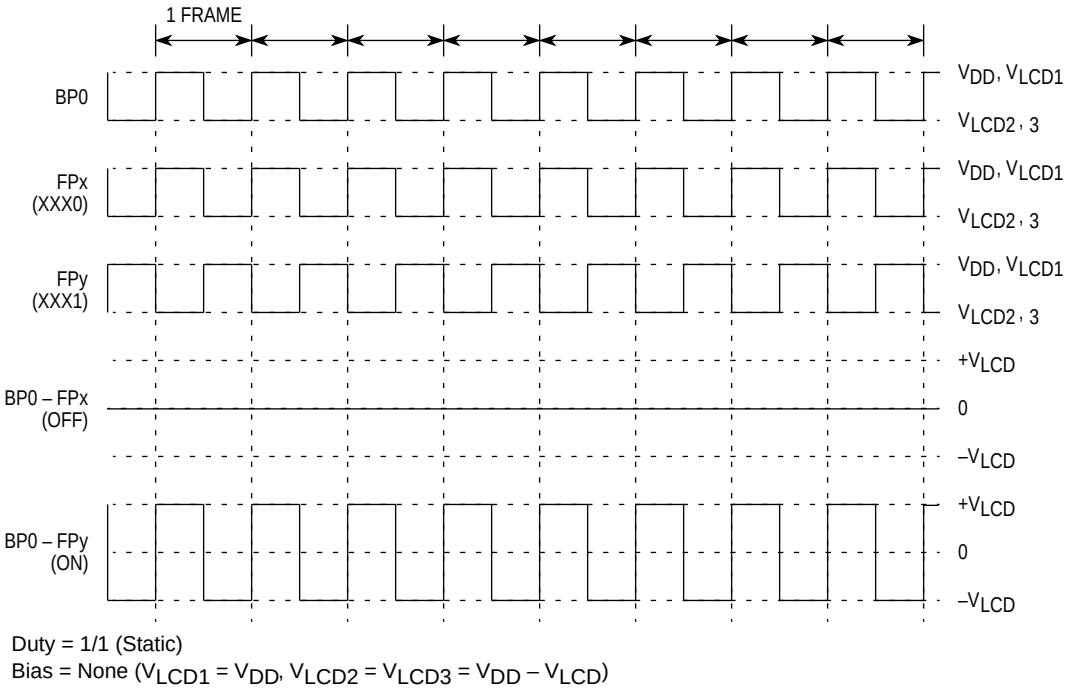
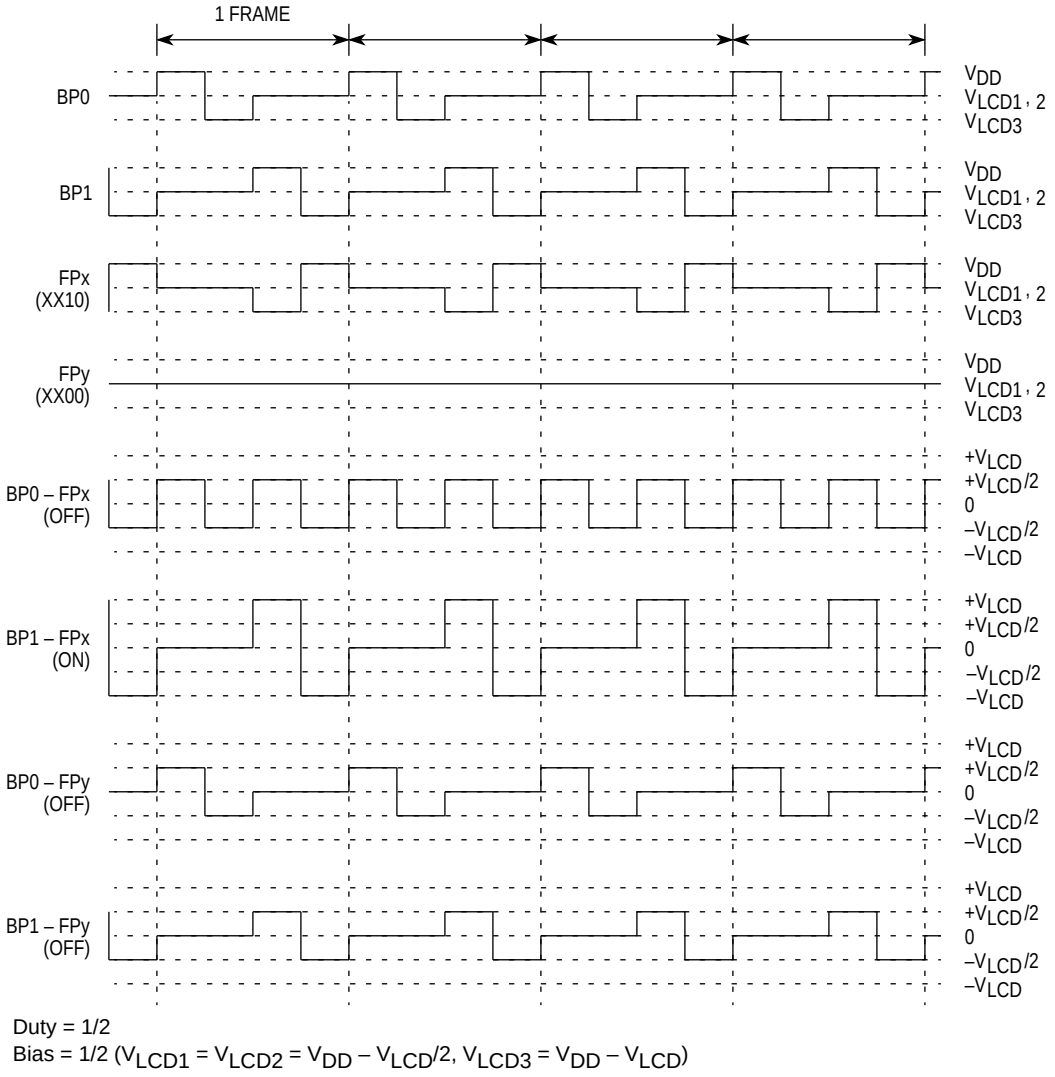
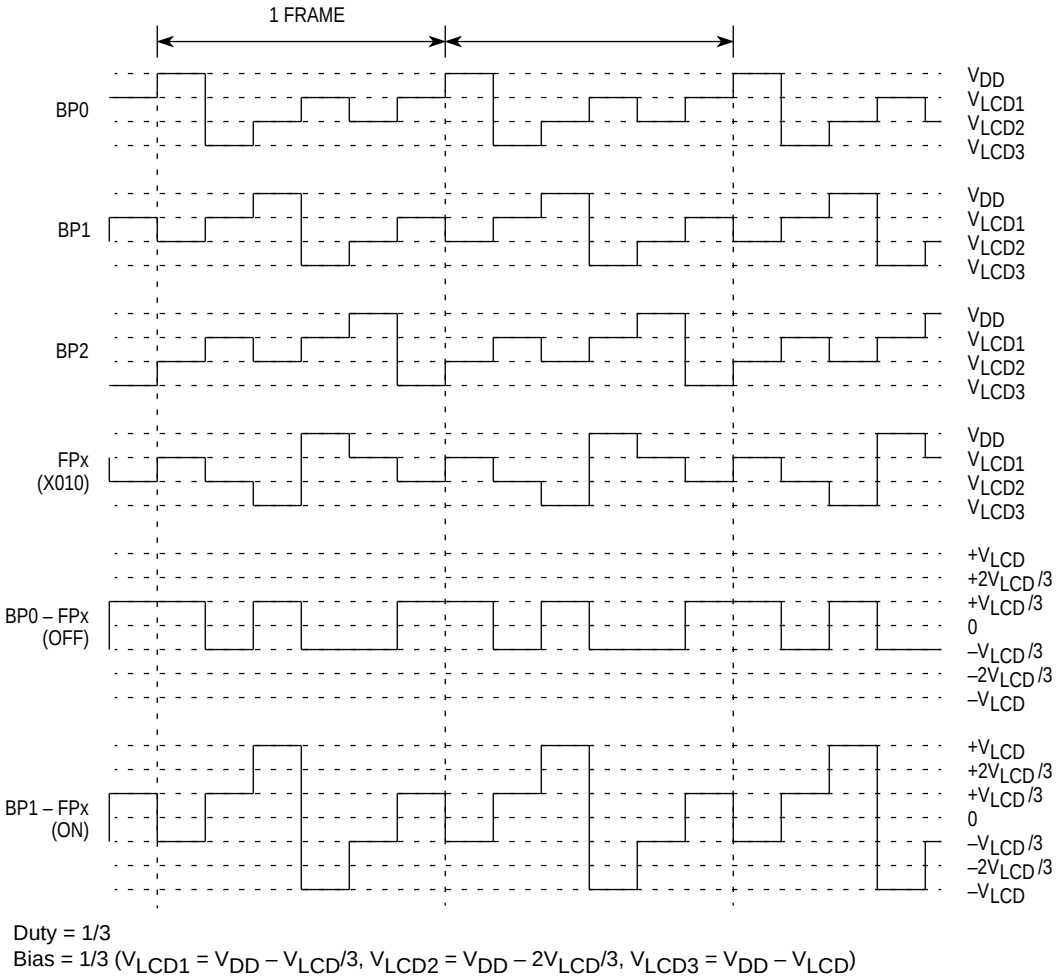


Figure 19. 1/1 Duty and 1/1 Bias



Duty = 1/2
Bias = 1/2 ($V_{LCD1} = V_{LCD2} = V_{DD} - V_{LCD}/2$, $V_{LCD3} = V_{DD} - V_{LCD}$)

Figure 20. 1/2 Duty and 1/2 Bias



Duty = 1/3
Bias = 1/3 ($V_{LCD1} = V_{DD} - V_{LCD}/3$, $V_{LCD2} = V_{DD} - 2V_{LCD}/3$, $V_{LCD3} = V_{DD} - V_{LCD}$)

Figure 21. 1/3 Duty and 1/3 Bias

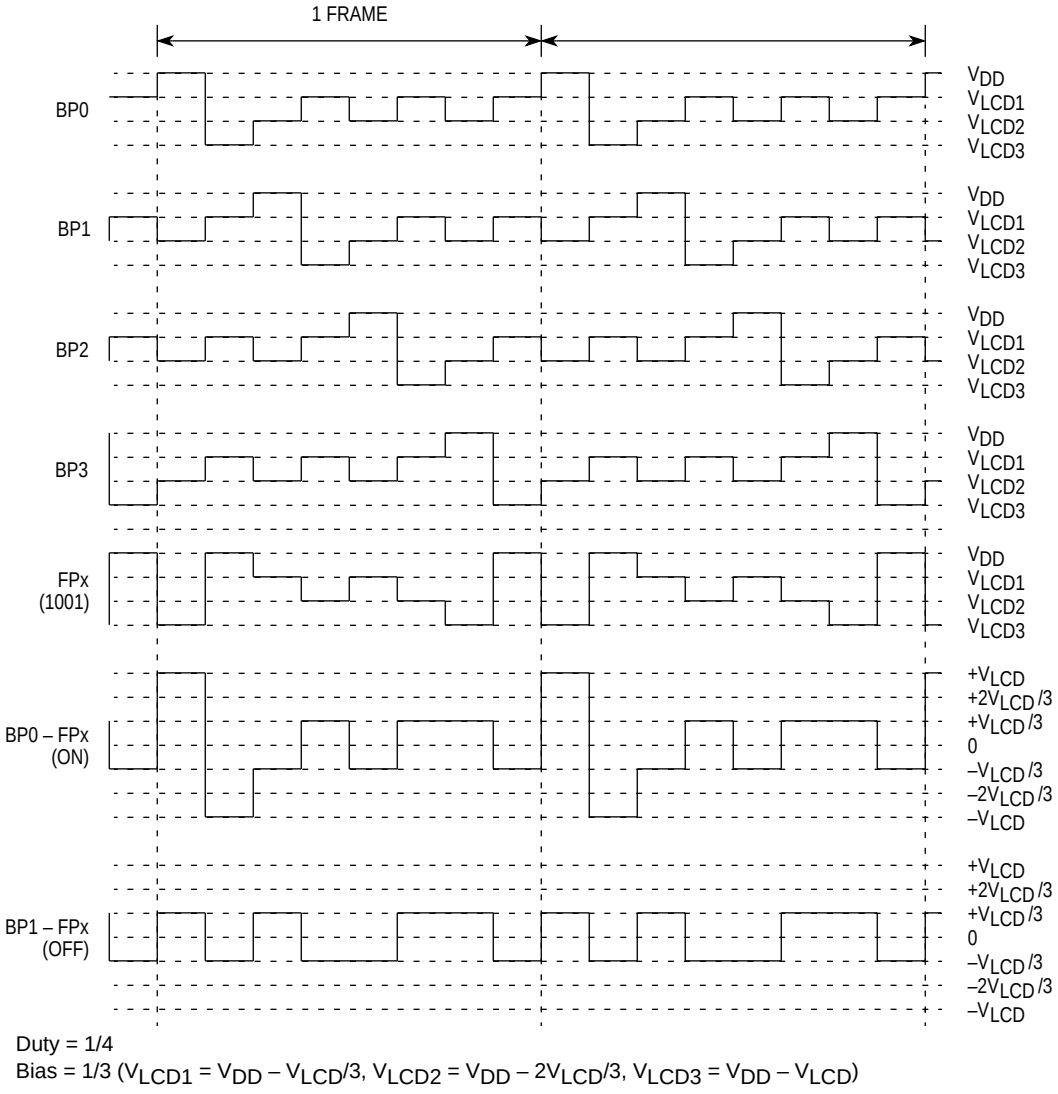


Figure 22. 1/4 Duty and 1/3 Bias

Serial Peripheral Interface

The serial peripheral interface (SPI) allows high-speed synchronous serial data transfer between the MC68HC05L5 and peripheral devices or between several MC68HC05L5s.

- Full Duplex, Three Wire Synchronous Data Transfers
- Master or Slave Operation
- 1.05-MHz (Maximum) Bit Frequency
- LSB First or MSB First Data Transfer
- Two Programmable Bit Rates
- End of Transmission Interrupt Flag
- Data Collision Flag Protection
- Wakeup from Stop Mode (Slave Mode Only)

Figure 23 shows the structure of the SPI.

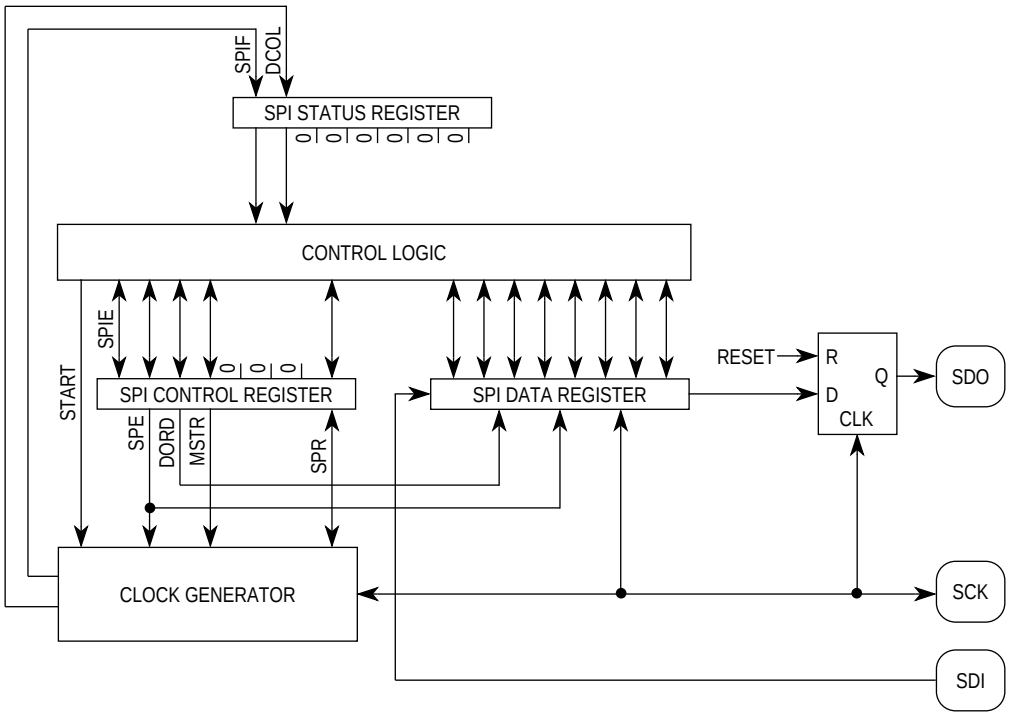


Figure 23. SPI Structure

Figure 24 shows the interconnection between master and slave MCUs. In master mode the SCK pin functions as the clock output. In slave mode the SCK pin is an input. Writing to the SPI data register of the master MCU starts the master clock generator, and the data written shifts out the master SDO pin and into the slave SDI pin. After shifting one byte, the master clock generator stops, setting the end of transmission flag (SPIF). If the SPI interrupt enable bit (SPIE) is set, an interrupt is requested.

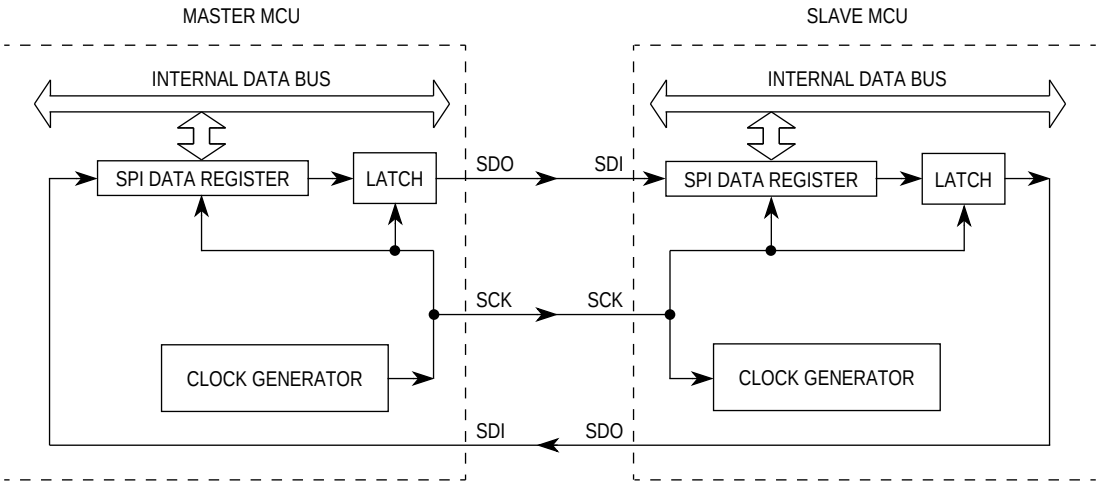


Figure 24. Master-Slave Interconnection

SPI Control Register (SPCR)

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	DORD	MSTR	0	0	0	SPR
Reset:	0	0	0	0	0	0	0	0

SPIE — SPI Interrupt Enable

This read/write bit enables interrupts.

1 = SPI interrupts enabled

0 = SPI interrupts disabled

SPE — SPI Enable

This read/write bit enables the SPI system and connects SDI, SDO, and SCK to pins PC0, PC1, and PC2.

1 = SPI enabled
0 = SPI disabled

DORD — Data Order

This read/write bit selects LSB first or MSB first data transmission.

1 = LSB first
0 = MSB first

MSTR — Master

This read/write bit determines whether the SPI is in master or slave mode.

1 = Master mode
0 = Slave mode

SPR — SPI Rate

This read/write bit selects the clock rate of SCK.

1 = System clock divided by 2
0 = System clock divided by 16

SPI Status Register (SPSR)

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIF	DCOL	0	0	0	0	0	0
Reset:	0	0	0	0	0	0	0	0

SPIF — SPI Interrupt Flag

This read-only bit is set when a serial transfer is complete and generates an interrupt if the SPIE bit is set. Clear the SPIF bit by reading the SPI status register with SPIF set, and then accessing the SPI data register.

DCOL — Data Collision

This read-only bit is set when the serial peripheral data register is accessed during a data transfer. During a data transfer, reads of the SPDR may be incorrect, and writes to it have no effect. Clear the DCOL bit (and the SPIF bit) by reading the SPI status register with SPIF and DCOL set, and then accessing the SPI data register.

SPI Data Register (SPDR)

Address: $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset:	Unaffected by Reset							

This read/write register contains SPI data. Accessing the SPI data register during a serial transfer sets the DCOL bit.

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