# MC68HC05J1A MC68HCL05J1A MC68HSC05J1A

Addendum to
MC68HC05J1A
HCMOS Microcontroller Unit
Technical Data

This addendum supplements *MC68HC05J1A Technical Data* (Motorola document number MC68HC05J1A/D) with the following additional information:

- Corrections to MC68HC05J1A Technical Data (including Typical RC responses).
- MC68HCL05J1A data Appendix A contains data for the MC68HCL05J1A, a low-power version of the MC68HC05J1A
- MC68HSC05J1A data Appendix B contains data for the MC68HSC05J1A, a high-speed version of the MC68HC05J1A

#### NOTE

For convenience, this manual contains change bars. These bars appear in the margin and highlight those areas of the manual that have been revised since the last publication.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



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# CORRECTIONS MC68HC05J1A/D

Corrections to the technical data manual are as follows:

 Page 10-3, Table 10-3. DC Electrical Characteristics (V<sub>DD</sub> = 5.0 V) — change the third table entry (Output Low Voltage) as follows:

From:

Characteristic	Symbol	Min	Тур	Max	Unit
Output Low Voltage PA3-PA0 (I <sub>LOAD</sub> = 1.6 mA) PA7-PA4 (I <sub>LOAD</sub> = 8.0 mA)	V <sub>OL</sub>		_	0.4 0.4	V

To:

Characteristic	Symbol	Min	Тур	Max	Unit
Output Low Voltage PA3-PA0, PB5-PB0 ( $I_{LOAD}$ = 1.6 mA) PA7-PA4 ( $I_{LOAD}$ = 8.0 mA)	$V_{OL}$		_ _	0.4 0.4	V

2. Page 10-5. Replace the figure title for **Figure 10-1** as follows:

From:

Figure 10-1. 
$$V_{OH}/I_{OH}$$
 ( $V_{DD} = 5.0 \text{ V}$ )

To:

Figure 10-1. Typical 
$$V_{OH}/I_{OH}$$
 ( $V_{DD} = 5.0 \text{ V}$ )

3. Page 10-5. Replace the figure title for **Figure 10-2** as follows:

From:

Figure 10-2. 
$$V_{OH}/I_{OH}$$
 ( $V_{DD} = 3.3 \text{ V}$ )

To:

Figure 10-2. Typical 
$$V_{OH}/I_{OH}$$
 ( $V_{DD} = 3.3 \text{ V}$ )

4. Page 10-5. Replace the figure title for **Figure 10-3** as follows:

From:

Figure 10-3. 
$$V_{OL}/I_{OL}$$
 ( $V_{DD} = 5.0 \text{ V}$ )

To:

Figure 10-3. Typical 
$$V_{OL}/I_{OL}$$
 ( $V_{DD} = 5.0 \text{ V}$ )

5. Page 10-5. Replace the figure title for **Figure 10-4** as follows:

From:

Figure 10-4. 
$$V_{OL}/I_{OL}$$
 ( $V_{DD} = 3.3 \text{ V}$ )

To:

Figure 10-4. Typical 
$$V_{OL}/I_{OL}$$
 ( $V_{DD} = 3.3 \text{ V}$ )

6. Page 1-7. Add the following figure after Figure 10-6.

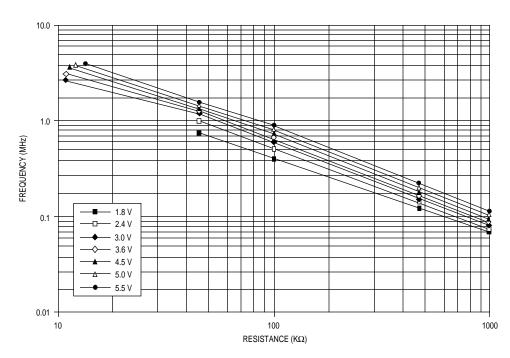


Figure 10-7. Typical Internal Operating Frequency for Various  $V_{DD}$  at 25  $^{\circ}C$  — RC Option Only

# APPENDIX A MC68HCL05J1A

This appendix introduces the MC68HCL05J1A, a low-power version of the MC68HC05J1A. All of the information in *MC68HC05J1A Technical Data* applies to the MC68HCL05J1A with the exceptions given in this appendix.

#### A.1 DC ELECTRICAL CHARACTERISTICS

The data in Table 10-3 and Table 10-4 of *MC68HC05J1A Technical Data* applies to the MC68HCL05J1A with the following exceptions in Table A-1, Table A-2, Table A-3, and Table A-4.

Table A-1. Low-Power Output Voltage ( $V_{DD} = 1.8-2.4 \text{ Vdc}$ )

Characteristic	Symbol	Min	Тур	Max	Unit
Output High Voltage (I <sub>LOAD</sub> = -0.1 mA) PA7-PA0, PB5-PB0	V <sub>OH</sub>	V <sub>DD</sub> -0.3	_	_	V
Output Low Voltage PA3-PA0 (I <sub>LOAD</sub> = 0.2 mA) PA7-PA4 (I <sub>LOAD</sub> = 2.0 mA)	V <sub>OL</sub>	_ _	_	0.3 0.3	V

Table A-2. Low-Power Output Voltage ( $V_{DD} = 2.5-3.6 \text{ Vdc}$ )

Characteristic	Symbol	Min	Тур	Max	Unit
Output High Voltage (I <sub>LOAD</sub> = -0.2 mA) PA7-PA0, PB5-PB0	V <sub>OH</sub>	V <sub>DD</sub> -0.3	_	_	V
Output Low Voltage PA3–PA0 (I <sub>LOAD</sub> = 0.4 mA) PA7–PA4 (I <sub>LOAD</sub> = 5.0 mA)	V <sub>OL</sub>	_ _	_	0.3 0.3	V

**Table A-3. Low-Power Supply Current** 

Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
Supply Current ( $V_{DD}$ = 4.5–5.5 Vdc, $f_{OP}$ = 2.1 MHz) Run <sup>2</sup> WAIT <sup>3</sup> STOP <sup>4</sup>	I <sub>DD</sub>		3.0 1.6	4.0 2.5	mA mA
25 °C 0 °C to 70 °C (Standard)		_ _	0.2 2.0	10 20	μA μA
Supply Current ( $V_{DD}$ = 2.5–3.6 Vdc, $f_{OP}$ = 1.0 MHz) Run <sup>(2)</sup> WAIT <sup>(3)</sup> STOP <sup>(4)</sup>	I <sub>DD</sub>		1.0 0.5	2.0 1.0	mA mA
25 °C 0 °C to 70 °C (Standard)		_	0.1 1.0	5.0 10.0	μA μA
Supply Current ( $V_{DD}$ = 2.5–3.6 Vdc, $f_{OP}$ = 500 kHz) Run <sup>(2)</sup> WAIT <sup>(3)</sup> STOP <sup>(4)</sup>	I <sub>DD</sub>		0.5 250	1.0 500	mA μA
25 °C 0 °C to 70 °C (Standard)			0.1 1.0	5.0 10.0	μA μA
Supply Current ( $V_{DD}$ = 1.8–2.4 Vdc, $f_{OP}$ = 500 kHz) Run <sup>(2)</sup> WAIT <sup>(3)</sup> STOP <sup>(4)</sup>	I <sub>DD</sub>	_	300 150	700 400	μΑ μΑ
25 C 0 °C to 70 °C (Standard)		<u> </u>	0.1 1.0	2 5	μA μA

- 1. Typical values reflect average measurements at midpoint of voltage range at 25  $^{\circ}\text{C}.$
- 2. Run (operating)  $I_{DD}$  measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs.  $C_L = 20$  pF on OSC2. 3. WAIT  $I_{DD}$  measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less
- than 50 pF on all outputs.  $C_L = 20$  pF on OSC2. All ports configured as inputs.  $V_{IL} = 0.2$  V,  $V_{IH} = V_{DD} 0.2$  V. OSC2 capacitance linearly affects WAIT  $I_{DD}$ . 4. STOP  $I_{DD}$  measured with OSC1 =  $V_{DD}$ . All ports configured as inputs.  $V_{IL} = 0.2 \text{ V}$ ,  $V_{IH} = V_{DD} - 0.2 \text{ V}$ .

**Table A-4. Low-Power Pulldown Current** 

Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
Pulldown Current ( $V_{DD}$ = 4.5–5.5 Vdc, $f_{OP}$ = 2.1 MHz) PA7–PA0, PB5–PB0 (Pulldown Device On)	I <sub>IL</sub>	50	100	200	μА
Pulldown Current ( $V_{DD}$ = 2.5–3.6 Vdc, $f_{OP}$ = 1.0 MHz) PA7–PA0, PB5–PB0 (Pulldown Device On)	I <sub>IL</sub>	8	30	100	μА
Pulldown Current ( $V_{DD}$ = 2.5–3.6 Vdc, $f_{OP}$ = 500 kHz) PA7–PA0, PB5–PB0 (Pulldown Device On)	I <sub>IL</sub>	3	10	50	μА
Pulldown Current ( $V_{DD}$ = 1.8–2.4 Vdc, $f_{OP}$ = 500 kHz) PA7–PA0, PB5–PB0 (Pulldown Device On)	I <sub>IL</sub>	3	10	50	μА

<sup>1.</sup> Typical values reflect average measurements at midpoint of voltage range at 25  $^{\circ}\text{C}.$ 

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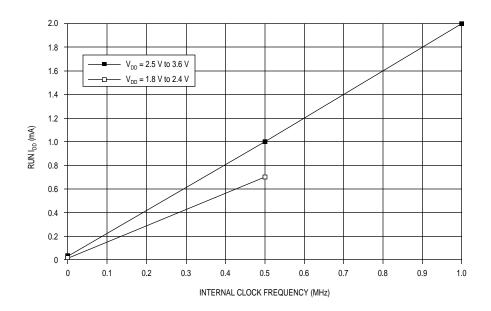


Figure A-1. Maximum Run Mode  $I_{\rm DD}$  vs Frequency

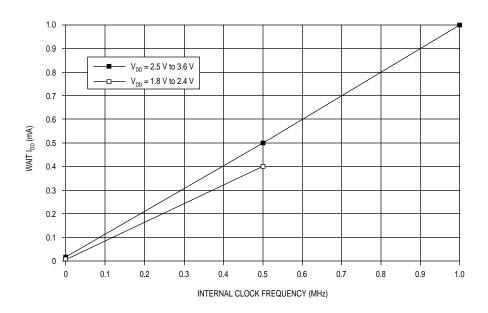


Figure A-2. Maximum WAIT Mode  $\mathbf{I}_{\mathrm{DD}}$  vs Frequency

## A.2 MC ORDERING INFORMATION

Table A-5 gives order numbers for the available package types.

**Table A-5. MC Order Numbers** 

Package Type	Temperature Range	Order Number
20-Pin Dual In-Line Package (DIP)	0 °C to 70 °C	MC68HCL05J1AP
20-Pin Small Outline Integrated Circuit (SOIC)	0 °C to 70 °C	MC68HCL05J1ADW

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#### **APPENDIX B** MC68HSC05J1A

This appendix introduces the MC68HSC05J1A, a high-speed version of the MC68HC05J1A. All of the information in MC68HC05J1A Technical Data applies to the MC68HSC05J1A with the exceptions given in this appendix.

#### **B.1 DC ELECTRICAL CHARACTERISTICS**

The data in Table 10-3 and Table 10-4 of MC68HC05J1A Technical Data applies to the MC68HSC05J1A with the exceptions given in Table B-1.

**Table B-1. High-Speed Supply Current** 

Characteristic	Symbol	Min	Typ <sup>1</sup>	Max	Unit
Supply Current ( $V_{DD}$ = 4.5–5.5 Vdc, $f_{OP}$ = 4.0 MHz) Run <sup>2</sup> WAIT <sup>3</sup> STOP <sup>4</sup> 25 °C -40 °C to +85 °C	I <sub>DD</sub>	_ _ _	4.5 2.5 0.2 2.0	6.0 3.25 10 20	mA mA μA μA
Supply Current ( $V_{DD}$ = 3.0–3.6 Vdc, $f_{OP}$ = 2.1 MHz Run WAIT STOP 25 °C -40 °C to +85 °C	I <sub>DD</sub>	_ _ _	2.0 1.0 0.1 1.0	4.0 2.0 5.0 10	mA mA μA μA

<sup>1.</sup> Typical values reflect average measurements at midpoint of voltage range at 25  $^{\circ}$ C.

<sup>2.</sup> Run (operating)  $I_{DD}$  measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs.  $C_L = 20$  pF on OSC2.

<sup>3.</sup> WAIT I<sub>DD</sub> measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs.  $C_L = 20$  pF on OSC2. All ports configured as inputs.  $V_{IL} = 0.2 \text{ V}$ ,  $V_{IH} = V_{DD} - 0.2 \text{ V}$ . OSC2 capacitance linearly affects WAIT  $I_{DD}$ . 4. STOP  $I_{DD}$  measured with OSC1 =  $V_{DD}$ . All ports configured as inputs.  $V_{IL} = 0.2 \text{ V}$ ,  $V_{IH} = V_{DD} - 0.2 \text{ V}$ .

### **B.2 CONTROL TIMING**

The data in Table 10-5 and Table 10-6 of *MC68HC05J1A Technical Data* applies to the MC68HSC05J1A with the exceptions given in Table B-2 and Table B-3.

Table B-2. High-Speed Control Timing (V  $_{DD}$  = 5.0 V  $\pm$  10%)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal Oscillator <sup>1</sup> Ceramic Resonator External Clock	f <sub>osc</sub>		8.0 8.0 8.0	MHz
Internal Operating Frequency (f <sub>OSC</sub> ÷ 2) Crystal Oscillator <sup>(1)</sup> Ceramic Resonator External Clock	f <sub>OP</sub>	_ _ _	4.0 4.0 4.0	MHz
Cycle Time (1 ÷ f <sub>OP</sub> )	t <sub>CYC</sub>	250	_	ns
IRQ Pulse Width Low (Edge-Triggered)	t <sub>ILIL</sub>	63	_	ns
PA3-PA0 Interrupt Pulse Width (Edge-Triggered)	t <sub>IHIL</sub>	63	_	ns
OSC1 Pulse Width	t <sub>OH</sub> or t <sub>OL</sub>	45	_	ns

<sup>1.</sup> Use only AT-cut crystals.

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Table B-3. High-Speed Control Timing (V  $_{DD}$  = 3.3 V  $\pm\,10\%$ )

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal Oscillator <sup>1</sup> Ceramic Resonator External Clock	f <sub>osc</sub>	_ _ _	4.2 4.2 4.2	MHz
Internal Operating Frequency (f <sub>OSC</sub> ÷ 2) Crystal Oscillator <sup>(1)</sup> Ceramic Resonator External Clock	f <sub>OP</sub>	_ _ _	2.1 2.1 2.1	MHz
Cycle Time (1 ÷ f <sub>OP</sub> )	t <sub>CYC</sub>	480		ns
IRQ Pulse Width Low (Edge-Triggered)	t <sub>ILIL</sub>	125	_	ns
PA3-PA0 Interrupt Pulse Width (Edge-Triggered)	t <sub>IHIL</sub>	125	_	ns
OSC1 Pulse Width	t <sub>OH</sub> or t <sub>OL</sub>	90		ns

<sup>1.</sup> Use only AT-cut crystals.

### **B.3 MC ORDERING INFORMATION**

Table B-4 gives order numbers for the available package types.

**Table B-4. MC Order Numbers** 

Package Type	Temperature Range	Order Number
20-Pin Dual In-Line Package (DIP)	0 °C to 70 °C	MC68HSC05J1AP
20-Pin Small Outline Integrated Circuit (SOIC)	0 °C to 70 °C	MC68HSC05J1ADW

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