HC05C12AGRS/D
REV 2.0

68HC05C12A
68HCL05C12A
68HSC05C12A

SPECIFICATION
(General Release)

CSIC System Design Group
Austin, Texas

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SECTION 1
GENERAL DESCRIPTION

1.1 Introduction

The MC68HC05C12A is an enhanced version of the MC68HC05C12. It includes keyboard scanning logic, a high current pin, a COP watchdog timer, and read-only memory (ROM) security.

1.2 Features

- M68HC05 Core
- Single 3.0- to 5.5-Volt Supply
- Available Packages:
  - 40-Pin Dual In-Line (DIP)
  - 42-Pin Plastic Shrink Dual In-Line (SDIP)
  - 44-Lead Plastic Leaded Chip Carrier (PLCC)
  - 44-Lead Quad Flat Pack (QFP)
- On-Chip Oscillator for Crystal/Ceramic Resonator
- Fully Static Operation
- 12,096 Bytes of User ROM
- ROM Security Feature
- 176 Bytes of On-Chip Random-Access Memory (RAM)
- Asynchronous Serial Communications Interface (SCI) System
- Synchronous Serial Peripheral Interface (SPI) System
- 16-Bit Capture/Compare Timer System
- Computer Operating Properly (COP) Watchdog Timer
- 24 Bidirectional Input/Output (I/O) Lines
- Seven Input-Only Lines
- User Mode
- Self-Check Mode
- Power-Saving Stop and Wait Modes

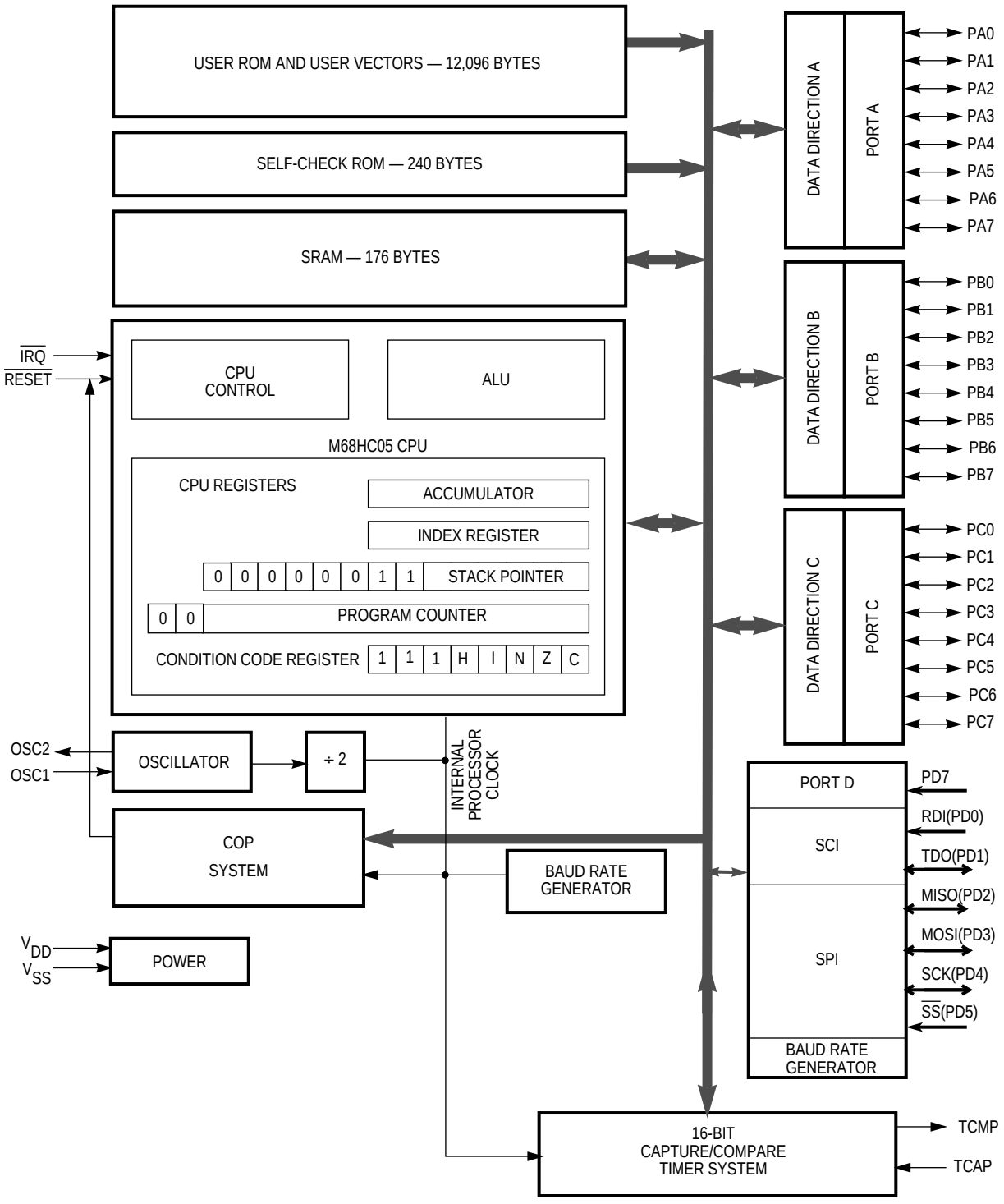


Figure 1-1. Block Diagram

- High Current Sink and Source on One Port Pin (PC7)
- Mask Selectable External Interrupt Sensitivity
- Mask-Programmable Keyscan Logic

1.3 Mask Options

Eight mask options are available to select the pullup/interrupts on port B on a pin-by-pin basis.

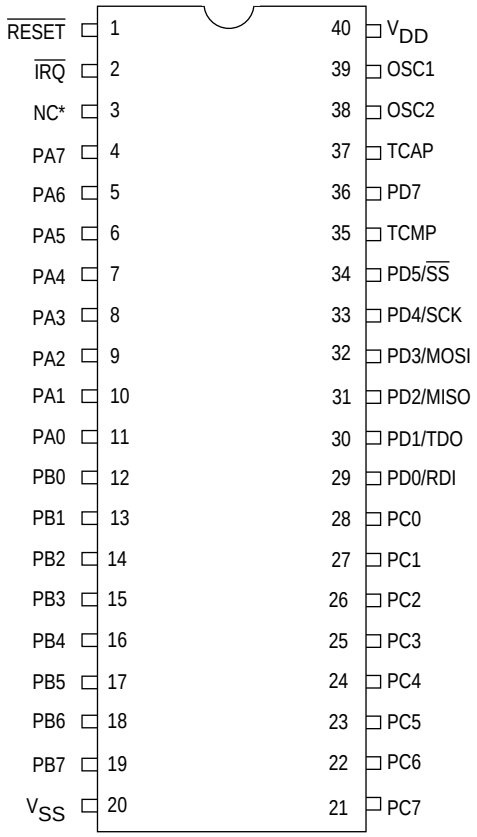
There are also four mask options for $\overline{\text{IRQ}}$ (edge-sensitive only or edge- and level-sensitive), CLOCK (crystal or RC), COP (enable or disable), and STOP (enable or disable).

1.4 Functional Pin Description

NOTE

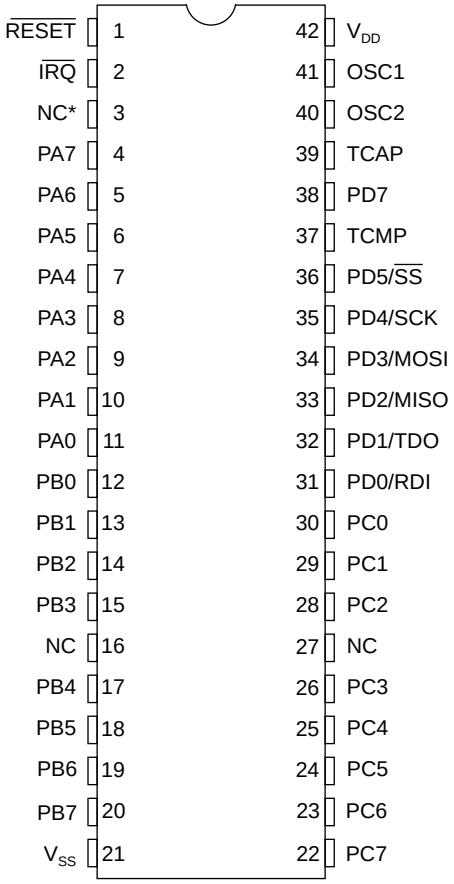
A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{\text{RESET}}$ is active low. Any reference to voltage, current, resistance, capacitance, time, or frequency specified in the following paragraphs will refer to the nominal values. The exact values and their tolerance or limits are specified in **SECTION 13 ELECTRICAL SPECIFICATIONS**.

The MC68HC05C12A is available in a 40-pin DIP (see Figure 1-2), 42-pin SDIP (see Figure 1-3), 44-pin PLCC (see Figure 1-4), and 44-pin QFP (see Figure 1-5). The following paragraphs describe the general function of each pin.



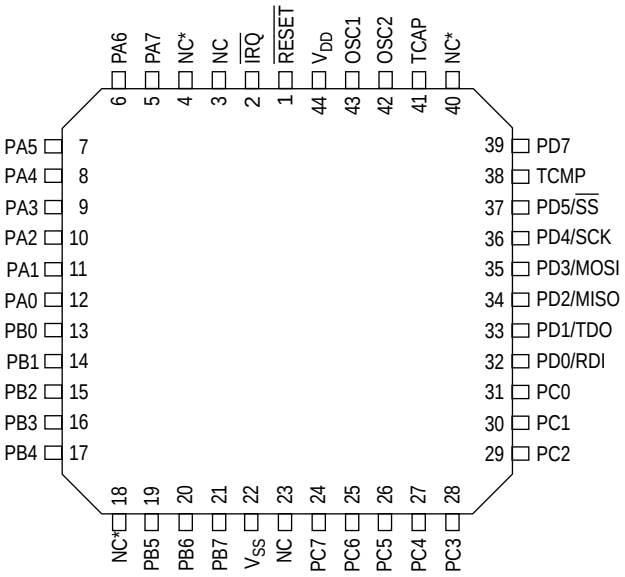
* If MC68HC705C9A OTPs are to be used in the same application, this pin should be tied to V_{DD}.

Figure 1-2. 40-Pin Dual In-Line Package



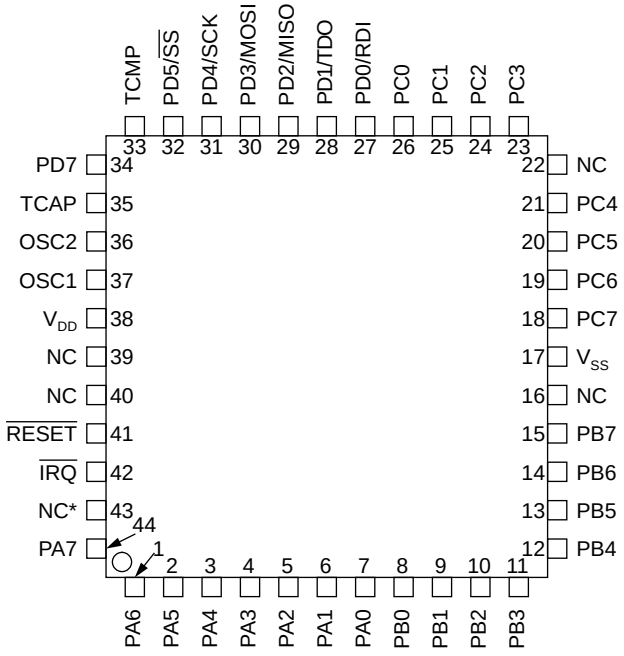
* If MC68HC705C9A OTPs are to be used in the same application, this pin should be tied to V_{DD}.

Figure 1-3. 42-Pin Plastic Shrink Dual In-Line Package



* If MC68HC705C9A OTPs are to be used in the same application, pin 4 should be tied to pin 44 (V_{DD}), pin 18 should be tied to pin 17 (PB4), and pin 40 should be tied to pin 39 (PD7).

Figure 1-4. 44-Lead Plastic Leaded Chip Carrier



* If MC68HC705C9A OTPs are to be used in the same application, this pin should be tied to V_{DD}.

Figure 1-5. 44-Lead Quad Flat Pack

1.4.1 V_{DD} and V_{SS}

Power is supplied to the microcontroller using these two pins. V_{DD} is the positive supply and V_{SS} is ground.

1.4.2 $\overline{\text{IRQ}}$

This pin has a mask selectable option that provides two different choices of interrupt triggering sensitivity. The $\overline{\text{IRQ}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to **SECTION 4 INTERRUPTS** for more detail.

1.4.3 OSC1 and OSC2

These pins provide control input for an on-chip clock oscillator circuit. A crystal, a ceramic resonator, a resistor/capacitor combination, or an external signal connects to these pins providing a system clock. The internal bus rate is one-half the external oscillator frequency.

1.4.4 $\overline{\text{RESET}}$

This active low pin is used to reset the MCU to a known startup state by pulling $\overline{\text{RESET}}$ low. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

1.4.5 TCAP

This pin controls the input capture feature for the on-chip programmable timer. The TCAP pin contains an internal Schmitt trigger as part of its input to improve noise immunity.

1.4.6 TCMP

The TCMP pin provides an output for the output compare feature of the on-chip timer subsystem.

1.4.7 Port A (PA0–PA7)

These eight I/O lines comprise port A. The state of any pin is software programmable and all port A lines are configured as input during power-on or reset. For detailed information on I/O programming, see **7.6 Input/Output Programming**.

1.4.8 Port B (PB0–PB7)

These eight I/O lines comprise port B. The state of any pin is software programmable, and all port B lines are configured as input during power-on or reset. Port B has mask option enabled pullup devices and interrupt capability by pin. The interrupts and pullups are enabled together. For a detailed description on I/O programming, refer to **7.6 Input/Output Programming**.

1.4.9 Port C (PC0–PC7)

These eight I/O lines comprise port C. The state of any pin is software programmable and all port C lines are configured as input during power-on or reset. PC7 has high current sink and source capability. For a detailed description on I/O programming, refer to **7.6 Input/Output Programming**.

1.4.10 Port D (PD0–PD5 and PD7)

These seven port lines comprise port D. PD7 and PD5–PD0 are input only. PD0 and PD1 are shared with the SCI subsystem and PD2–PD5 are shared with the SPI subsystem. For a detailed description on I/O programming, refer to **7.6 Input/Output Programming**.

SECTION 2
MEMORY

2.1 Introduction

The MC68HC05C12A has an 16-Kbyte memory map, consisting of user read-only memory (ROM), user random-access memory (RAM), self-check ROM, and input/output (I/O) registers. See Figure 2-1 and Figure 2-2.

2.2 Read-Only Memory (ROM)

The user ROM consists of 48 bytes of page zero ROM from $0020 to $004F, 12,032 bytes of ROM from $1000 to $3EFF and 16 bytes of user vectors from $3FF0 to $3FFF. The self-check ROM and vectors are located from $3F00 to $3FEF. See Figure 2-1.

Twelve of the user vectors, $3FF4 through $3FFF, are dedicated to user-defined reset and interrupt vectors. The remaining four bytes from $3FF0-$3FF3 are not used.

2.3 ROM Security Feature

A security feature has been incorporated into the MC68HC05C12A to help prevent external viewing of the ROM contents. This feature aids in keeping customer developed software proprietary.

2.4 Random-Access Memory (RAM)

The user RAM consists of 176 bytes and is used both for general-purpose RAM and stack area. See Figure 2-1. The stack begins at address $00FF. The stack pointer can access 64 bytes of RAM in the range $00FF to $00C0. See **3.2.4 Stack Pointer (SP)**.

NOTE

When developing ROM code for the MC68HC05C12A using the OTP MC68HC705C9A, set the OTP mask option register to configure the OTP as an MC68HC05C12A. This will limit the OTP to a memory map identical to the MC68HC05C12A.

NOTE

Using the stack area for data storage or temporary work locations requires care to prevent it from being overwritten due to stacking from an interrupt or subroutine call.

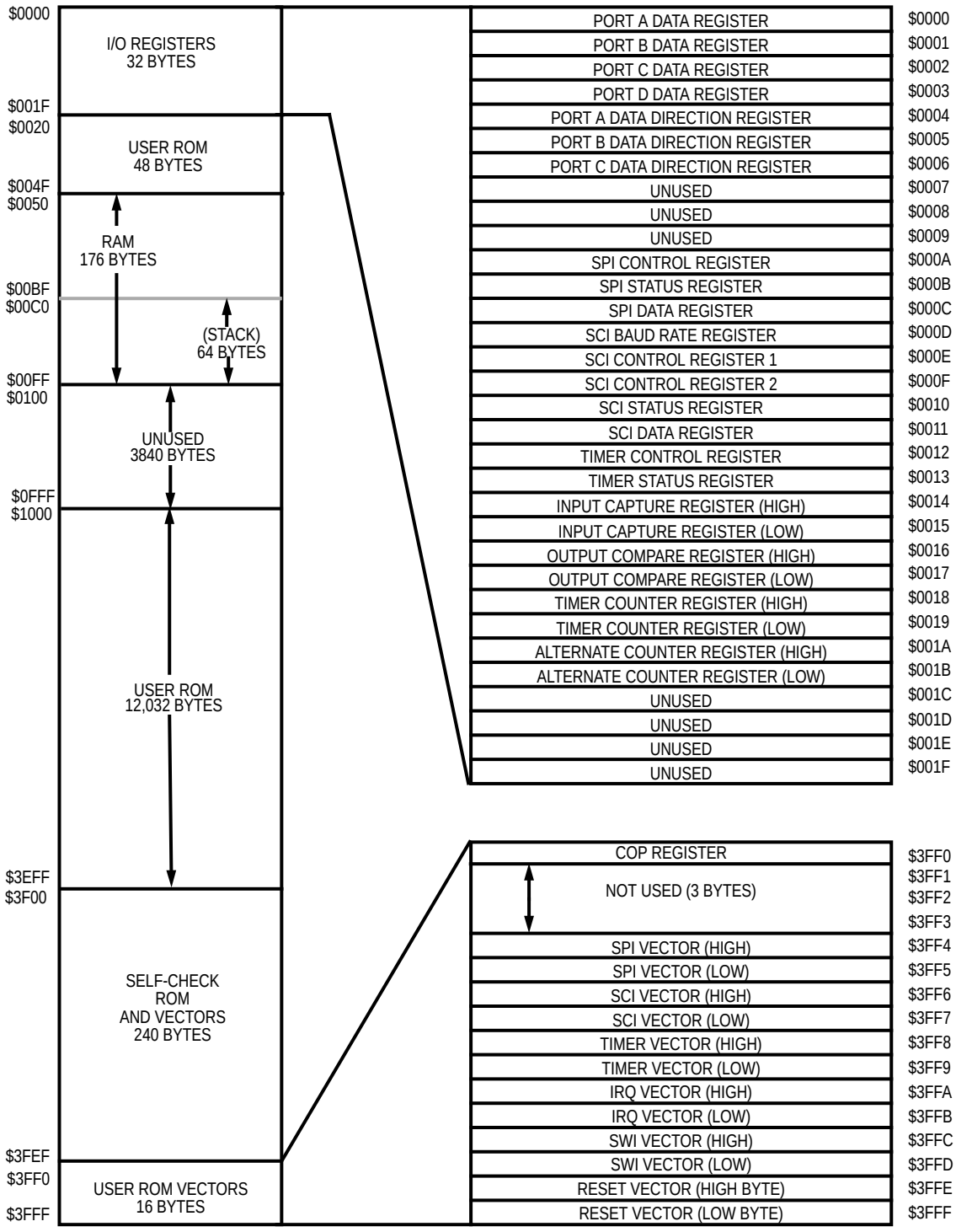


Figure 2-1. Memory Map

Addr.	Register	R/W	Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data PORTA	R	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		W								
$0001	Port B Data PORTB	R	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		W								
$0002	Port C Data PORTD	R	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		W								
$0003	Port D Data PORTD	R	PD7		PD5	PD4	PD3	PD2	PD1	PD0
		W								
$0004	Port A Data Direction DDRA	R	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		W								
$0005	Port B Data Direction DDRB	R	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		W								
$0006	Port C Data Direction DDRC	R	DDRC7	DDRC6	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		W								
$0007	Unimplemented	R								
		W								
$0008	Unimplemented	R								
		W								
$0009	Unimplemented	R								
		W								
$000A	SPI Control Register SPCR	R	SPIE	SPE		MSTR	CPOL	CPHA	SPR1	SPR0
		W								
$000B	SPI Status Register SPSR	R	SPIF	WCOL	0	MODF	0	0	0	0
		W								
$000C	SPI Data Register SPDR	R	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
		W								
$000D	SCI Baud Rate Register BAUD	R	0	0	SCP1	SCP0	0	SCR2	SCR1	SCR0
		W								
$000E	SCI Control 1 SCCR1	R	R8	T8	0	M	WAKE	0	0	0
		W								
$000F	SCI Control 2 SCCR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RMW	SBK
		W								

= Unimplemented

Figure 2-2. Input/Output Registers

Addr.	Register	R/W	Bit 7	6	5	4	3	2	1	Bit 0
$0010	SCI Status Register SCSR	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
		W								
$0011	SCI Data Register SCDAT	R	SCD7	SCD6	SCD5	SCD4	SCD3	SCD2	SCD1	SCD0
		W								
$0012	Timer Control Register TCR	R	ICIE	OCIE	TOIE	0	0	0	IEDGE	OLVL
		W								
$0013	Timer Status Register TSR	R	ICF	OCF	TOF	0	0	0	0	0
		W								
$0014	Input Capture Register ICR (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
$0015	Input Capture Register ICR (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
$0016	Output Compare Reg. OCR (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
$0017	Output Compare Reg. OCR (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
$0018	Timer Counter Register TCNT (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
$0019	Timer Counter Register TCNT (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
$001A	Alternate Counter Reg. ALTCNT (High)	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
$001B	Alternate Counter Reg. ALTCNT (Low)	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
$001C	Unimplemented	R								
		W								
$001D	Unimplemented	R								
		W								
$001E	Unimplemented	R								
		W								
$001F	Reserved	R	R	R	R	R	R	R	R	R
		W								

= Unimplemented R = Reserved

Figure 2-2. Input/Output Registers (Continued)

Addr.	Register	R/W	Bit 7	6	5	4	3	2	1	Bit 0
↓										↓
$3FF0	COP Reset	R	User ROM Data							
		W								COPC

= Unimplemented

Figure 2-2. Input/Output Registers (Continued)

SECTION 3
CPU REGISTERS

3.1 Introduction

This section describes the CPU registers.

3.2 CPU Registers

The five CPU registers are shown in Figure 3-1 and the interrupt stacking order in Figure 3-2.

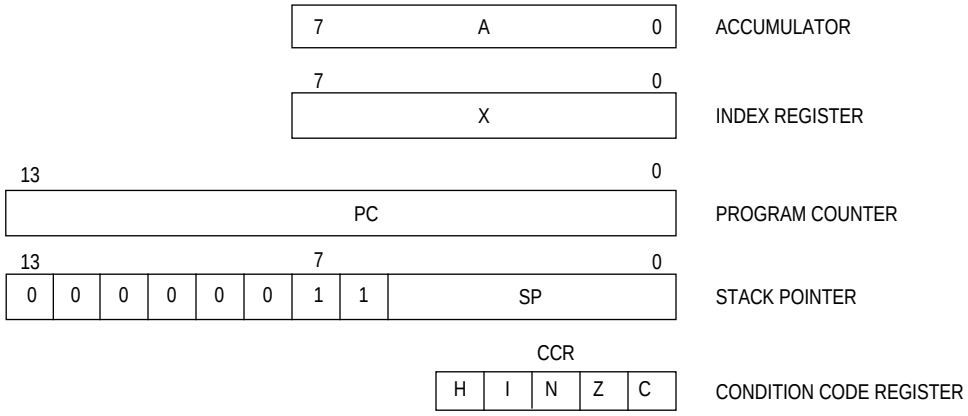
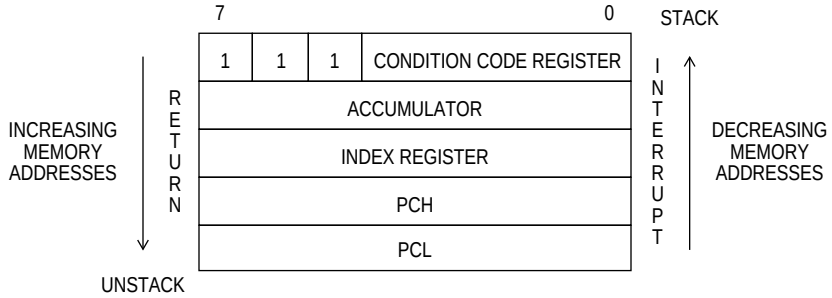


Figure 3-1. Programming Model



NOTE: Since the stack pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Figure 3-2. Stacking Order

3.2.1 Accumulator (A)

The accumulator shown in Figure 3-1 is a general-purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

3.2.2 Index Register (X)

The index register is an 8-bit register used by the indexed addressing value to create an effective address. The index register also may be used as a temporary storage area.

3.2.3 Program Counter (PC)

The program counter is a 14-bit register that contains the address of the next byte to be fetched.

3.2.4 Stack Pointer (SP)

The stack pointer contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the seven most significant bits are permanently set to 0000011. These eight bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and loses the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.

3.2.5 Condition Code Register (CCR)

The CCR is a 5-bit register in which four bits are used to indicate the results of the instruction just executed, and the fifth bit indicates whether interrupts are masked. These bits can be tested individually by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.

H — Half Carry

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

I — Interrupt

When this bit is set, the timer and external interrupt are masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and processed as soon as the interrupt bit is cleared.

N — Negative

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Z — Zero

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

C — Carry/Borrow

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit also is affected during bit test and branch instructions and during shifts and rotates.

SECTION 4
INTERRUPTS

4.1 Introduction

The MCU can be interrupted five different ways: the four maskable hardware interrupts ($\overline{\text{IRQ}}$, SPI, SCI, and timer) and the non-maskable software interrupt instruction (SWI). Port B interrupts, if enabled, are combined with the $\overline{\text{IRQ}}$ to form a single interrupt source.

Interrupts cause the processor to save register contents on the stack and to set the interrupt mask (I bit) to prevent additional interrupts. The RTI instruction causes the register contents to be recovered from the stack and normal processing to resume.

Unlike reset, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction is complete.

NOTE

The current instruction is the one already fetched and being operated on.

When the current instruction is complete, the processor checks all pending hardware interrupts. If interrupts are not masked (CCR I bit clear) and if the corresponding interrupt enable bit is set, the processor proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed the same as any other instruction, regardless of the I-bit state.

Vector addresses for all interrupts including reset are listed in Table 4-1.

Table 4-1. Vector Addresses for Interrupts and Reset

Register	Flag Name	Interrupts	CPU Interrupt	Vector Address
N/A	N/A	Reset	RESET	$3FFE–$3FFF
N/A	N/A	Software	SWI	$3FFC–$3FFD
N/A	N/A	External Interrupt	IRQ	$3FFA–$3FFB
TSR	ICF	Timer Input Capture	TIMER	$3FF8–$3FF9
TSR	OCF	Timer Output Compare	TIMER	$3FF8–$3FF9
TSR	TOF	Timer Overflow	TIMER	$3FF8–$3FF9
SCSR	TDRE	Transmit Buffer Empty	SCI	$3FF6–$3FF7
SCSR	TC	Transmit Complete	SCI	$3FF6–$3FF7
SCSR	RDRF	Receiver Buffer Full	SCI	$3FF6–$3FF7
SCSR	IDLE	Idle Line Detect	SCI	$3FF6–$3FF7
SCSR	OR	Overrun	SCI	$3FF6–$3FF7
SPSR	SPIF	Transfer Complete	SPI	$3FF4–$3FF5
SPSR	MODF	Mode Fault	SPI	$3FF4–$3FF5

4.2 Hardware Controlled Interrupt Sequence

The following three functions ($\overline{\text{RESET}}$, STOP, and WAIT) are not in the strictest sense interrupts; however, they are acted upon in a similar manner. Flowcharts for hardware interrupts are shown in Figure 4-1 and Figure 3-2. A discussion is provided below.

1. $\overline{\text{RESET}}$ — A low input on the $\overline{\text{RESET}}$ input pin causes the program to vector to its starting address which is specified by the contents of memory locations $3FFE and $3FFF. The I bit in the condition code register is also set. Much of the MCU is configured to a known state during this type of reset as previously described in **SECTION 5RESETS**.
2. STOP — The STOP instruction causes the oscillator to be turned off and the processor to “sleep” until an external interrupt ($\overline{\text{IRQ}}$) or reset occurs.
3. WAIT — The WAIT instruction causes all processor clocks to stop, but leaves the timer clock running. This “rest” state of the processor can be cleared by reset, an external interrupt ($\overline{\text{IRQ}}$), SPI, SCI, or timer interrupt. These individual interrupts have no special wait vectors.

4.3 Software Interrupt (SWI)

The SWI is an executable instruction and a non-maskable interrupt: It is executed regardless of the state of the I bit in the CCR. If the I bit is zero (interrupts enabled), SWI executes after interrupts which were pending when the SWI was fetched but before interrupts generated after the SWI was fetched. The interrupt service routine address is specified by the contents of memory locations $3FFC and $3FFD.

4.4 External Interrupt

If the interrupt mask bit (I bit) of the CCR is set, all maskable interrupts (internal and external) are disabled. Clearing the I bit enables interrupts. The interrupt request is latched immediately following the falling edge of $\overline{\text{IRQ}}$. It is then synchronized internally and serviced as specified by the contents of $3FFA and $3FFB.

When any of the port B pullups are enabled, that pin becomes an additional external interrupt source which is coupled to the $\overline{\text{IRQ}}$ pin logic. It follows the same edge/edge-level selection that the $\overline{\text{IRQ}}$ pin has. See **Figure 7-1. Port B Pullup Option**.

Either a level-sensitive and edge-sensitive trigger, or an edge-sensitive-only trigger operation is selectable by mask option.

NOTE

The internal interrupt latch is cleared in the first part of the interrupt service routine; therefore, one external interrupt pulse could be latched and serviced as soon as the I bit is cleared.

4.5 Timer Interrupt

Three different timer interrupt flags cause a timer interrupt whenever they are set and enabled. The interrupt flags are in the timer status register (TSR), and the enable bits are in the timer control register (TCR). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF8 and $3FF9.

4.6 SCI Interrupt

Five different SCI interrupt flags cause an SCI interrupt whenever they are set and enabled. The interrupt flags are in the SCI status register (SCSR), and the enable bits are in the SCI control register 2 (SCCR2). Any of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF6 and $3FF7.

4.7 SPI Interrupt

Two different SPI interrupt flags cause an SPI interrupt whenever they are set and enabled. The interrupt flags are in the SPI status register (SPSR), and the enable bits are in the SPI control register (SPCR). Either of these interrupts will vector to the same interrupt service routine, located at the address specified by the contents of memory locations $3FF4 and $3FF5.

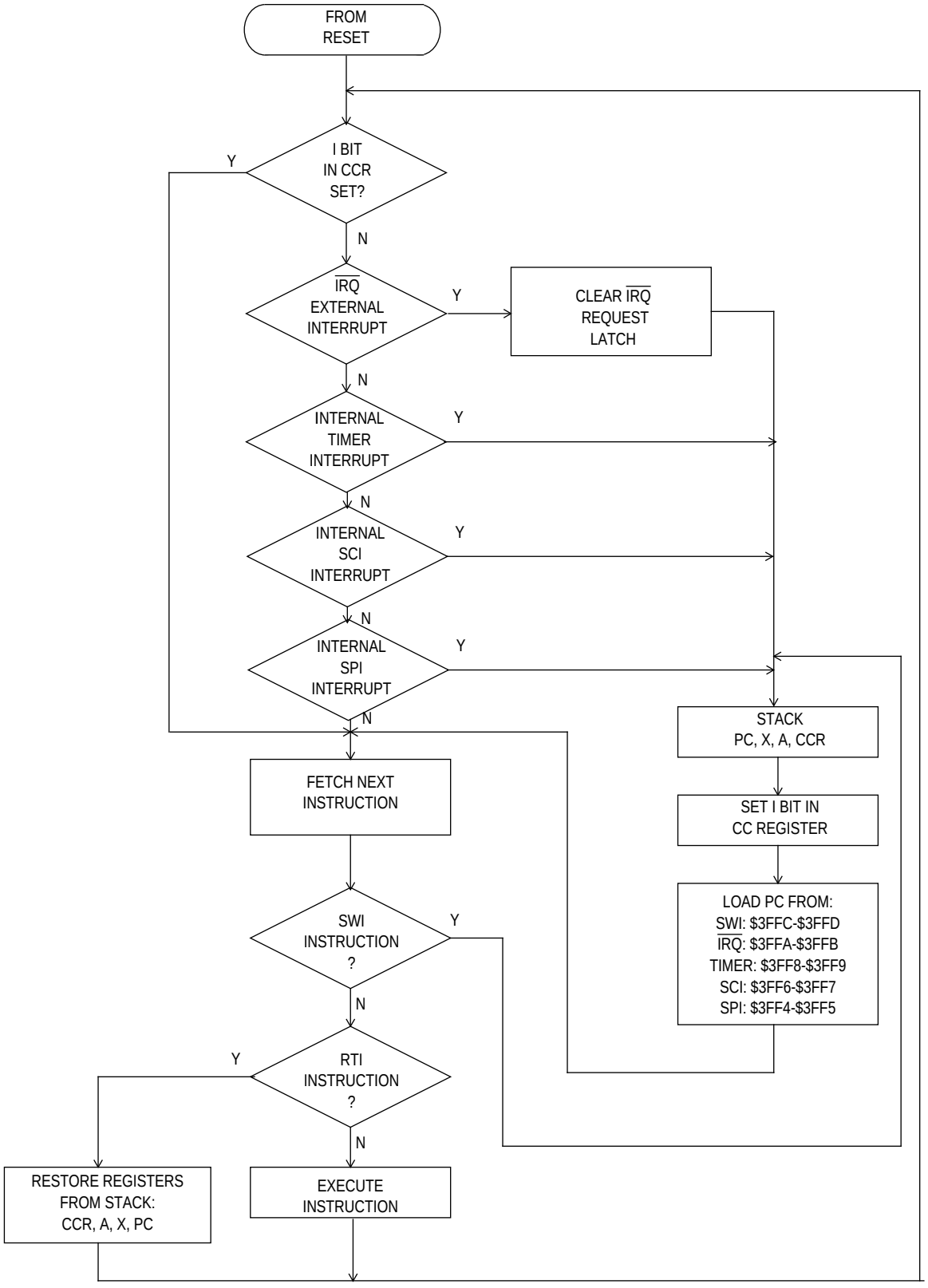


Figure 4-1. Interrupt Flowchart

SECTION 5
RESETS

5.1 Introduction

The MCU can be reset three ways: by the initial power-on reset function, by an active low input to the $\overline{\text{RESET}}$ pin, or by the computer operating properly (COP) reset.

5.2 Power-On Reset (POR)

An internal reset is generated on power-up to allow the internal clock generator to stabilize. The power-on reset is strictly for power turn-on conditions and should not be used to detect a drop in the power supply voltage. There is a 4064 internal processor clock cycle (t_{CYC}) oscillator stabilization delay after the oscillator becomes active. If the $\overline{\text{RESET}}$ pin is low after the end of this 4064-cycle delay, the MCU will remain in the reset condition until $\overline{\text{RESET}}$ goes high.

For additional information, refer to **Figure 13-8. Power-On Reset Timing Diagram**.

5.3 $\overline{\text{RESET}}$ Pin

The MCU is reset when a logic zero is applied to the $\overline{\text{RESET}}$ input for a period of one and one-half machine cycles (t_{RL}).

5.4 Computer Operating Properly (COP) Reset

This device includes a watchdog COP feature as a mask option. The COP is implemented with an 18-bit ripple counter. This provides a timeout period of 64 milliseconds at a bus rate of 2 MHz. If the COP should time out, a system reset will occur and the device will be re-initialized in the same fashion as a POR or external reset.

NOTE

When developing ROM code for the MC68HC05C12A using the OTP MC68HC05C9A, set the OTP mask option register to configure the OTP as an MC68HC05C12A. This will enable access to the MC68HC05C12A compatible COP and disable the COP which is NOT compatible with the MC68HC05C12A.

5.4.1 Resetting the COP

Preventing a COP reset is done by writing a logic zero to the COPC bit. This action will reset the counter and begin the timeout period again. The COPC bit is bit 0 of address $3FF0. A read of address $3FF0 will result in the user defined ROM data at that location.

5.4.2 COP During Wait Mode

The COP will continue to operate normally during wait mode. The software should pull the device out of wait mode periodically and reset the COP by writing to the COPC bit to prevent a COP reset.

5.4.3 COP During Stop Mode

Stop mode disables the oscillator circuit and thereby turns the clock off for the entire device. The COP counter will be reset when stop mode is entered. If a reset is used to exit stop mode, the COP counter will be reset after the 4064 cycles of delay after stop mode. If an interrupt is used to exit stop mode, the COP counter will not be reset after the 4064-cycle delay and will have that many cycles already counted when control is returned to the program.

5.4.4 COP During Self-Check Mode

The COP is disabled by hardware during self-check mode.

SECTION 6
LOW-POWER MODES

6.1 Introduction

This section describe the two low-power modes — stop and wait. Figure 6-1 shows the sequence of events caused by the STOP and WAIT instructions.

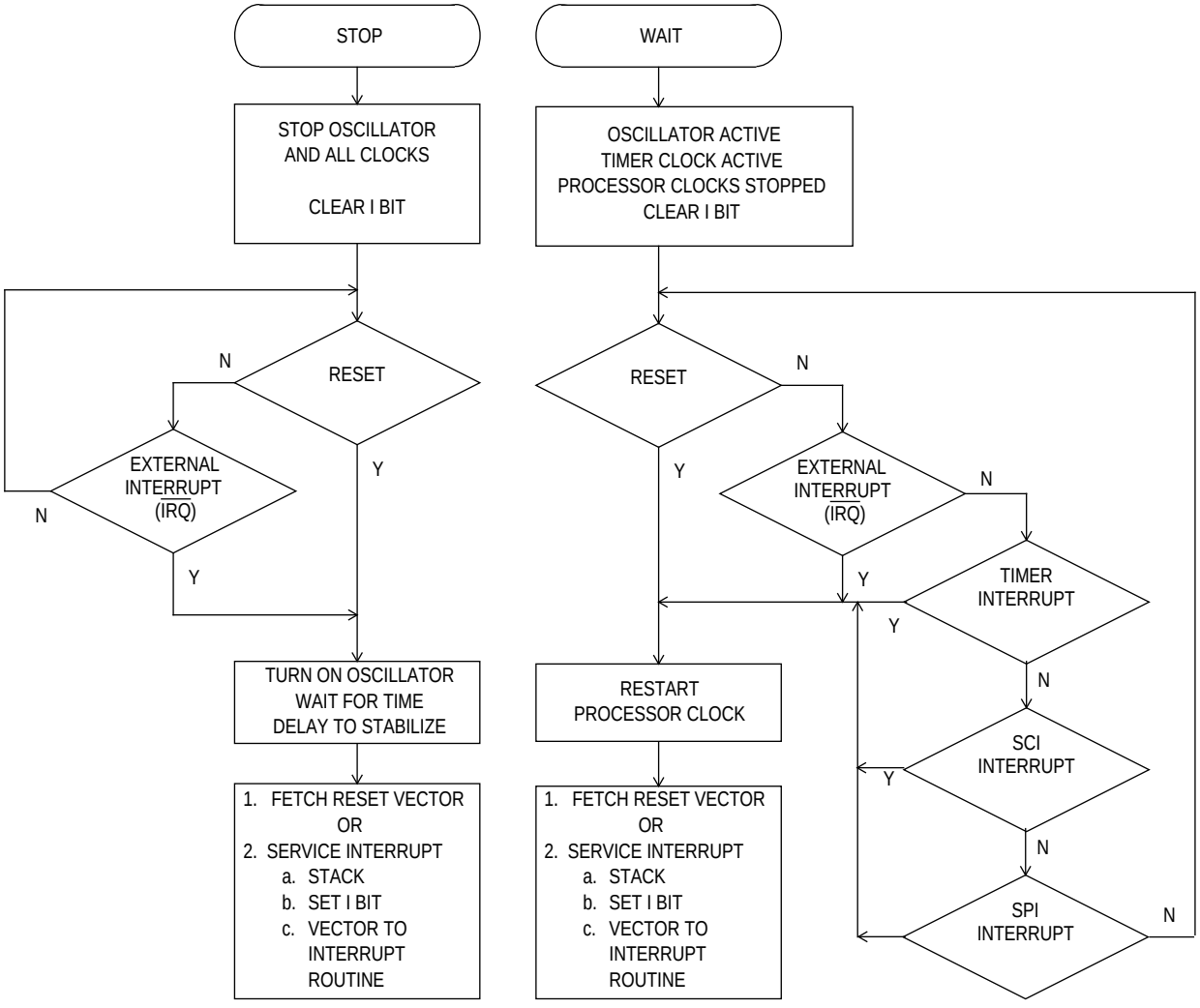


Figure 6-1. Stop/Wait Mode Flowchart

6.2 Stop Mode

The STOP instruction places the MCU in its lowest-power consumption mode. In stop mode, the internal oscillator is turned off, halting all internal processing, including timer operation.

During the stop mode, the TCR bits are altered to remove any pending timer interrupt request and to disable any further timer interrupts. The timer prescaler is cleared. The I bit in the condition code register is cleared to enable external interrupts. All other registers and memory remain unaltered. All input/output lines remain unchanged. The processor can be brought out of the stop mode only by an external interrupt or reset.

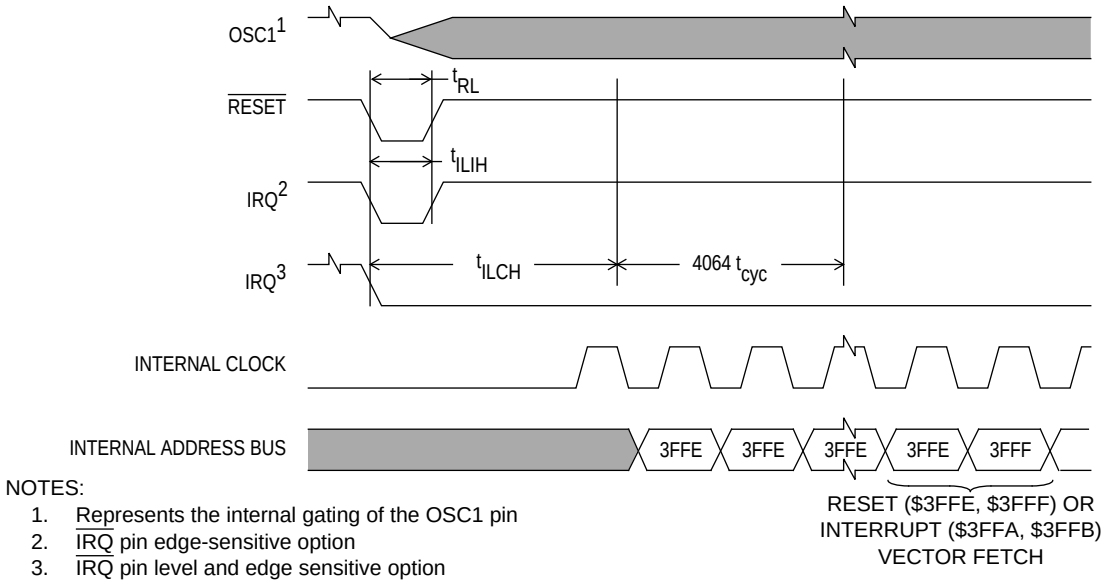
6.3 Stop Recovery

The processor can be brought out of the stop mode only by an external interrupt or $\overline{\text{RESET}}$. See Figure 6-2.

6.4 Wait Mode

The WAIT instruction places the MCU in a low-power consumption mode, but the wait mode consumes more power than the stop mode. All CPU action is suspended, but the timer, SCI, SPI, and the oscillator remain active. Any interrupt or reset will cause the MCU to exit the wait mode.

During the wait mode, the I bit in the CCR is cleared to enable interrupts. All other registers, memory, and input/output lines remain in their previous state. The timer may be enabled to allow a periodic exit from the wait mode.



NOTES:
1. $\overline{\text{RESET}}$ represents the internal gating of the OSC1 pin
2. $\overline{\text{IRQ}}$ pin edge-sensitive option
3. $\overline{\text{IRQ}}$ pin level and edge sensitive option

Figure 6-2. Stop Recovery Timing Diagram

SECTION 7
INPUT/OUTPUT PORTS

7.1 Introduction

The MC68HC05C12A has three 8-bit input/output (I/O) ports.These 24 port pins are programmable as either inputs or outputs under software control of the data direction registers. Port D does not have a data direction register, and its seven pins are input only with the exception of certain SCI/SPI functions.

NOTE

To avoid a glitch on the output pins, write data to the I/O port data register before writing a one to the corresponding data direction register.

7.2 Port A

Port A is an 8-bit bidirectional port which does not share any of its pins with other subsystems. The port A data register is at $0000 and the data direction register (DDR) is at $0004. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

7.3 Port B

Port B is an 8-bit bidirectional port. The port B data register is at $0001 and the data direction register (DDR) is at $0005. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port pin to output mode. Each of the port B pins has a mask programmable interrupt capability. This interrupt option also enables a pullup device when the pin is configured as an input (see Figure 7-1). The edge or edge and level sensitivity of the $\overline{\text{IRQ}}$ pin will also pertain to the enabled port B pins via mask options. Be careful when using port B pins that have the pullup enabled. Before switching from an output to an input, the data should be preconditioned to a one to prevent an interrupt from occurring.

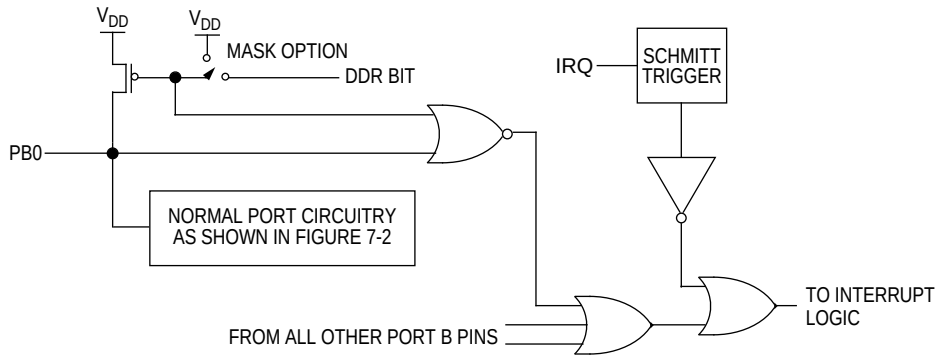


Figure 7-1. Port B Pullup Option

7.4 Port C

Port C is an 8-bit bidirectional port. The port C data register is at $0002 and the data direction register (DDR) is at $0006. Reset does not affect the data registers, but clears the data direction registers, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode. PC7 has a high current sink and source capability.

7.5 Port D

Port D is a 7-bit fixed input port. Four of its pins are shared with the SPI subsystem, two more are shared with the SCI subsystem. Reset does not affect the data registers. During reset, all seven bits become valid input ports because all special function output drivers associated with the SCI, timer, and SPI subsystems are disabled.

7.6 Input/Output Programming

I/O port pins may be programmed as inputs or outputs under software control. The direction of the pins is determined by the state of the corresponding bit in the port data direction register (DDR). Each I/O port has an associated DDR. Any I/O port pin is configured as an output if its corresponding DDR bit is set to a logic one. A pin is configured as an input if its corresponding DDR bit is cleared to a logic zero.

At power-on or reset, all DDRs are cleared, which configures all I/O pins as inputs. The data direction registers are capable of being written to or read by the processor. During the programmed output state, a read of the data register actually

reads the value of the output data latch and not the I/O pin. For further information, refer to Table 7-1 and Figure 7-2**.**

Table 7-1. I/O Pin Functions

R/$\overline{W}$*	DDR	I/O Pin Function
0	0	The I/O pin is in input mode. Data is written into the output data latch.
0	1	Data is written into the output data latch and output to the I/O pin.
1	0	The state of the I/O pin is read.
1	1	The I/O pin is in an output mode. The output data latch is read.

*R/$\overline{W}$ is an internal signal.

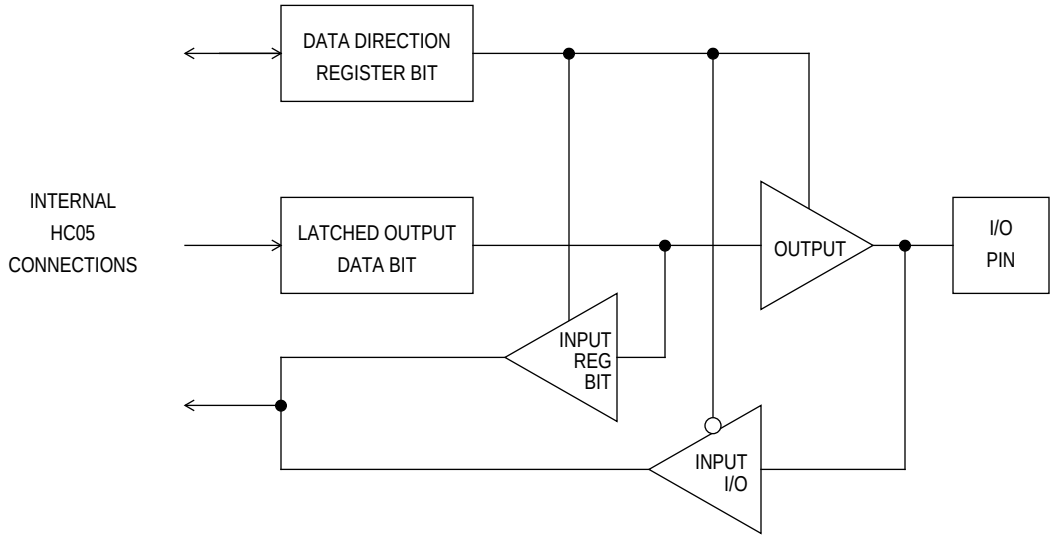


Figure 7-2. I/O Circuitry

SECTION 8
TIMER

8.1 Introduction

The timer consists of a 16-bit, software-programmable counter driven by a fixed divide-by-four prescaler. This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from several microseconds to many seconds. Refer to Figure 8-1 for a timer block diagram.

Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is also accessed.

NOTE

The I bit in the condition code register should be set while manipulating both the high and low byte register of a specific timer function to ensure that an interrupt does not occur.

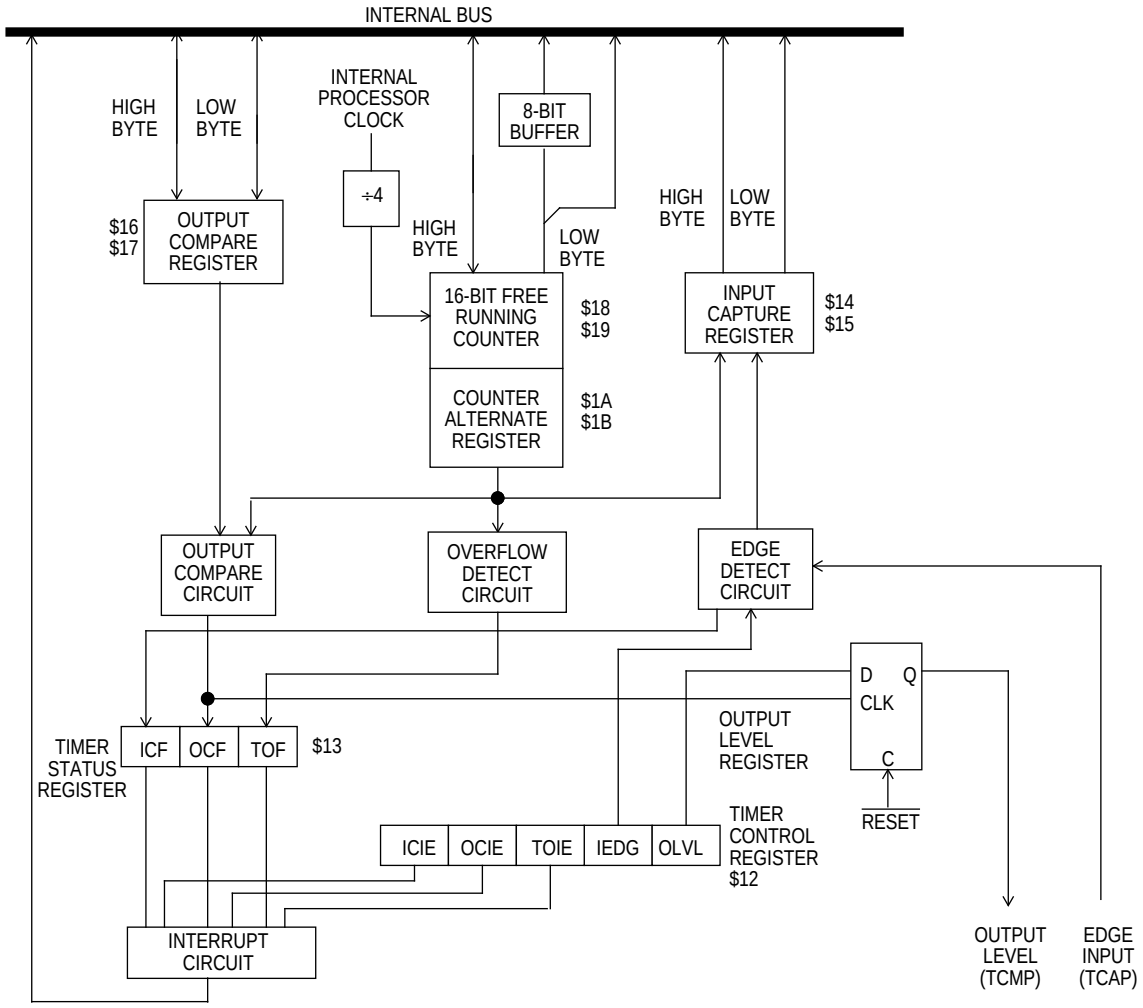


Figure 8-1. Timer Block Diagram

8.2 Counter

The key element in the programmable timer is a 16-bit, free-running counter or counter register, preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 2.0 microseconds if the internal bus clock is 2.0 MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

The double-byte, free-running counter can be read from either of two locations, $18-$19 (counter register) or $1A-$1B (counter alternate register). A read from only the least significant byte (LSB) of the free-running counter ($19, $1B) receives the count value at the time of the read. If a read of the free-running counter or counter alternate register first addresses the most significant byte (MSB) ($18, $1A), the LSB ($19, $1B) is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the user reads the MSB several times. This buffer is accessed when reading the free-running counter or counter alternate register LSB ($19 or $1B) and, thus, completes a read sequence of the total counter value. In reading either the free-running counter or counter alternate register, if the MSB is read, the LSB must also be read to complete the sequence.

The counter alternate register differs from the counter register in one respect: A read of the counter register MSB can clear the timer overflow flag (TOF). Therefore, the counter alternate register can be read at any time without the possibility of missing timer overflow interrupts due to clearing of the TOF.

The free-running counter is configured to $FFFC during reset and is always a read-only register. During a power-on reset, the counter is also preset to $FFFC and begins running after the oscillator start-up delay. Because the free-running counter is 16 bits preceded by a fixed divide-by-four prescaler, the value in the free-running counter repeats every 262,144 internal bus clock cycles. When the counter rolls over from $FFFF to $0000, the TOF bit is set. An interrupt can also be enabled whenever counter rollover occurs by setting its interrupt enable bit (TOIE).

8.3 Output Compare Register

The 16-bit output compare register is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The output compare register is used for several purposes, such as indicating when a period of time has elapsed. All bits are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

The output compare register contents are compared with the contents of the free-running counter continually, and if a match is found, the corresponding output compare flag (OCF) bit is set and the corresponding output level (OLVL) bit is clocked to an output level register. The output compare register values and the

output level bit should be changed after each successful comparison to establish a new elapsed timeout. An interrupt also can accompany a successful output compare provided the corresponding interrupt enable bit (OCIE) is set.

After a processor write cycle to the output compare register containing the MSB ($16), the output compare function is inhibited until the LSB ($17) is also written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare function. The free-running counter is updated every four internal bus clock cycles. The minimum time required to update the output compare register is a function of the program rather than the internal hardware.

The processor can write to either byte of the output compare register without affecting the other byte. The output level (OLVL) bit is clocked to the output level register regardless of whether the output compare flag (OCF) is set or clear.

8.4 Input Capture Register

Two 8-bit registers, which make up the 16-bit input capture register, are read-only and are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a defined transition. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register except when exiting stop mode.

The result obtained by an input capture will be one more than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles.

The free-running counter contents are transferred to the input capture register on each proper signal transition regardless of whether the input capture flag (ICF) is set or clear. The input capture register always contains the free-running counter value that corresponds to the most recent input capture.

After a read of the input capture register ($14) MSB, the counter transfer is inhibited until the LSB ($15) is also read. This characteristic causes the time used in the input capture software routine and its interaction with the main program to determine the minimum pulse period.

A read of the input capture register LSB ($15) does not inhibit the free-running counter transfer since they occur on opposite edges of the internal bus clock.

8.5 Timer Control Register (TCR)

The TCR is a read/write register containing five control bits. Three bits control interrupts associated with the timer status register flags ICF, OCF, and TOF.

		Bit 7	6	5	4	3	2	1	Bit 0
TCR $12	Read: / Write:	ICIE	OCIE	TOIE	0	0	0	IEDG	OLVL
	Reset:	0	0	0	0	0	0	U	0

U = Unaffected

Figure 8-2. Timer Control Register

ICIE — Input Capture Interrupt Enable
1 = Interrupt enabled
0 = Interrupt disabled

OCIE — Output Compare Interrupt Enable
1 = Interrupt enabled
0 = Interrupt disabled

TOIE — Timer Overflow Interrupt Enable
1 = Interrupt enabled
0 = Interrupt disabled

IEDG — Input Edge

Value of input edge determines which level transition on TCAP pin will trigger free-running counter transfer to the input capture register.
1 = Positive edge
0 = Negative edge

Reset does not affect the IEDG bit.

OLVL — Output Level

Value of output level is clocked into output level register by the next successful output compare and will appear on the TCMP pin.
1 = High output
0 = Low output

Bits 2, 3, and 4 —Not used

Always read zero

8.6 Timer Status Register (TSR)

The TSR is a read-only register containing three status flag bits.

		Bit 7	6	5	4	3	2	1	Bit 0
TSR $13	Read:	ICF	OCF	TOF	0	0	0	0	0
	Write:								
	Reset:	U	U	U	0	0	0	0	0

U = Unaffected

Figure 8-3. Timer Control Register

ICF — Input Capture Flag
- 1 = Flag set when selected polarity edge is sensed by input capture edge detector
- 0 = Flag cleared when TSR and input capture low register ($15) are accessed

OCF — Output Compare Flag
- 1 = Flag set when output compare register contents match the free-running counter contents
- 0 = Flag cleared when TSR and output compare low register ($17) are accessed

TOF — Timer Overflow Flag
- 1 = Flag set when free-running counter transition from $FFFF to $0000 occurs
- 0 = Flag cleared when TSR and counter low register ($19) are accessed

Bits 0-4 — Not used

Always read zero

Accessing the timer status register satisfies the first condition required to clear status bits. The remaining step is to access the register corresponding to the status bit.

A problem can occur when using the timer overflow function and reading the free-running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if:

1. The timer status register is read or written when TOF is set.
2. The LSB of the free-running counter is read but not for the purpose of servicing the flag.

The counter alternate register at addresses $1A and $1B contains the same value as the free-running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

8.7 Timer During Wait Mode

The CPU clock halts during the wait mode, the timer remains active. If interrupts are enabled, a timer interrupt will cause the processor to exit the wait mode.

8.8 Timer During Stop Mode

In the stop mode, the timer stops counting and holds the last count value if STOP is exited by an interrupt. If reset is used, the counter is forced to $FFFC. During stop, if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuit is armed. This does not set any timer flags or wake up the MCU. But if the MCU exits stop due to an external interrupt, there is an active input capture flag and data from the first valid edge that occurred during the stop mode. If reset is used to exit stop mode, then no input capture flag or data remains, even if a valid input capture edge occurred.

SECTION 9
SERIAL COMMUNICATIONS INTERFACE

9.1 Introduction

The serial communications interface (SCI) module allows high-speed asynchronous communication with peripheral devices and other MCUs.

9.2 Features

Features of the SCI module include:

- Standard Mark/Space Non-Return-to-Zero Format
- Full Duplex Operation
- 32 Programmable Baud Rates
- Programmable 8-Bit or 9-Bit Character Length
- Separately Enabled Transmitter and Receiver
- Two Receiver Wakeup Methods:
  - Idle Line Wakeup
  - Address Mark Wakeup
- Interrupt-Driven Operation Capability with Five Interrupt Flags:
  - Transmitter Data Register Empty
  - Transmission Complete
  - Receiver Data Register Full
  - Receiver Overrun
  - Idle Receiver Input
- Receiver Framing Error Detection
- 1/16 Bit-Time Noise Detection

9.3 SCI Data Format

The SCI uses the standard non-return-to-zero mark/space data format illustrated in Figure 9-1.

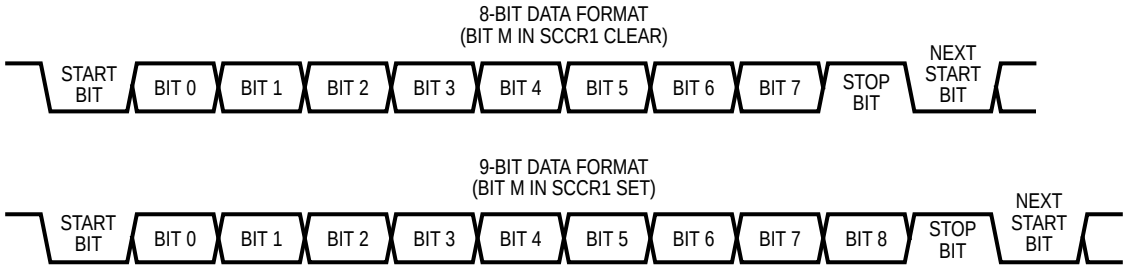


Figure 9-1. SCI Data Format

9.4 SCI Operation

The SCI allows full-duplex, asynchronous, RS232 or RS422 serial communication between the MCU and remote devices, including other MCUs. The SCI's transmitter and receiver operate independently, although they use the same baud-rate generator. The following paragraphs describe the operation of the SCI transmitter and receiver.

9.4.1 Transmitter

Figure 9-2 shows the structure of the SCI transmitter.

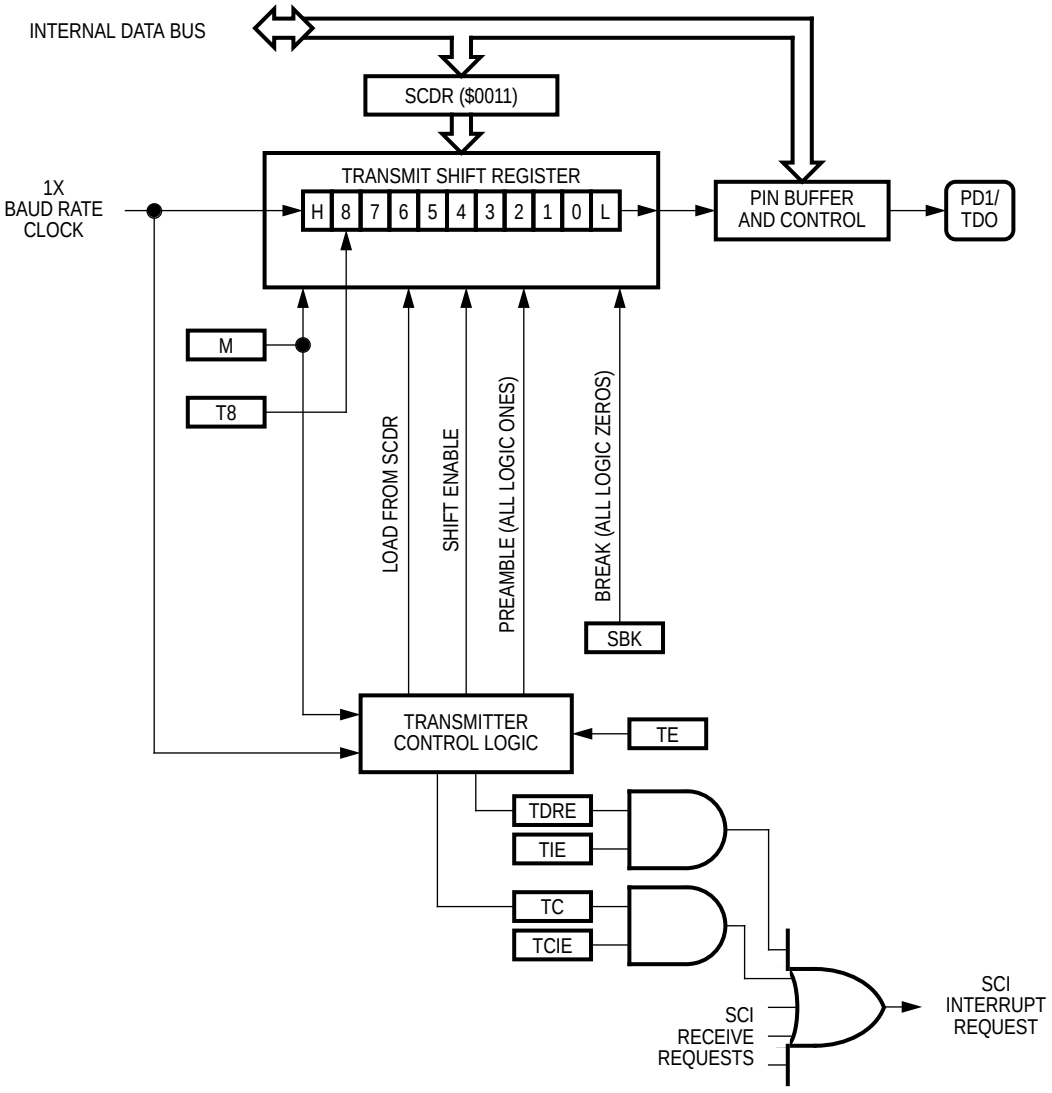
Character Length

The transmitter can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCCR1) determines character length. When transmitting 9-bit data, bit T8 in SCCR1 is the ninth bit (bit 8).

Character Transmission

During transmission, the transmit shift register shifts a character out to the PD1/TDO pin. The SCI data register (SCDR) is the write-only buffer between the internal data bus and the transmit shift register.

Writing a logic one to the TE bit in SCI control register 2 (SCCR2) and then writing data to the SCDR begins the transmission. At the start of a transmission, transmitter control logic automatically loads the transmit shift register with a preamble of logic ones. After the preamble shifts out, the control logic transfers the SCDR data into the shift register. A logic zero start bit automatically goes into the least significant bit position of the shift register, and a logic one stop bit goes into the most significant bit position.



	BIT 7	6	5	4	3	2	1	BIT 0	
BAUD RATE REGISTER (BAUD)	0	0	SCP1	SCP0	0	SCR2	SCR1	SCR0	$000D
SCI CONTROL REGISTER 1 (SCCR1)	R8	T8	0	M	WAKE	0	0	0	$000E
SCI CONTROL REGISTER 2 (SCCR2)	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	$000F
SCI STATUS REGISTER (SCSR)	TDRE	TC	RDRF	IDLR	OR	NF	FE	0	$0010
SCI DATA REGISTER (SCDR)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	$0011

Figure 9-2. SCI Transmitter

When the data in the SCDR transfers to the transmit shift register, the transmit data register empty (TDRE) flag in the SCI status register (SCSR) becomes set. The TDRE flag indicates that the SCDR can accept new data from the internal data bus.

When the shift register is not transmitting a character, the PD1/TDO pin goes to the idle condition, logic one. If software clears the TE bit during the idle condition, and while TDRE is set, the transmitter relinquishes control of the PD1/TDO pin.

Break Characters

Writing a logic one to the SBK bit in SCCR2 loads the shift register with a break character. A break character contains all logic zeros and has no start and stop bits. Break character length depends on the M bit in SCCR1. As long as SBK is at logic one, transmitter logic continuously loads break characters into the shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic one. The automatic logic one at the end of a break character is to guarantee the recognition of the start bit of the next character.

Idle Characters

An idle character contains all logic ones and has no start or stop bits. Idle character length depends on the M bit in SCCR1. The preamble is a synchronizing idle character that begins every transmission.

Clearing the TE bit during a transmission relinquishes the PD1/TDO pin after the last character to be transmitted is shifted out. The last character may already be in the shift register, or waiting in the SCDR, or in a break character generated by writing to the SBK bit. Toggling TE from logic zero to logic one while the last character is in transmission generates an idle character (a preamble) that allows the receiver to maintain control of the PD1/TDO pin.

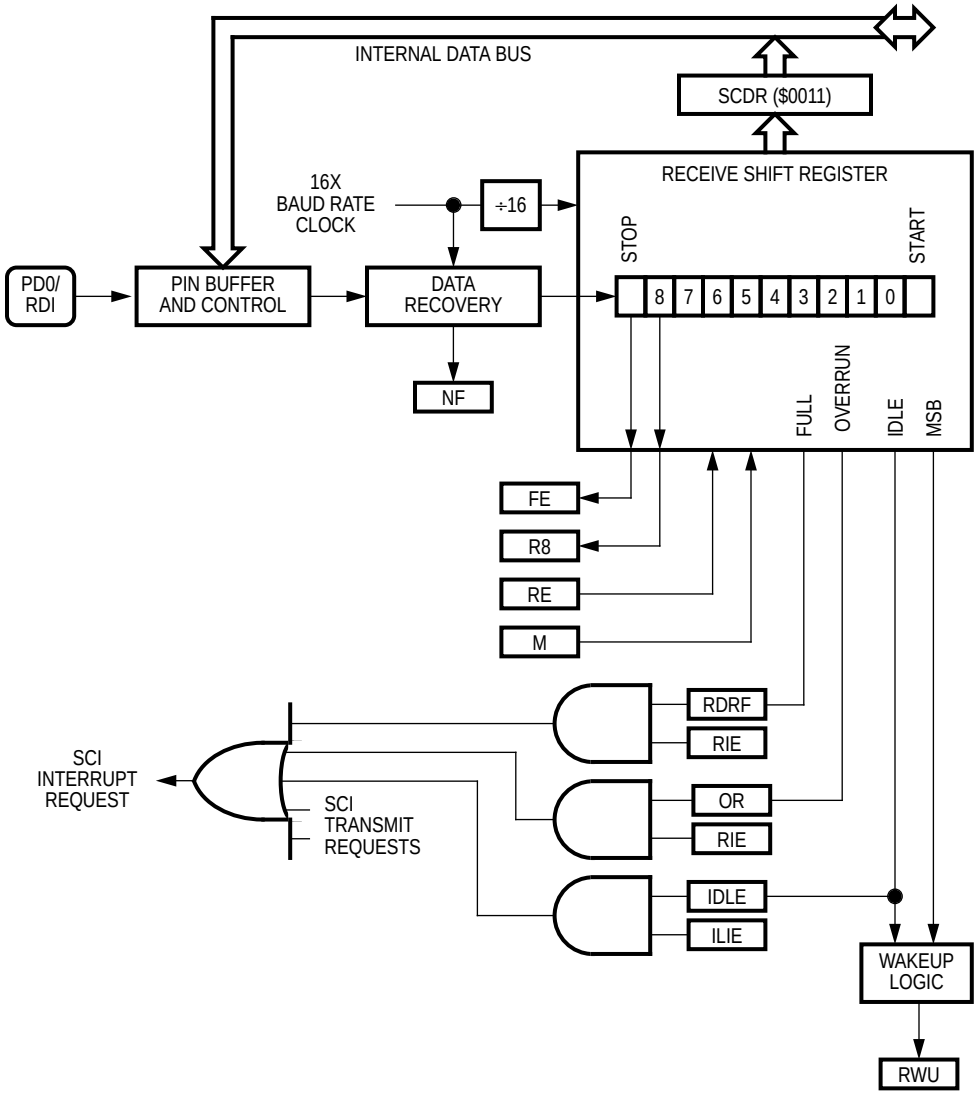
Transmitter Interrupts

Two sources can generate SCI transmitter interrupt requests:

- Transmit Data Register Empty (TDRE) — The TDRE bit in the SCSR indicates that the SCDR has transferred a character to the transmit shift register. TDRE is a source of SCI interrupt requests. The transmission complete interrupt enable bit (TCIE) in SCCR2 is the local mask for TDRE interrupts.
- Transmission Complete (TC) — The TC bit in the SCSR indicates that both the transmit shift register and the SCDR are empty and that no break or idle character has been generated. TC is a source of SCI interrupt requests. The transmission complete interrupt enable bit (TCIE) in SCCR2 is the local mask for TC interrupts.

9.4.2 Receiver

Figure 9-3 shows the structure of the SCI receiver.



	BIT 7	6	5	4	3	2	1	BIT 0	
BAUD RATE REGISTER (BAUD)	0	0	SCP1	SCP0	0	SCR2	SCR1	SCR0	$000D
SCI CONTROL REGISTER 1 (SCCR1)	R8	T8	0	M	WAKE	0	0	0	$000E
SCI CONTROL REGISTER 2 (SCCR2)	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK	$000F
SCI STATUS REGISTER (SCSR)	TDRE	TC	RDRF	IDLR	OR	NF	FE	0	$0010
SCI DATA REGISTER (SCDR)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	$0011

Figure 9-3. SCI Receiver

Character Length

The receiver can accommodate either 8-bit or 9-bit data. The state of the M bit in SCI control register 1 (SCCR1) determines character length. When receiving 9-bit data, bit R8 in SCCR1 is the ninth bit (bit 8).

Character Reception

During reception, the receive shift register shifts characters in from the PD0/RDI pin. The SCI data register (SCDR) is the read-only buffer between the internal data bus and the receive shift register.

After a complete character shifts into the receive shift register, the data portion of the character is transferred to the SCDR, setting the receive data register full (RDRF) flag. The RDRF flag can be used to generate an interrupt.

Receiver Wakeup

So that the MCU can ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup enable (RWU) bit in SCI control register 2 (SCCR2) puts the receiver into a standby state during which receiver interrupts are disabled.

Either of two conditions on the PD0/RDI pin can bring the receiver out of the standby state:

1. Idle input line condition — If the PD0/RDI pin is at logic one long enough for 10 or 11 logic ones to shift into the receive shift register, receiver interrupts are again enabled.
2. Address mark — If a logic one occurs in the most significant bit position of a received character, receiver interrupts are again enabled.

The state of the WAKE bit in SCCR1 determines which of the two conditions wakes up the MCU.

Receiver Noise Immunity

The data recovery logic samples each bit 16 times to identify and verify the start bit and to detect noise. Any conflict between noise-detection samples sets the noise flag (NF) in the SCSR. The NF bit is set at the same time that the RDRF bit is set.

Framing Errors

If the data recovery logic does not detect a logic one where the stop bit should be in an incoming character, it sets the framing error (FE) bit in the SCSR. The FE bit is set at the same time that the RDRF bit is set.

Receiver Interrupts

Three sources can generate SCI receiver interrupt requests:

1. Receive Data Register Full (RDRF) — The RDRF bit in the SCSR indicates that the receive shift register has transferred a character to the SCDR.
2. Receiver Overrun (OR) — The OR bit in the SCSR indicates that the receive shift register shifted in a new character before the previous character was read from the SCDR.
3. Idle Input (IDLE) — The IDLE bit in the SCSR indicates that 10 or 11 consecutive logic ones shifted in from the PD0/RDI pin.

9.5 SCI I/O Registers

These following I/O registers control and monitor SCI operation:

- SCI data register (SCDR)
- SCI control register 1 (SCCR1)
- SCI control register 2 (SCCR2)
- SCI status register (SCSR)

9.5.1 SCI Data Register (SCDR)

The SCI data register is the buffer for characters received and for characters transmitted.

		Bit 7	6	5	4	3	2	1	Bit 0
SCDR $0011	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Write:								
	Reset:	Unaffected by reset							

Figure 9-4. SCI Data Register

9.5.2 SCI Control Register 1 (SCCR1)

SCI control register 1 has the following functions:

- Stores ninth SCI data bit received and ninth SCI data bit transmitted
- Controls SCI character length
- Controls SCI wakeup method

		Bit 7	6	5	4	3	2	1	Bit 0
SCCR1 $000E	Read:	R8	T8	0	M	WAKE	0	0	0
	Write:								
	Reset:	Unaffected by reset							

Figure 9-5. SCI Control Register 1

R8 — Bit 8 (Received)

When the SCI is receiving 9-bit characters, R8 is the ninth bit of the received character. R8 receives the ninth bit from the receive shift register at the same time that the SCDR receives the other eight bits. Reset has no effect on the R8 bit.

T8 — Bit 8 (Transmitted)

When the SCI is transmitting 9-bit characters, T8 is the ninth bit of the transmitted character. T8 is loaded into the transmit shift register at the same time that SCDR is loaded into the transmit shift register. Reset has no effect on the T8 bit.

M — Character Length

This read/write bit determines whether SCI characters are 8 bits long or 9 bits long. The ninth bit can be used as an extra stop bit, as a receiver wakeup signal, or as a mark or space parity bit. Reset has no effect on the M bit.

1 = 9-bit SCI characters
0 = 8-bit SCI characters

WAKE — Wakeup Bit

This read/write bit determines which condition wakes up the SCI: a logic one (address mark) in the most significant bit position of a received character or an idle condition of the PD0/RDI pin. Reset has no effect on the WAKE bit.

1 = Address mark wakeup
0 = Idle line wakeup

9.5.3 SCI Control Register 2 (SCCR2)

SCI control register 2 has the following functions:

- Enables the SCI receiver and SCI receiver interrupts
- Enables the SCI transmitter and SCI transmitter interrupts
- Enables SCI receiver idle interrupts
- Enables SCI transmission complete interrupts
- Enables SCI wakeup
- Transmits SCI break characters

		Bit 7	6	5	4	3	2	1	Bit 0
SCCR2 $000F	Read: / Write:	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
	Reset:	0	0	0	0	0	0	0	0

Figure 9-6. SCI Control Register 2

TIE — Transmit Interrupt Enable

This read/write bit enables SCI interrupt requests when the TDRE bit becomes set. Reset clears the TIE bit.

1 = TDRE interrupt requests enabled
0 = TDRE interrupt requests disabled

TCIE — Transmission Complete Interrupt Enable

This read/write bit enables SCI interrupt requests when the TC bit becomes set. Reset clears the TCIE bit

1 = TC interrupt requests enabled
0 = TC interrupt requests disabled

RIE — Receive Interrupt Enable

This read/write bit enables SCI interrupt requests when the RDRF bit or the OR bit becomes set. Reset clears the RIE bit.

1 = RDRF interrupt requests enabled
0 = RDRF interrupt requests disabled

ILIE — Idle Line Interrupt Enable

This read/write bit enables SCI interrupt requests when the IDLE bit becomes set. Reset clears the ILIE bit.

1 = IDLE interrupt requests enabled
0 = IDLE interrupt requests disabled

TE — Transmit Enable

Setting this read/write bit begins the transmission by sending a preamble of 10 or 11 logic ones from the transmit shift register to the PD1/TDO pin. Reset clears the TE bit.

1 = Transmission enabled
0 = Transmission disabled

RE — Receive Enable

Setting this read/write bit enables the receiver. Clearing the RE bit disables the receiver and receiver interrupts but does not affect the receiver interrupt flags. Reset clears the RE bit.

1 = Receiver enabled
0 = Receiver disabled

RWU — Receiver Wakeup Enable

This read/write bit puts the receiver in a standby state. Typically, data transmitted to the receiver clears the RWU bit and returns the receiver to normal operation. The WAKE bit in SCCR1 determines whether an idle input or an address mark brings the receiver out of the standby state. Reset clears the RWU bit.

1 = Standby state
0 = Normal operation

SBK — Send Break

Setting this read/write bit continuously transmits break codes in the form of 10-bit or 11-bit groups of logic zeros. Clearing the SBK bit stops the break codes and transmits a logic one as a start bit. Reset clears the SBK bit.

1 = Break codes being transmitted
0 = No break codes being transmitted

9.5.4 SCI Status Register (SCSR)

The SCI status register contains flags to signal the following conditions:

- Transfer of SCDR data to transmit shift register complete
- Transmission complete
- Transfer of receive shift register data to SCDR complete
- Receiver input idle
- Receiver overrun
- Noisy data
- Framing error

		Bit 7	6	5	4	3	2	1	Bit 0
SCSR $0010	Read:	TDRE	TC	RDRF	IDLE	OR	NF	FE	0
	Write:								
	Reset:	1	1	0	0	0	0	0	0

Figure 9-7. SCI Control Register 2

TDRE — Transmit Data Register Empty

This clearable, read-only bit is set when the data in the SCDR transfers to the transmit shift register. TDRE generates an interrupt request if the TIE bit in SCCR2 is also set. Clear the TDRE bit by reading the SCSR with TDRE set, and then writing to the SCDR. Reset sets the TDRE bit. Software must initialize the TDRE bit to logic zero to avoid an instant interrupt request when turning on the transmitter.

1 = SCDR data transferred to transmit shift register
0 = SCDR data not transferred to transmit shift register

TC — Transmission Complete

This clearable, read-only bit is set when the TDRE bit is set, and no data, preamble, or break character is being transmitted. TC generates an interrupt request if the TCIE bit in SCCR2 is also set. Clear the TC bit by reading the SCSR with TC set, and then writing to the SCDR. Reset sets the TC bit. Software must initialize the TC bit to logic zero to avoid an instant interrupt request when turning on the transmitter.

1 = No transmission in progress
0 = Transmission in progress

RDRF — Receive Data Register Full

This clearable, read-only bit is set when the data in the receive shift register transfers to the SCI data register. RDRF generates an interrupt request if the RIE bit in SCCR2 is also set. Clear the RDRF bit by reading the SCSR with RDRF set, and then reading the SCDR. Reset clears the RDRF bit.

1 = Received data available in SCDR
0 = Received data not available in SCDR

IDLE — Receiver Idle

This clearable, read-only bit is set when 10 or 11 consecutive logic ones appear on the receiver input. IDLE generates an interrupt request if the ILIE bit in SCCR2 is also set. Clear the IDLE bit by reading the SCSR with IDLE set, and then reading the SCDR. Reset clears the IDLE bit.

1 = Receiver input idle
0 = Receiver input not idle

OR — Receiver Overrun

This clearable, read-only bit is set if the SCDR is not read before the receive shift register receives the next word. OR generates an interrupt request if the RIE bit in SCCR2 is also set. The data in the shift register is lost, but the data already in the SCDR is not affected. Clear the OR bit by reading the SCSR with OR set and then reading the SCDR. Reset clears the OR bit.

1 = Receiver shift register full and RDRF = 1
0 = No receiver overrun

NF — Receiver Noise Flag

This clearable, read-only bit is set when noise is detected in data received in the SCI data register. Clear the NF bit by reading the SCSR and then reading the SCDR. Reset clears the NF bit.

1 = Noise detected in SCDR
0 = No noise detected in SCDR

FE — Receiver Framing Error

This clearable, read-only flag is set when there is a logic zero where a stop bit should be in the character shifted into the receive shift register. If the received word causes both a framing error and an overrun error, the OR bit is set and the FE bit is not set. Clear the FE bit by reading the SCSR, and then reading the SCDR. Reset clears the FE bit.

1 = Framing error
0 = No framing error

9.5.5 Baud Rate Register (BAUD)

The baud rate register selects the baud rate for both the receiver and the transmitter.

		Bit 7	6	5	4	3	2	1	Bit 0
BAUD $000D	Read:	0	0	SCP1	SCP0	0	SCR2	SCR2	SCR0
	Write:								
	Reset:	0	0	0	0	0	U	U	U

U = Unaffected

Figure 9-8. Baud Rate Register

SCP1 and SCP0 — SCI Prescaler Select Bits

These read/write bits control prescaling of the baud rate generator clock, as shown in Table 9-1. Resets clear both SCP1 and SCP0.

Table 9-1. Baud Rate Generator Clock Prescaling

SCP[0:1]	Baud Rate Generator Clock
00	Internal Clock divided by 1
01	Internal Clock divided by 3
10	Internal Clock divided by 4
11	Internal Clock divided by 13

SCR2–SCR0 — SCI Baud Rate Select Bits

These read/write bits select the SCI baud rate, as shown in Table 9-2. Reset has no effect on the SCR2–SCR0 bits.

Table 9-2. Baud Rate Selection

SCR[2:1:0]	SCI Baud Rate (Baud)
000	Prescaled Clock divided by 1
001	Prescaled Clock divided by 2
010	Prescaled Clock divided by 4
011	Prescaled Clock divided by 8
100	Prescaled Clock divided by 16
101	Prescaled Clock divided by 32
110	Prescaled Clock divided by 64
111	Prescaled Clock divided by 128

Table 9-3 shows all possible SCI baud rates derived from crystal frequencies of 2 MHz, 4 MHz, and 4.194304 MHz.

Table 9-3. Baud Rate Selection Examples

SCP[1:0]	SCR[2:1:0]	SCI Baud Rate		
		f_{osc} = 2 MHZ	f_{osc} = 4 MHZ	f_{osc} = 4.194304 MHZ
00	000	62.50 kbaud	125 kbaud	131.1 kbaud
00	001	31.25 kbaud	62.50 kbaud	65.54 kbaud
00	010	15.63 kbaud	31.25 kbaud	32.77 kbaud
00	011	7813 Baud	15.63 kbaud	16.38 kbaud
00	100	3906 Baud	7813 Baud	8192 Baud
00	101	1953 Baud	3906 Baud	4096 Baud
00	110	976.6 Baud	1953 Baud	2048 Baud
00	111	488.3 Baud	976.6 Baud	1024 Baud
01	000	20.83 kbaud	41.67 kbaud	43.69 kbaud
01	001	10.42 kbaud	20.83 kbaud	21.85 kbaud
01	010	5208 Baud	10.42 kbaud	10.92 kbaud
01	011	2604 Baud	5208 Baud	5461 Baud
01	100	1302 Baud	2604 Baud	2731 Baud
01	101	651.0 Baud	1302 Baud	1365 Baud
01	110	325.5 Baud	651.0 Baud	682.7 Baud
01	111	162.8 Baud	325.5 Baud	341.3 Baud
10	000	15.63 kbaud	31.25 kbaud	32.77 kbaud
10	001	7813 Baud	15.63 kbaud	16.38 kbaud
10	010	3906 Baud	7813 Baud	8192 Baud
10	011	1953 Baud	3906 Baud	4906 Baud
10	100	976.6 Baud	1953 Baud	2048 Baud
10	101	488.3 Baud	976.6 Baud	1024 Baud
10	110	244.1 Baud	488.3 Baud	512.0 Baud
10	111	122.1 Baud	244.1 Baud	256.0 Baud
11	000	4808 Baud	9615 Baud	10.08 kbaud
11	001	2404 Baud	4808 Baud	5041 Baud
11	010	1202 Baud	2404 Baud	2521 Baud
11	011	601.0 Baud	1202 Baud	1260 Baud
11	100	300.5 Baud	601.0 Baud	630.2 Baud
11	101	150.2 Baud	300.5 Baud	315.1 Baud
11	110	75.12 Baud	150.2 Baud	157.5 Baud
11	111	37.56 Baud	75.12 Baud	78.77 Baud

SECTION 10
SERIAL PERIPHERAL INTERFACE

10.1 Introduction

The serial peripheral interface (SPI) is an interface built into the MC68HC05 MCU which allows several MC68HC05 MCUs or MC68HC05 MCU plus peripheral devices to be interconnected within a single printed circuit board. In an SPI, separate wires are required for data and clock. In the SPI format, the clock is not included in the data stream and must be furnished as a separate signal. An SPI system may be configured in a system containing one master MCU and several slave MCUs or in a system in which an MCU is capable of being a master or a slave.

10.2 Features

- Full Duplex, 4-Wire Synchronous Transfers
- Master or Slave Operation
- Bus Frequency Divided by 2 (Maximum) Master Bit Frequency
- Bus Frequency (Maximum) Slave Bit Frequency
- Four Programmable Master Bit Rates
- Programmable Clock Polarity and Phase
- End of Transmission Interrupt Flag
- Write Collision Flag Protection
- Master-Master Mode Fault Protection Capability

10.3 SPI Signal Description

The four basic signals (MOSI, MISO, SCK, $\overline{SS}$) are described in the following paragraphs. Each signal function is described for both the master and slave mode.

10.3.1 Master In Slave Out (MISO)

The MISO line is configured as an input in a master device and as an output in a slave device. It is one of the two lines that transfer serial data in one direction, with the most significant bit sent first. The MISO line of a slave device is placed in the high-impedance state if the slave is not selected.

10.3.2 Master Out Slave In (MOSI)

The MOSI line is configured as an output in a master device and as an input in a slave device. It is one of the two lines that transfer serial data in one direction with the most significant bit sent first.

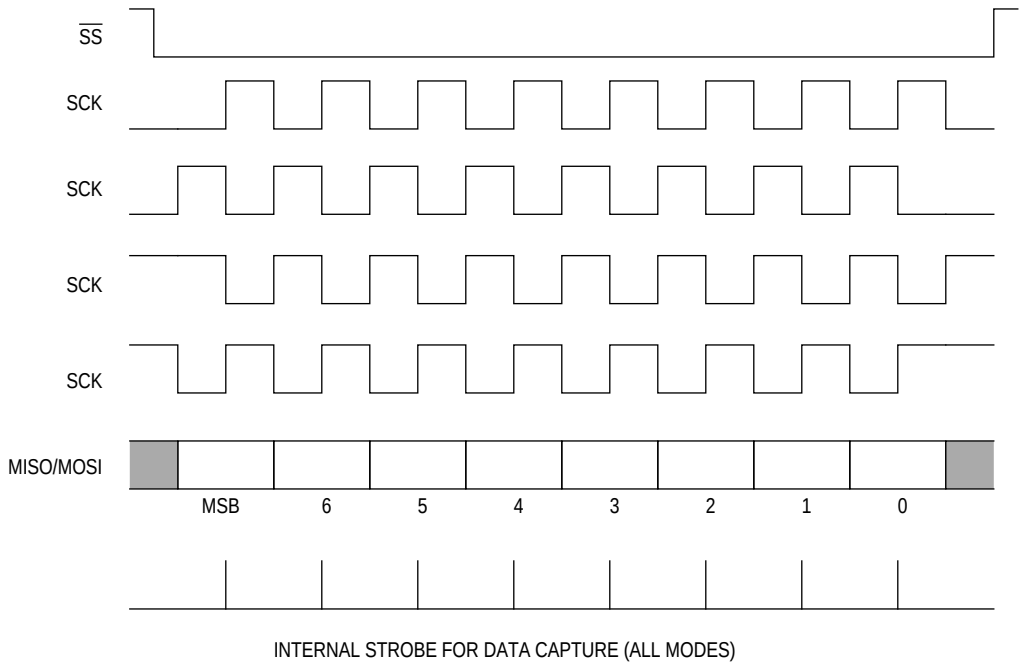


Figure 10-1. Data Clock Timing Diagram

10.3.3 Serial Clock (SCK)

The master clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines. The master and slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles. Since SCK is generated by the master device, this line becomes an input on a slave device.

As shown in Figure 10-1, four possible timing relationships may be chosen by using control bits CPOL and CPHA in the serial peripheral control register (SPCR). Both master and slave devices must operate with the same timing. The master

device always places data on the MOSI line one-half cycle before the clock edge (SCK), so the slave device can latch the data.

Two bits (SPR0 and SPR1) in the SPCR of the master device select the clock rate. In a slave device, SPR0 and SPR1 have no effect on the SPI operation.

10.3.4 Slave Select ($\overline{SS}$)

The slave select ($\overline{SS}$) input line is used to select a slave device. It has to be low prior to data transactions and must stay low for the duration of the transaction.

The $\overline{SS}$ line on the master must be tied high. If it goes low, a mode fault error flag (MODF) is set in the SPSR.

When CPHA = 0, the shift clock is the OR of $\overline{SS}$ with SCK. In this clock phase mode, $\overline{SS}$ must go high between successive characters in an SPI message. When CPHA = 1, $\overline{SS}$ may be left low for several SPI characters. In cases where there is only one SPI slave MCU, its $\overline{SS}$ line could be tied to V_{SS} as long as CPHA = 1 clock modes are used.

10.4 Functional Description

Figure 10-2 shows a block diagram of the serial peripheral interface circuitry. When a master device transmits data to a slave via the MOSI line, the slave device responds by sending data to the master device via the master's MISO line. This implies full duplex transmission with both data out and data in synchronized with the same clock signal. Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receive-full status bits. A single status bit (SPIF) is used to signify that the I/O operation has been completed.

The SPI data register (SPDR) is double buffered on read, but not on write. If a write is performed during data transfer, the transfer occurs uninterrupted, and the write will be unsuccessful. This condition will cause the write collision (WCOL) status bit in the SPSR to be set. After a data byte is shifted, the SPIF flag of the SPSR is set.

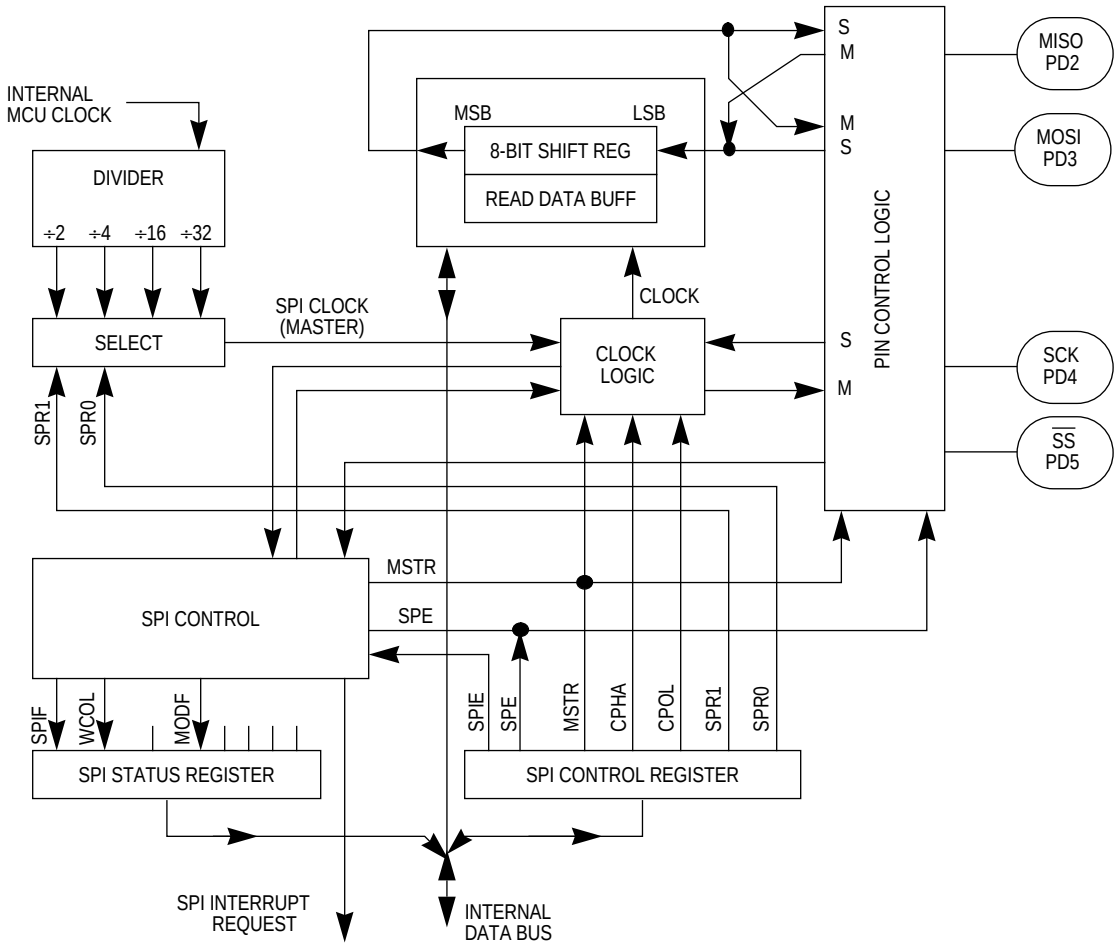


Figure 10-2. Serial Peripheral Interface Block Diagram

In the master mode, the SCK pin is an output. It idles high or low, depending on the CPOL bit in the SPCR, until data is written to the shift register, at which point eight clocks are generated to shift the eight bits of data and then SCK goes idle again.

In a slave mode, the slave select start logic receives a logic low at the $\overline{SS}$ pin and a clock at the SCK pin. Thus, the slave is synchronized with the master. Data from the master is received serially at the MOSI line and loads the 8-bit shift register. After the 8-bit shift register is loaded, its data is parallel transferred to the read buffer. During a write cycle, data is written into the shift register, then the slave waits for a clock train from the master to shift the data out on the slave's MISO line.

Figure 10-3 illustrates the MOSI, MISO, SCK, and $\overline{SS}$ master-slave interconnections.

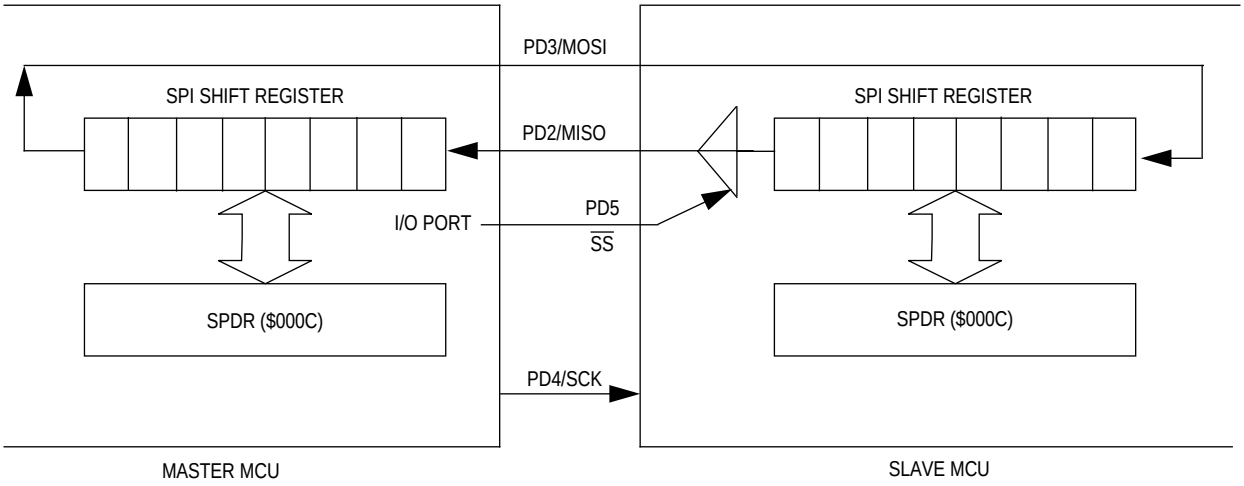


Figure 10-3. Serial Peripheral Interface Master-Slave Interconnection

10.5 SPI Registers

Three registers in the SPI provide control, status, and data storage functions. These registers are called the serial peripheral control register (SPCR), serial peripheral status register (SPSR), and serial peripheral data I/O register (SPDR) and are described in the following paragraphs.

10.5.1 Serial Peripheral Control Register (SPCR)

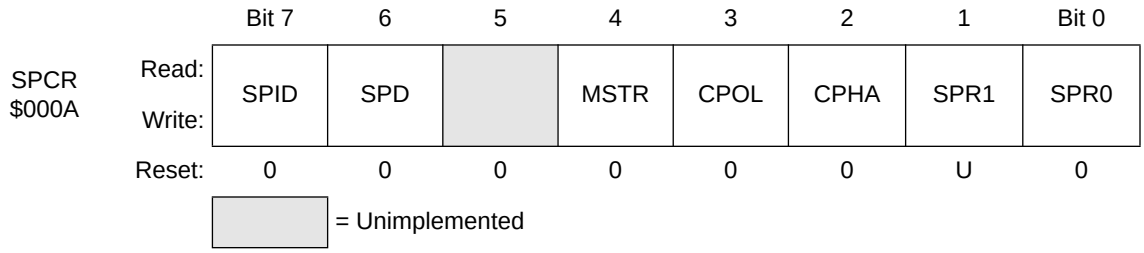


Figure 10-4. SPI Control Register

SPIE — Serial Peripheral Interrupt Enable
- 0 = SPIF interrupts disabled
- 1 = SPI interrupt is enabled

SPE — Serial Peripheral System Enable
- 0 = SPI system off
- 1 = SPI system on

MSTR — Master Mode Select
- 0 = Slave mode
- 1 = Master mode

CPOL — Clock Polarity

When the clock polarity bit is cleared and data is not being transferred, a steady state low value is produced at the SCK pin of the master device. Conversely, if this bit is set, the SCK pin will idle high. This bit also is used in conjunction with the clock phase control bit to produce the desired clock-data relationship between master and slave. See Figure 10-1.

CPHA — Clock Phase

The clock phase bit, in conjunction with the CPOL bit, controls the clock-data relationship between master and slave. The CPOL bit can be thought of as simply inserting an inverter in series with the SCK line. The CPHA bit selects one of two fundamentally different clocking protocols. When CPHA = 0, the shift

clock is the OR of SCK with $\overline{SS}$. As soon as $\overline{SS}$ goes low, the transaction begins and the first edge on SCK invokes the first data sample. When CPHA = 1, the $\overline{SS}$ pin may be thought of as a simple output enable control. See Figure 10-1.

SPR1 and SPR0 — SPI Clock Rate Selects

These two bits select one of four baud rates to be used as SCK if the device is a master; however, they have no effect in the slave mode. See Table 10-1.

Table 10-1. Serial Peripheral Rate Selection

SPR1	SPR0	Bus Clock Divided By
0	0	2
0	1	4
1	0	16
1	1	32

10.5.2 Serial Peripheral Status Register (SPSR)

		Bit 7	6	5	4	3	2	1	Bit 0
SPSR $000B	Read:	SPIF	WCOL	0	MODF	0	0	0	0
	Write:								
	Reset:	0	0	0	0	0	0	U	0

= Unimplemented

Figure 10-5. SPI Status Register

SPIF — SPI Transfer Complete Flag

The serial peripheral data transfer flag bit is set upon completion of data transfer between the processor and external device. If SPIF goes high and if SPIE is set, a serial peripheral interrupt is generated. Clearing the SPIF bit is accomplished by reading the SPSR (with SPIF set) followed by an access of the SPDR. Unless SPSR is read (with SPIF set) first, attempts to write to SPDR are inhibited.

WCOL — Write Collision

The write collision bit is set when an attempt is made to write to the serial peripheral data register while data transfer is taking place. If CPHA is zero, a transfer is said to begin when $\overline{SS}$ goes low and the transfer ends when $\overline{SS}$ goes high after eight clock cycles on SCK. When CPHA is one, a transfer is said to begin the first time SCK becomes active while $\overline{SS}$ is low. The transfer ends when the SPIF flag gets set. Clearing the WCOL bit is accomplished by reading the SPSR (with WCOL set) followed by an access to SPDR.

Bit 5 — Not implemented

This bit always reads zero.

MODF — Mode Fault

The mode fault flag indicates that there may have been a multi-master conflict for system control and allows a proper exit from system operation to a reset or default system state. The MODF bit is normally clear and is set only when the master device has its $\overline{SS}$ pin pulled low. Setting the MODF bit affects the internal serial peripheral interface system in the following ways:

1. An SPI interrupt is generated if SPIE = 1.
2. The SPE bit is cleared. This disables the SPI.
3. The MSTR bit is cleared, thus forcing the device into the slave mode.

Clearing the MODF bit is accomplished by reading the SPSR (with MODF set), followed by a write to the SPCR. Control bits SPE and MSTR may be restored by user software to their original state after the MODF bit has been cleared.

Bits 3–0 — Not Implemented

These bits always read zero.

10.5.3 Serial Peripheral Data I/O Register (SPDR) $0C

The serial peripheral data I/O register is used to transmit and receive data on the serial bus. Only a write to this register will initiate transmission/reception of another byte, and this will occur only in the master device. At the completion of transmitting a byte of data, the SPIF status bit is set in both the master and slave devices.

When the user reads the serial peripheral data I/O register, a buffer is actually being read. The first SPIF must be cleared by the time a second transfer of the data from the shift register to the read buffer is initiated or an overrun condition will exist. In cases of overrun, the byte which causes the overrun is lost.

A write to the serial peripheral data I/O register is not buffered and places data directly into the shift register for transmission.

SECTION 11
OPERATING MODES

11.1 Introduction

The MCU has two modes of operation: user mode and self-check mode. Table 11-1 shows the conditions required to enter into each mode, where $V_{TST} = 2 \times V_{DD}$.

Table 11-1. Operating Mode Conditions

$\overline{\text{RESET}}$	$\overline{\text{IRQ}}$	TCAP	Mode
	V_{SS} to V_{DD}	V_{SS} to V_{DD}	User
	V_{TST}	V_{DD}	Self-Check

11.2 User Mode

In user mode, the address and data buses are not available externally, but there are three 8-bit I/O ports and one 7-bit input-only port. This mode allows the MCU to function as a self-contained microcontroller, with maximum use of the pins for on-chip peripheral functions. All address and data activity occurs within the MCU. User mode is entered on the rising edge of $\overline{\text{RESET}}$ if the $\overline{\text{IRQ}}$ pin is within normal operating range.

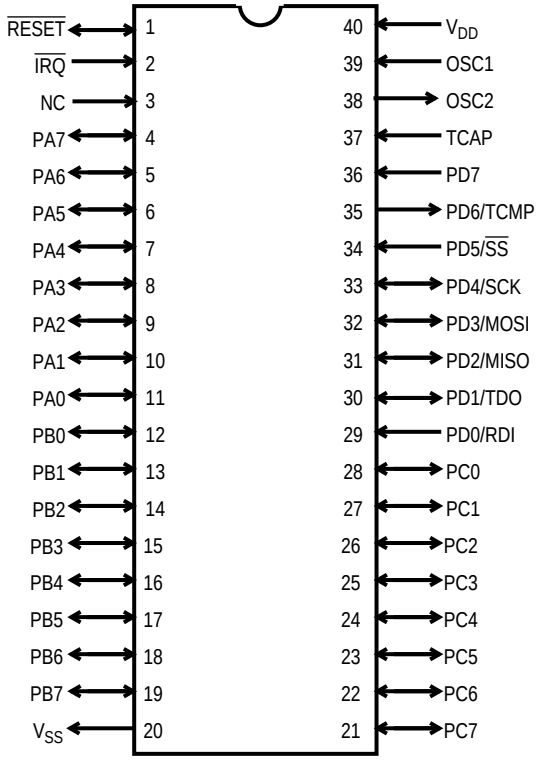


Figure 11-1. User Mode Pinout

11.3 Self-Check Mode

Self-check mode is entered upon the rising edge of $\overline{\text{RESET}}$ if the $\overline{\text{IRQ}}$ pin is at V_{TST} and the TCAP pin is at logic one.

11.3.1 Self-Check Tests

The self-check ROM at mask ROM location $3F00–$3FEF determines if the MCU is functioning properly.The following tests are performed:

1. I/O — Functional test of ports A, B, and C
2. RAM — Counter test for each RAM byte
3. Timer — Test of counter register and OCF bit
4. SCI — Transmission test checks for RDRF, TDRE, TC, and FE flags
5. ROM — Exclusive OR with odd ones parity result
6. SPI — Transmission test checks for SPIF and WCOL flags

The self-check circuit is shown in Figure 11-2.

11.3.2 Self-Check Results

Table 11-2 shows the LED codes that indicate self-check test results.

Table 11-2. Self-Check Circuit LED Codes

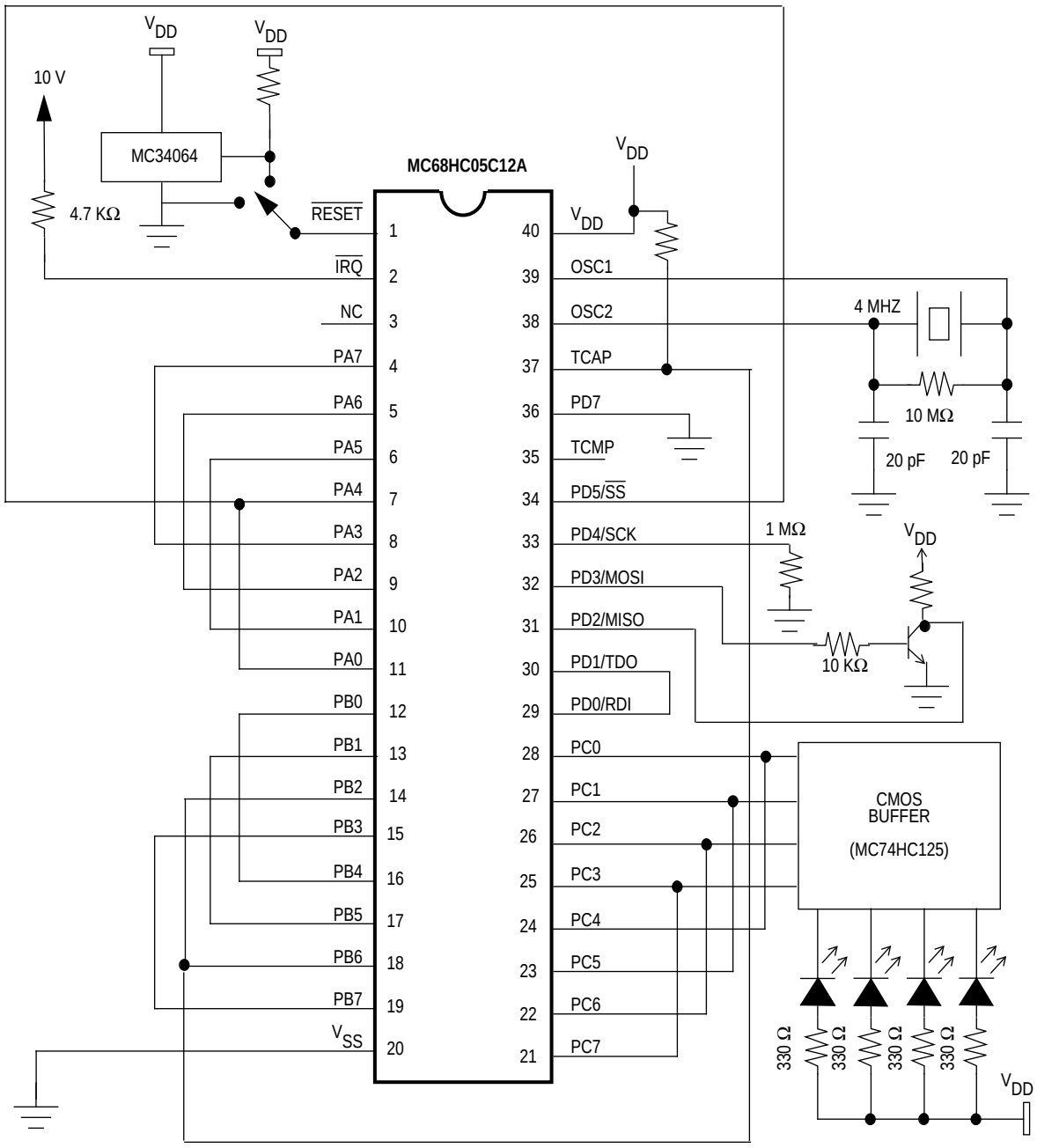
PC3	PC2	PC1	PC0	Remarks
Off	On	On	Off	I/O Failure
Off	On	Off	On	RAM Failure
Off	On	Off	Off	Timer Failure
Off	Off	On	On	SCI Failure
Off	Off	On	Off	ROM Failure
Off	Off	Off	On	SPI Failure
Flashing				No Failure
All Others				Device Failure

Perform the following steps to activate the self-check tests:

1. Apply 10 V (2 x V_{DD}) to the $\overline{IRQ}$ pin.
2. Apply a logic one to the TCAP pin.
3. Apply a logic zero to the $\overline{RESET}$ pin.

The self-check tests begin on the rising edge of the $\overline{RESET}$ pin.

$\overline{RESET}$ must be held low for 4064 cycles after power-on reset (POR) or for a time, t_{RL}, for any other reset. (For the t_{RL} value, see **Table 13-6. Control Timing (V_{DD} = 5.0 Vdc)**.)



NOTES:
1. V_{DD} = 5.0 V
2. TCMP = NC

Figure 11-2. Self-Check Circuit Schematic

SECTION 12
INSTRUCTION SET

12.1 Introduction

This section describes the MC68HC05C12A addressing modes and instruction types.

12.2 Addressing Modes

The CPU uses eight addressing modes for flexibility in accessing data. The addressing modes define the manner in which the CPU finds the data required to execute an instruction. The eight addressing modes are:

- Inherent
- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset
- Relative

12.2.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no memory address and are one byte long.

12.2.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no memory address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

12.2.3 Direct

Direct instructions can access any of the first 256 memory addresses with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address. BRSET and BRCLR are three-byte instructions that use direct addressing to access the operand and relative addressing to specify a branch destination.

12.2.4 Extended

Extended instructions use only three bytes to access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Motorola assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

12.2.5 Indexed, No Offset

Indexed instructions with no offset are one-byte instructions that can access data with variable addresses within the first 256 memory locations. The index register contains the low byte of the conditional address of the operand. The CPU automatically uses $00 as the high byte, so these instructions can address locations $0000–$00FF.

Indexed, no offset instructions are often used to move a pointer through a table or to hold the address of a frequently used RAM or I/O location.

12.2.6 Indexed, 8-Bit Offset

Indexed, 8-bit offset instructions are two-byte instructions that can access data with variable addresses within the first 511 memory locations. The CPU adds the unsigned byte in the index register to the unsigned byte following the opcode. The sum is the conditional address of the operand. These instructions can access locations $0000–$01FE.

Indexed 8-bit offset instructions are useful for selecting the kth element in an n-element table. The table can begin anywhere within the first 256 memory locations and could extend as far as location 510 ($01FE). The k value is typically in the index register, and the address of the beginning of the table is in the byte following the opcode.

12.2.7 Indexed, 16-Bit Offset

Indexed, 16-bit offset instructions are three-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned byte in the index register to the two unsigned bytes following the opcode. The sum is the conditional address of the operand. The first byte after the opcode is the high byte of the 16-bit offset; the second byte is the low byte of the offset. These instructions can address any location in memory.

Indexed, 16-bit offset instructions are useful for selecting the kth element in an n-element table anywhere in memory.

As with direct and extended addressing the Motorola assembler determines the shortest form of indexed addressing.

12.2.8 Relative

Relative addressing is only for branch instructions. If the branch condition is true, the CPU finds the conditional branch destination by adding the signed byte following the opcode to the contents of the program counter. If the branch condition is not true, the CPU goes to the next instruction. The offset is a signed, two’s complement byte that gives a branching range of –128 to +127 bytes from the address of the next location after the branch instruction.

When using the Motorola assembler, the programmer does not need to calculate the offset because the assembler determines the proper offset and verifies that it is within the span of the branch.

12.3 Instruction Types

The MCU instructions fall into five categories:

- Register/Memory instructions
- Read-Modify-Write instructions
- Jump/Branch instructions
- Bit Manipulation instructions
- Control instructions

12.3.1 Register/Memory Instructions

Most of these instructions use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory. Table 12-1 lists the register/memory instructions.

Table 12-1. Register/Memory Instructions

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

12.3.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register. The test for negative or zero instruction (TST) is an exception to the read-modify-write sequence because it does not write a replacement value. Table 12-2 lists the read-modify-write instructions.

Table 12-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic Shift Left	ASL
Arithmetic Shift Right	ASR
Clear Bit in Memory	BCLR
Set Bit in Memory	BSET
Clear	CLR
Complement (One’s Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left	LSL
Logical Shift Right	LSR
Negate (Two’s Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST

12.3.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump to subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed. All branch instructions use relative addressing.

Bit test and branch instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These three-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the conditional branch destination by adding

the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register. Table 12-3 lists the jump and branch instructions.

Table 12-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if Carry Bit Clear	BCC
Branch if Carry Bit Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Bit Clear	BHCC
Branch if Half-Carry Bit Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if $\overline{\text{IRQ}}$ Pin High	BIH
Branch if $\overline{\text{IRQ}}$ Pin Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit Clear	BRCLR
Branch Never	BRN
Branch if Bit Set	BRSET
Branch to Subroutine	BSR
Unconditional Jump	JMP
Jump to Subroutine	JSR

12.3.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory. Port registers, port data direction registers, timer registers, and on-chip RAM locations are in the first 256 bytes of memory. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations. Bit manipulation instructions use direct addressing. Table 12-4 lists these instructions.

Table 12-4. Bit Manipulation Instructions

Instruction	Mnemonic
Clear Bit	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Set Bit	BSET

12.3.5 Control Instructions

These register reference instructions control CPU operation during program execution. Control instructions, listed in Table 12-5, use inherent addressing.

Table 12-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

12.4 Instruction Set Summary

Table 12-6 is an alphabetical list of all M68HC05 instructions and shows the effect of each instruction on the condition code register.

Table 12-6. Instruction Set Summary

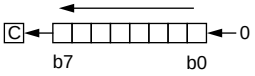
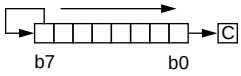
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AN*D opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3

Table 12-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BIH *rel*	Branch if $\overline{\text{IRQ}}$ Pin High	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if $\overline{\text{IRQ}}$ Pin Low	PC ← (PC) + 2 + *rel* ? $\overline{\text{IRQ}}$ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff p	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if bit n clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr	5
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr	5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3

Table 12-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (M) X ← ($\overline{X}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	1	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3

Table 12-6. Instruction Set Summary (Continued)

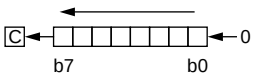
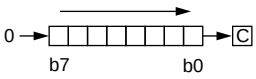
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC CC DC EC FC	dd hh ll ee ff ff 	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Conditional Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD DD ED FD	dd hh ll ee ff ff 	5 6 7 6 5
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff 	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff 	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	ii ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2

Table 12-6. Instruction Set Summary (Continued)

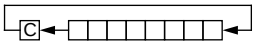
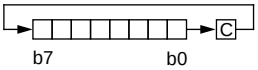
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff	5 3 3 6 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	INH	80		6
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)						INH			
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff	4 5 6 5 4
STOP	Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff	4 5 6 5 4

Table 12-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff	2 3 4 5 4 3
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10
TAX	Transfer Accumulator to Index Register	X ← (A)	—	—	—	—	—	INH	97		2
TST *opr* TSTA TSTX TST *opr*,X TST ,X	Test Memory Byte for Negative or Zero	(M) – $00	—	—	—	—	—	DIR INH INH IX1 IX	3D 4D 5D 6D 7D	dd ff	4 3 3 5 4
TXA	Transfer Index Register to Accumulator	A ← (X)	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	×	—	—	—	INH	8F		2

A	Accumulator	*opr*	Operand (one or two bytes)
C	Carry/borrow flag	PC	Program counter
CCR	Condition code register	PCH	Program counter high byte
dd	Direct address of operand	PCL	Program counter low byte
dd rr	Direct address of operand and relative offset of branch instruction	REL	Relative addressing mode
DIR	Direct addressing mode	*rel*	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	rr	Relative program counter offset byte
EXT	Extended addressing mode	SP	Stack pointer
ff	Offset byte in indexed, 8-bit offset addressing	X	Index register
H	Half-carry flag	Z	Zero flag
hh ll	High and low bytes of operand address in extended addressing	#	Immediate value
I	Interrupt mask	∧	Logical AND
ii	Immediate operand byte	∨	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	( )	Contents of
IX	Indexed, no offset addressing mode	–( )	Negation (two's complement)
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX2	Indexed, 16-bit offset addressing mode	?	If
M	Memory location	:	Concatenated with
N	Negative flag	↕	Set or cleared
n	Any bit	—	Not affected

Table 12-7. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSB / LSB
0	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0
1	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1
2	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2
3	5 BRCLR1 3 DIR	5 BCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3
4	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4
5	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS/BLO 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5
6	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6
7	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7
8	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 ASL/LSL 2 DIR	3 ASLA/LSLA 1 INH	3 ASLX/LSLX 1 INH	6 ASL/LSL 2 IX1	5 ASL/LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8
9	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9
A	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A
B	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B
C	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C
D	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D
E	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E
F	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended
REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

MSB / LSB	0	
LSB of Opcode in Hexadecimal	0	5 BRSET0 3 DIR

MSB of Opcode in Hexadecimal
Number of Cycles
Opcode Mnemonic
Number of Bytes/Addressing Mode

SECTION 13
ELECTRICAL SPECIFICATIONS

13.1 Introduction

This section contains electrical and timing specifications.

13.2 Maximum Ratings

Maximum ratings are the extreme limits the device can be exposed to without causing permanent damage to the chip. The device is **not** intended to operate at these conditions. The MCU contains circuitry that protects the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in Table 13-1. Keep V_{IN} and V_{OUT} within the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Connect unused inputs to the appropriate logical voltage level, either V_{SS} or V_{DD}.

Table 13-1. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	V
Current Drain Per Pin (Excluding V_{DD} and V_{SS})	I	25	mA
$\overline{IRQ}$ Pin Only		V_{SS} – 0.3 to 2 × V_{DD} + 0.3	V
Storage Temperature Range	T_{STG}	–65 to +150	°C

13.3 Operating Temperature Range

Table 13-2. Operating Temperature Range

Characteristic	Symbol	Value	Unit
Operating Temperature Range MC68HC05C12AP, FN, B, FB MC68HC05C12ACP, CFN, CB, CFB	T_A	T_L to T_H 0 to +70 –40 to +85	°C

NOTES:

1. P = Plastic dual-in-line package (PDIP)
2. FN = Plastic-leaded chip carrier (PLCC)
3. C = Extended temperature range (–40° to +85°)
4. B = Shrink dual-in-line-package (SDIP)
5. FB = Quad flat pack (QFP)

13.4 Thermal Characteristics

Table 13-3. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance Plastic Dual-In-Line Package (PDIP) Plastic Leaded Chip Carrier (PLCC) Quad Flat Pack (QFP) Plastic Shrink DIP (SDIP)	θ_{JA}	 60 70 95 60	°C/W

13.5 Power Considerations

The average chip-junction temperature, T_J, in °C, can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction to ambient, °C/W.
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{DD} \times V_{DD}$ watts (chip internal power)
$P_{I/O}$ = Power dissipation on input and output pins (user-determined)

For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.

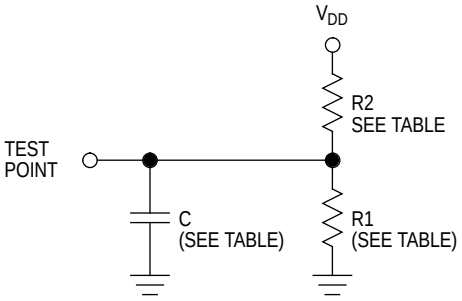
Following is an approximate relationship between P_D and T_J (neglecting $P_{I/O}$):

$$P_D = K \div (T_J + 273\ °C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273\ °C) + \theta_{JA} \times (P_D)^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.



V_{DD} = 4.5 V

Pins	R1	R2	C
PA7–PA0 PB7–PB0 PC7–PC0 PD5–PD0, PD7	3.26 Ω	2.38 Ω	50 pF

V_{DD} = 3.0 V

Pins	R1	R2	C
PA7–PA0 PB7–PB0 PC7–PC0 PD5–PD0, PD7	10.91 Ω	6.32 Ω	50 pF

Figure 13-1. Test Load

13.6 DC Electrical Characteristics

Table 13-4. DC Electrical Characteristics (V_{DD} = 5.0 Vdc)(1)

Characteristic(2)	Symbol	Min	Typ	Max	Unit
Output Voltage I_{LOAD} = 10.0 µA I_{LOAD} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD}–0.1	 — —	 0.1 —	 V
Output High Voltage (I_{LOAD} = –0.8 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP (I_{LOAD} = –1.6 mA) PD4–PD1 (I_{LOAD} = –5.0 mA) PC7	V_{OH}	 V_{DD}–0.8 V_{DD}–0.8 V_{DD}–0.8	 — — —	 — — —	V
Output Low Voltage (I_{LOAD} = 1.6 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1, TCMP (I_{LOAD} = 10 mA) PC7	V_{OL}	 — —	 — —	 0.4 0.4	V
Input High Voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply Current (4.5–5.5 Vdc @ f_{BUS} = 2.1 MHz) (See NOTES) Run(3) Wait(4) Stop(5) 25 °C 0 °C to 70 °C (Standard) –40 °C to +85 °C (Standard)	 I_{DD}	 — — — — —	 3.50 1.00 1 — —	 5.25 3.25 20 40 50	 mA mA µA µA µA
I/O Ports Hi-Z Leakage Current PA7–PA0, PB7–PB0 (Without Pullup) PC7–PC0, PD7, PD5–PD0	I_{oz}	—	—	±10	µA
Input Current $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5–PD0	I_{in}	—	—	±1	µA
Input Pullup Current(6) PB7–PB0 (With Pullup)	I_{in}	175	385	750	µA
Capacitance Ports (as Input or Output) $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5, PD0	 C_{out} C_{in}	 — —	 — —	 12 8	 pF

NOTES:
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 °C to +85 °C, unless otherwise noted.
2. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
4. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.
5. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD} –0.2 V.
6. Input pullup current measured with V_{IL} = 0.2 V.

Table 13-5. DC Electrical Characteristics (V_{DD} = 3.3 Vdc)[1]

Characteristic[2]	Symbol	Min	Typ	Max	Unit
Output Voltage I_{LOAD} = 10.0 µA I_{LOAD} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD}–0.1	 — —	 0.1 —	V
Output High Voltage (I_{LOAD} = –0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP (I_{LOAD} = –0.4 mA) PD4–PD1 (I_{LOAD} = –1.5 mA) PC7	V_{OH}	 V_{DD}–0.3 V_{DD}–0.3 V_{DD}–0.3	 — — —	 — — —	V
Output Low Voltage (I_{LOAD} = 0.4 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1, TCMP (I_{LOAD} = 6 mA) PC7	V_{OL}	 —	 —	 0.3	V
Input High Voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IH}	$0.7 \times V_{DD}$	—	V_{DD}	V
Input Low Voltage PA7–PA0, PB7–PB0, PC7–PC0, PD7, PD5–PD0, TCAP, $\overline{IRQ}$, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	$0.2 \times V_{DD}$	V
Supply Current (3.0–3.6 Vdc @ f_{BUS} = 1.0 MHz) (See NOTES) Run[3] Wait[4] Stop[5] 25°C 0 °C to +70 °C (Standard) –40 °C to +85 °C (Standard)	 I_{DD}	 — — — — —	 1.00 500 1 — —	 1.60 900 8 16 20	 mA µA µA µA µA
I/O Ports Hi-Z Leakage Current PA7–PA0, PB7–PB0 (Without Pullup) PC7–PC0, PD7, PD5–PD0	I_{oz}	—	—	±10	µA
Input Current $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5, PD0	I_{in}	—	—	±1	µA
Input Pullup Current (6) PB7–PB0 (With Pullup)	I_{in}	75	175	350	µA
Capacitance Ports (as Input or Output) $\overline{RESET}$, $\overline{IRQ}$, OSC1, TCAP, PD7, PD5, PD0	C_{out} C_{in}	 — —	 — —	 12 8	pF

NOTES:
1. V_{DD} = 3.3 Vdc ± 0.3 Vdc, V_{SS} = 0 Vdc, T_A = –40 °C to +85 °C, unless otherwise noted.
2. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.
3. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
4. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.
5. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V.
6. Input pullup current measured with V_{IL} = 0.2 V.

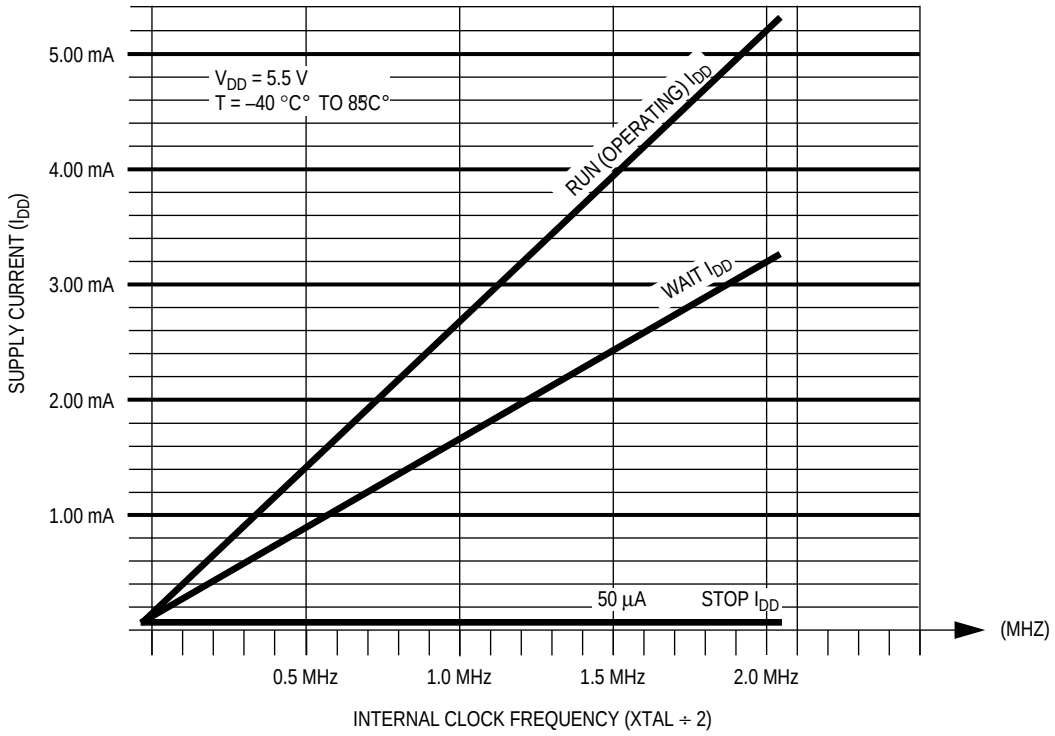


Figure 13-2. Maximum Supply Current vs. Internal Clock Frequency, V_{DD} = 5.5 V

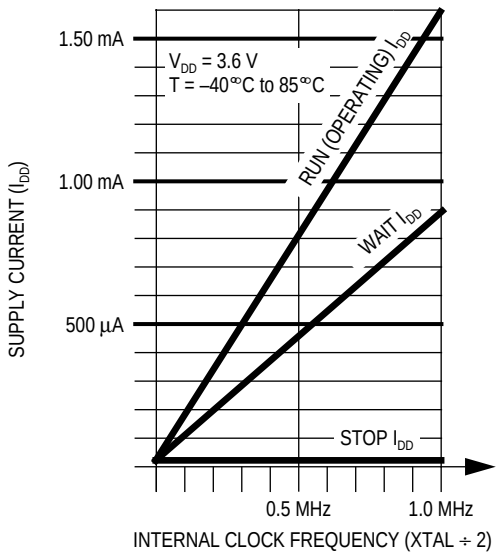


Figure 13-3. Maximum Supply Current vs. Internal Clock Frequency, V_{DD} = 3.6 V

Table 13-6. Control Timing (V_{DD} = 5.0 Vdc)[1]

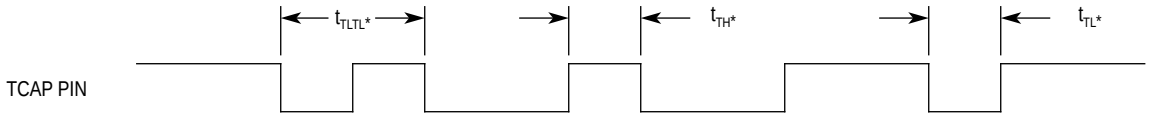
Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal External Clock	f_{osc}	— dc	4.2 4.2	MHz
Internal Operating Frequency Crystal External Clock	f_{op}	— dc	2.1 2.1	MHz
Internal Clock Cycle Time	t_{cyc}	480	—	ns
Crystal Oscillator Startup Time	t_{oxov}		100	ms
Stop Recovery Startup Time (Crystal Oscillator)	t_{ilch}		100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{rl}	1.5	—	t_{CYC}
Timer Resolution[2] Input Capture Pulse Width Input Capture Pulse Period	 t_{resl} t_{TH}, t_{TL} t_{TLTL}	 4.0 125 Note[3]	 — — —	 t_{CYC} ns t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
Interrupt Pulse Period	t_{ILIL}	Note[4]	—	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	90	—	ns

NOTES:
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40 °C to +85 °C, unless otherwise noted.
2. Because a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
3. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
4. The minimum t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.

Table 13-7. Control Timing (V_{DD} = 3.3 Vdc)[1]

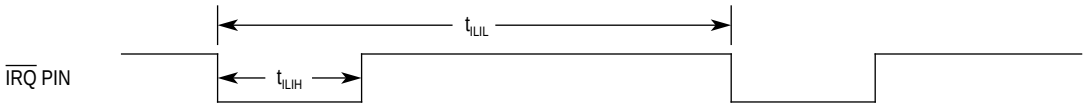
Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal External Clock	f_{osc}	— dc	2.0 2.0	MHz
Internal Operating Frequency Crystal External Clock	f_{op}	— dc	1.00 1.00	MHz
Internal Clock Cycle Time	t_{cyc}	1000	—	ns
Crystal Oscillator Startup Time	t_{oxov}		100	ms
Stop Recovery Startup Time (Crystal Oscillator)	t_{ILCH}		100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	—	t_{CYC}
Timer Resolution[2] Input Capture Pulse Width Input Capture Pulse Period	t_{RESL} t_{TH}, t_{TL} t_{TLTL}	4.0 250 Note[3]	— — —	t_{CYC} ns t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	250	—	ns
Interrupt Pulse Period	t_{ILIL}	Note[4]	—	t_{CYC}
OSC1 Pulse Width	t_{OH}, t_{OL}	200	—	ns

NOTES:
1. V_{DD} = 3.3 Vdc ± 0.3 Vdc, V_{SS} = 0 Vdc, T_A = –40 °C to +85 °C, unless otherwise noted.
2. Because a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
3. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
4. The minimum t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.

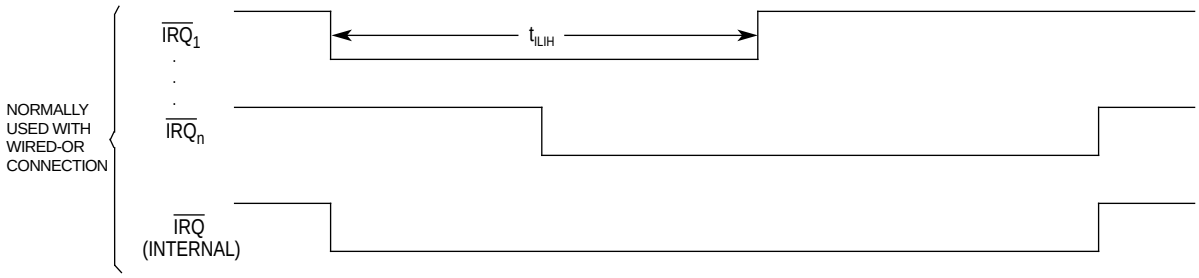


*Refer to timer resolution data in Tables 8-6 and 8-7.

Figure 13-4. TCAP Timing Relationships

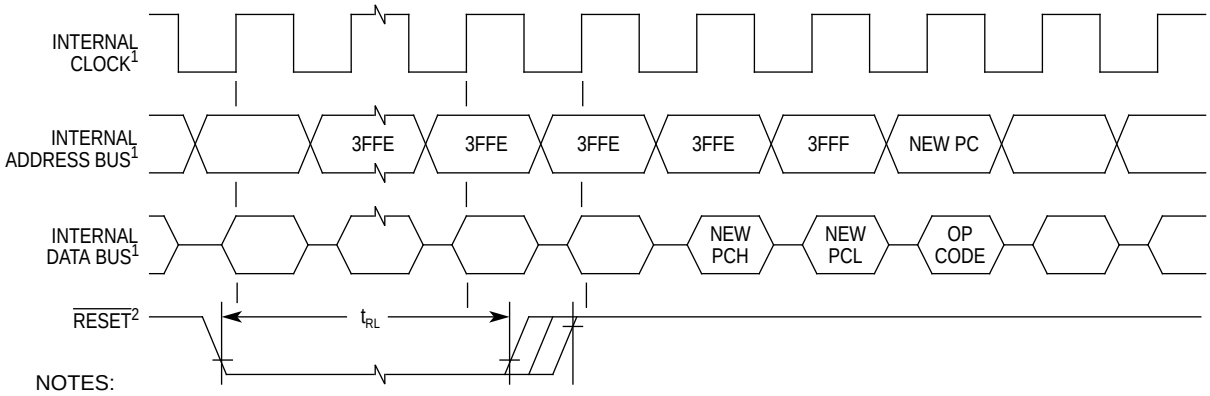


a. **Edge-Sensitive Trigger Condition.** The minimum pulse width (t_{ILIH}) is either 125 ns (f_{OP} = 2.1 MHz) or 250 ns (f_{OP} = 1 MHz). The period t_{ILIL} should not be less than the number of t_{CYC} cycles it takes to execute the interrupt service routine plus 19 t_{CYC} cycles.



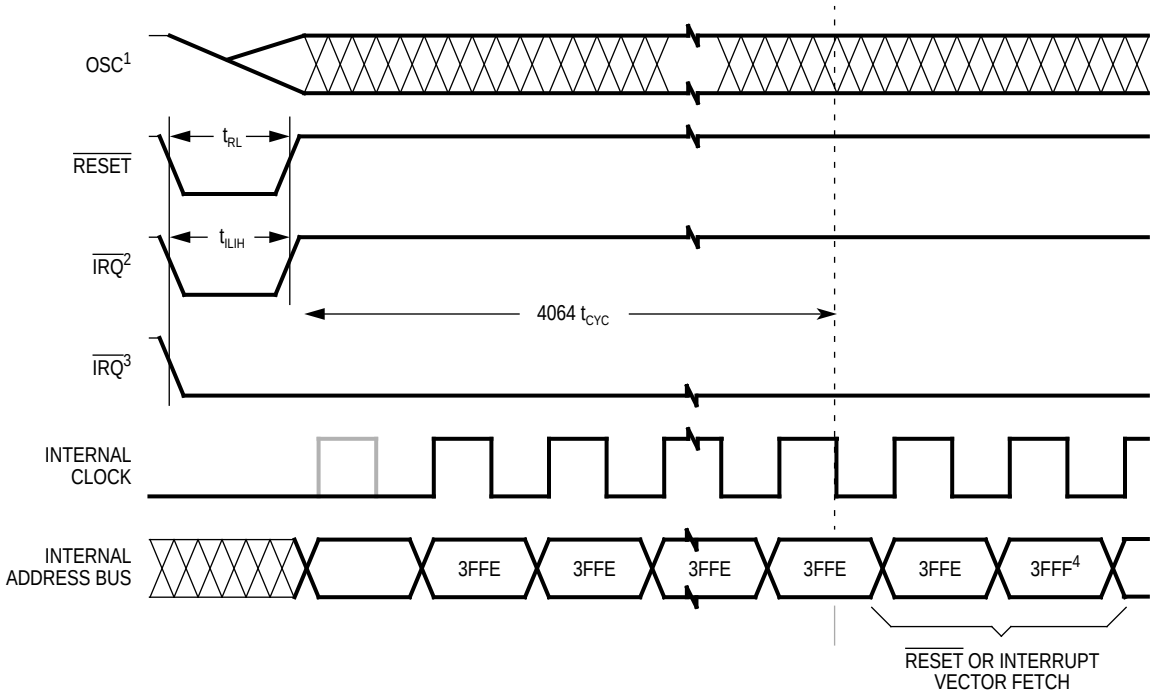
b. **Level-Sensitive Trigger Condition**. If after servicing an interrupt the $\overline{IRQ}$ remains low, the next interrupt is recognized.

Figure 13-5. External Interrupt Timing



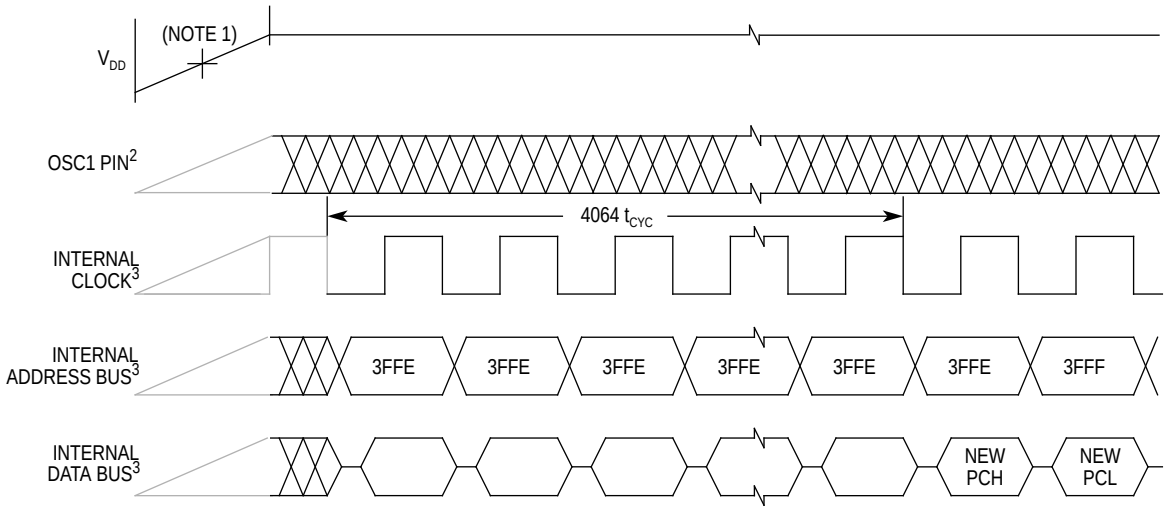
NOTES:
1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{RESET}$ initiates the reset sequence.

Figure 13-6. External Reset Timing



NOTES:
1. Represents the internal clocking of the OSC1 pin
2. IRQ pin edge-sensitive mask option
3. IRQ pin level- and edge-sensitive mask option
4. RESET vector address shown for timing example

Figure 13-7. STOP Recovery Timing Diagram



NOTES:
1. Power-on reset threshold is typically between 1 V and 2 V.
2. OSC1 line is meant to represent time only, not frequency.
3. Internal clock, internal address bus, and internal data bus are not available externally.

Figure 13-8. Power-On Reset Timing Diagram

Table 13-8. Serial Peripheral Interface Timing (V_{DD} = 5.0 Vdc)*

Num	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 dc dc	 0.5 2.1	 f_{OP} MHz
1	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 480	 — —	 t_{CYC} ns
2	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 † 240	 — —	 ns
3	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 † 720	 — —	 ns
4	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 340 190	 — —	 ns
5	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 340 190	 — —	 ns
6	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 100 100	 — —	 ns
7	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 100 100	 — —	 ns
8	Slave Access Time (Time to Data Active from High-Impedance State)	t_A	0	120	ns
9	Slave Disable Time (Hold Time to High-Impedance State)	t_{DIS}	—	240	ns
10	Data Valid Master (Before Capture Edge) Slave (After Enable Edge)‡	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 240	 $t_{CYC(M)}$ ns
11	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 100 2.0	 ns µs

*V_{DD} = 5.0 Vdc ± 10%; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H. Refer to Figures 8-9 and 8-10 for timing diagrams.

†Signal production depends on software.

‡Assumes 200 pF load on all SPI pins

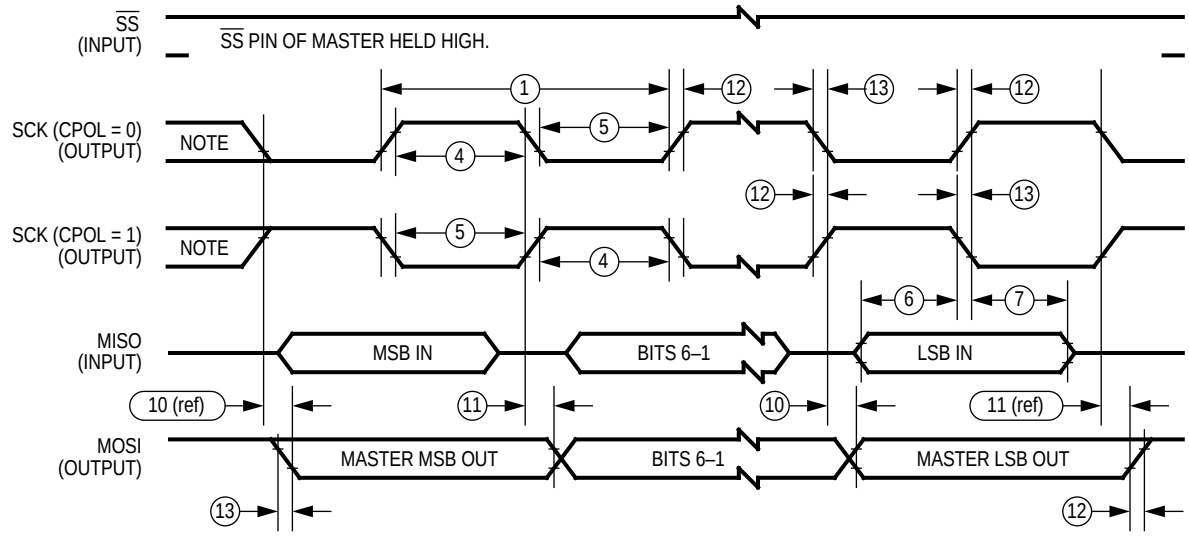
Table 13-9. Serial Peripheral Interface Timing (V_{DD} = 3.3 Vdc)*

Num	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 dc dc	 0.5 1.0	 f_{OP} MHz
1	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 1.0	 — —	 t_{CYC} µs
2	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 † 500	 — —	 ns
3	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 † 1.5	 — —	 ns µs
4	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 720 400	 — —	 ns
5	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 720 400	 — —	 ns
6	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 200 200	 — —	 ns
7	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 200 200	 — —	 ns
8	Slave Access Time (Time to Data Active from High-Impedance State)	t_A	0	250	ns
9	Slave Disable Time (Hold Time to High-Impedance State)	t_{DIS}	—	500	ns
10	Data Valid Master (Before Capture Edge) Slave (After Enable Edge)‡	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 500	 $t_{CYC(M)}$ ns
11	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	 $t_{CYC(M)}$ ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 200 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 200 2.0	 ns µs

*V_{DD} = 3.3 Vdc ± 0.3 Vdc; V_{SS} = 0 Vdc, $T_A = T_L$ to T_H. Refer to Figures 8-9 and 8-10 for timing diagrams.

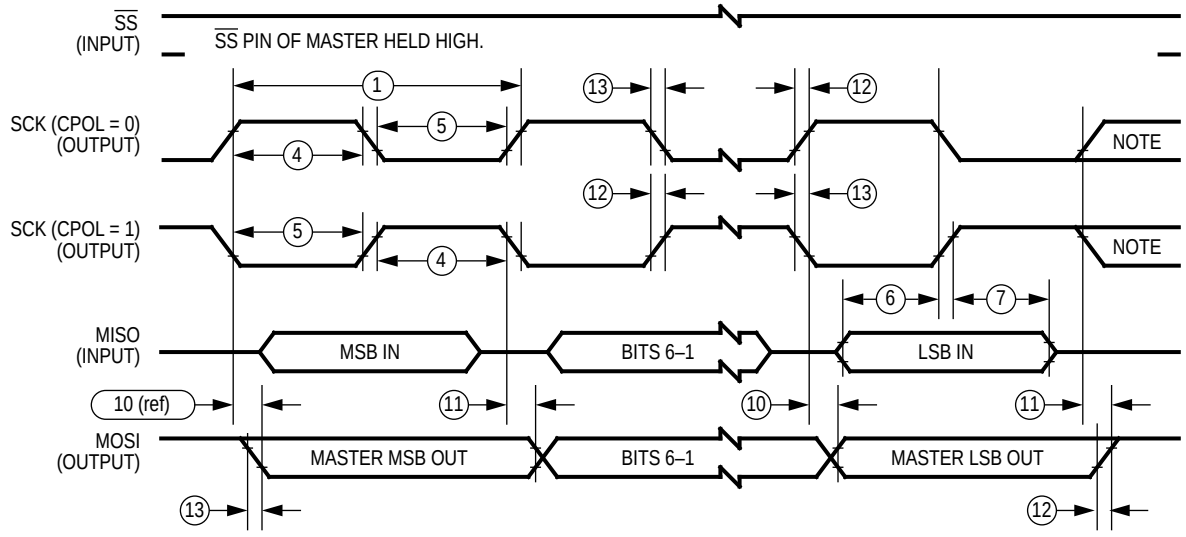
†Signal production depends on software.

‡Assumes 200 pF load on all SPI pins



NOTE: This first clock edge is generated internally, but is not seen at the SCK pin.

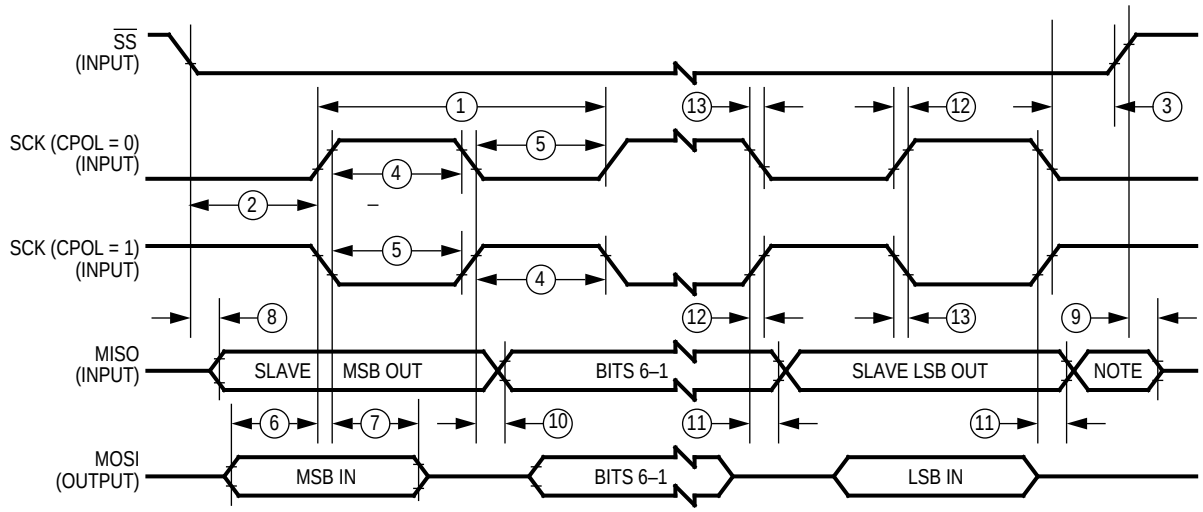
a) SPI Master Timing (CPHA = 0)



NOTE: This last clock edge is generated internally, but is not seen at the SCK pin.

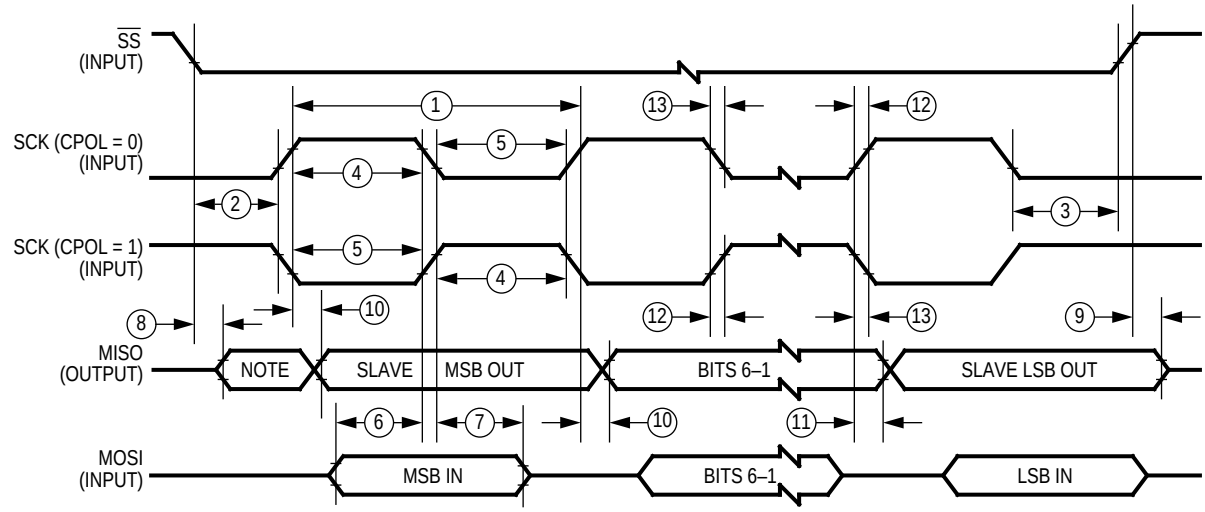
b) SPI Master Timing (CPHA = 1)

Figure 13-9. SPI Master Timing Diagram



NOTE: Not defined but normally MSB of character just received.

a) SPI Slave Timing (CPHA = 0)



NOTE: Not defined but normally LSB of character previously transmitted.

a) SPI Slave Timing (CPHA = 1)

Table 13-10. SPI Slave Timing Diagram

SECTION 14
MECHANICAL SPECIFICATIONS

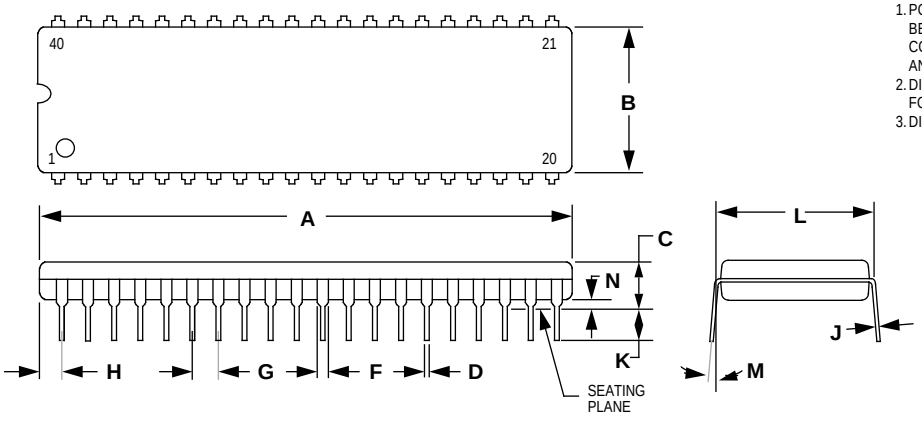
14.1 Introduction

This section describes the dimensions of the dual in-line package (DIP), plastic shrink dual in-line package (SDIP), plastic leaded chip carrier (PLCC), and quad flat pack (QFP) MCU packages. Package dimensions available at time of this publication are provided in this section. To make sure that you have the latest case outline specifications, contact one of the following:

- Local Motorola Sales Office
- Motorola Mfax
  - Phone 602-244-6609
  - EMAIL rmfax0@email.sps.mot.com
- Worldwide Web (wwweb) at http://design-net.com

Follow Mfax or wwweb on-line instructions to retrieve the current mechanical specifications.

14.2 40-Pin Plastic Dual In-Line (DIP) Package (Case 711-03)

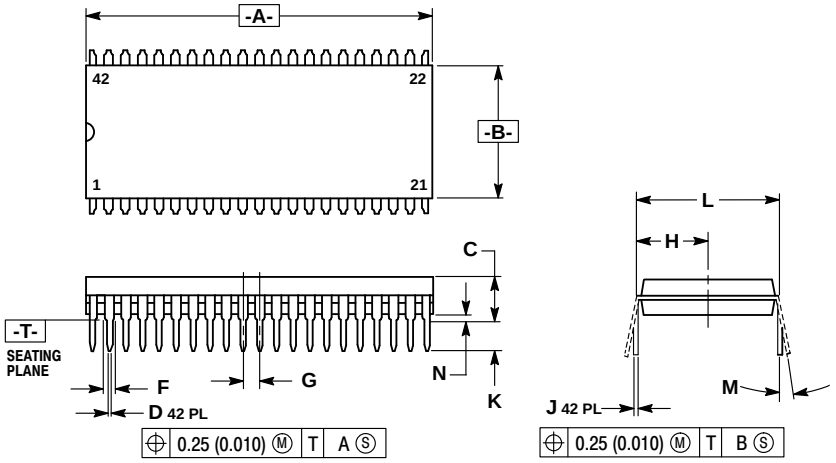


NOTES:
1. POSITION TOLERANCE OF LEADS (D), SHALL BEWITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITIONS, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	1°	0°	1°
N	0.51	1.02	0.020	0.040

Figure 14-1. 40-Pin Plastic DIP Package (Case 711-03)

14.3 42-Pin Plastic Shrink Dual In-Line (SDIP) Package (Case 858-01)

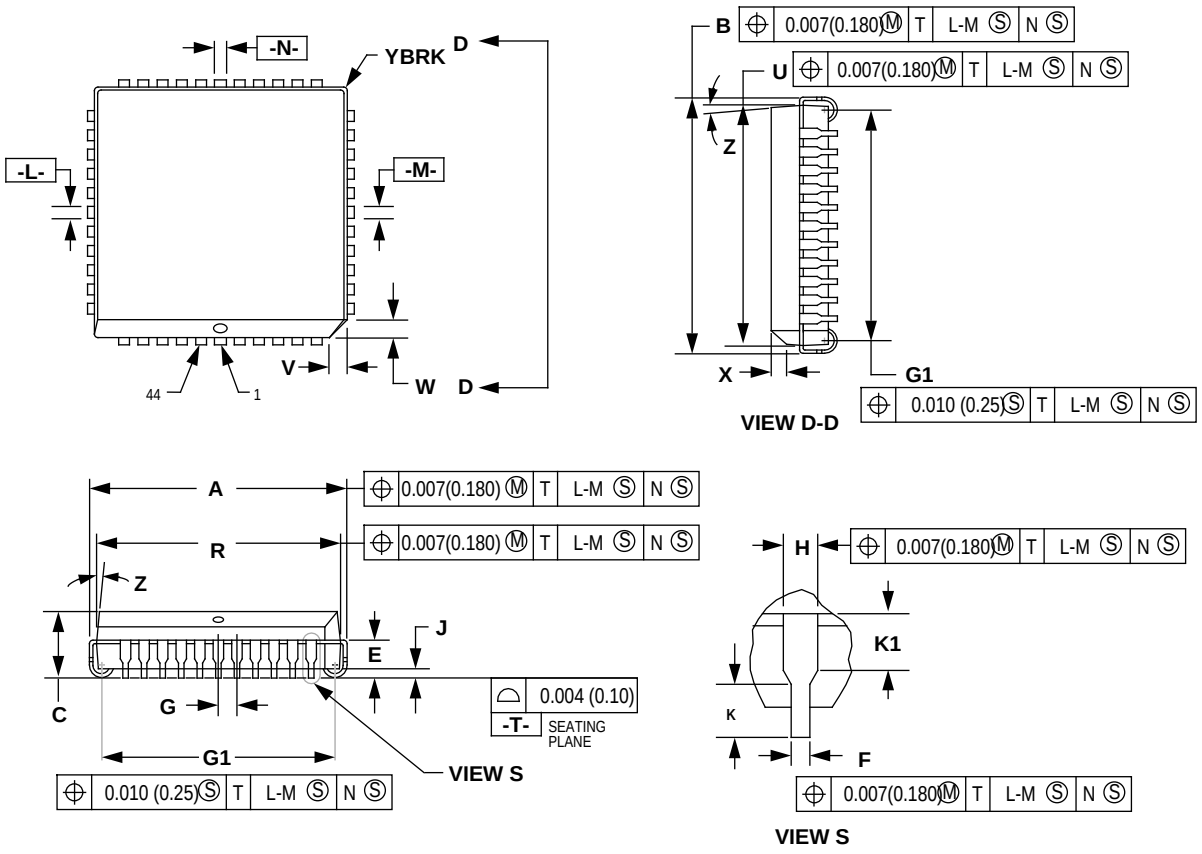


NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH. MAXIMUM MOLD FLASH 0.25 (0.010).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.435	1.465	36.45	37.21
B	0.540	0.560	13.72	14.22
C	0.155	0.200	3.94	5.08
D	0.014	0.022	0.36	0.56
F	0.032	0.046	0.81	1.17
G	0.070 BSC		1.778 BSC	
H	0.300 BSC		7.62 BSC	
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.600 BSC		15.24 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.02

Figure 14-2. 42-Pin Plastic SDIP Package (Case 858-01)

14.4 44-Lead Plastic Leaded Chip Carrier (PLCC) (Case 777-02)

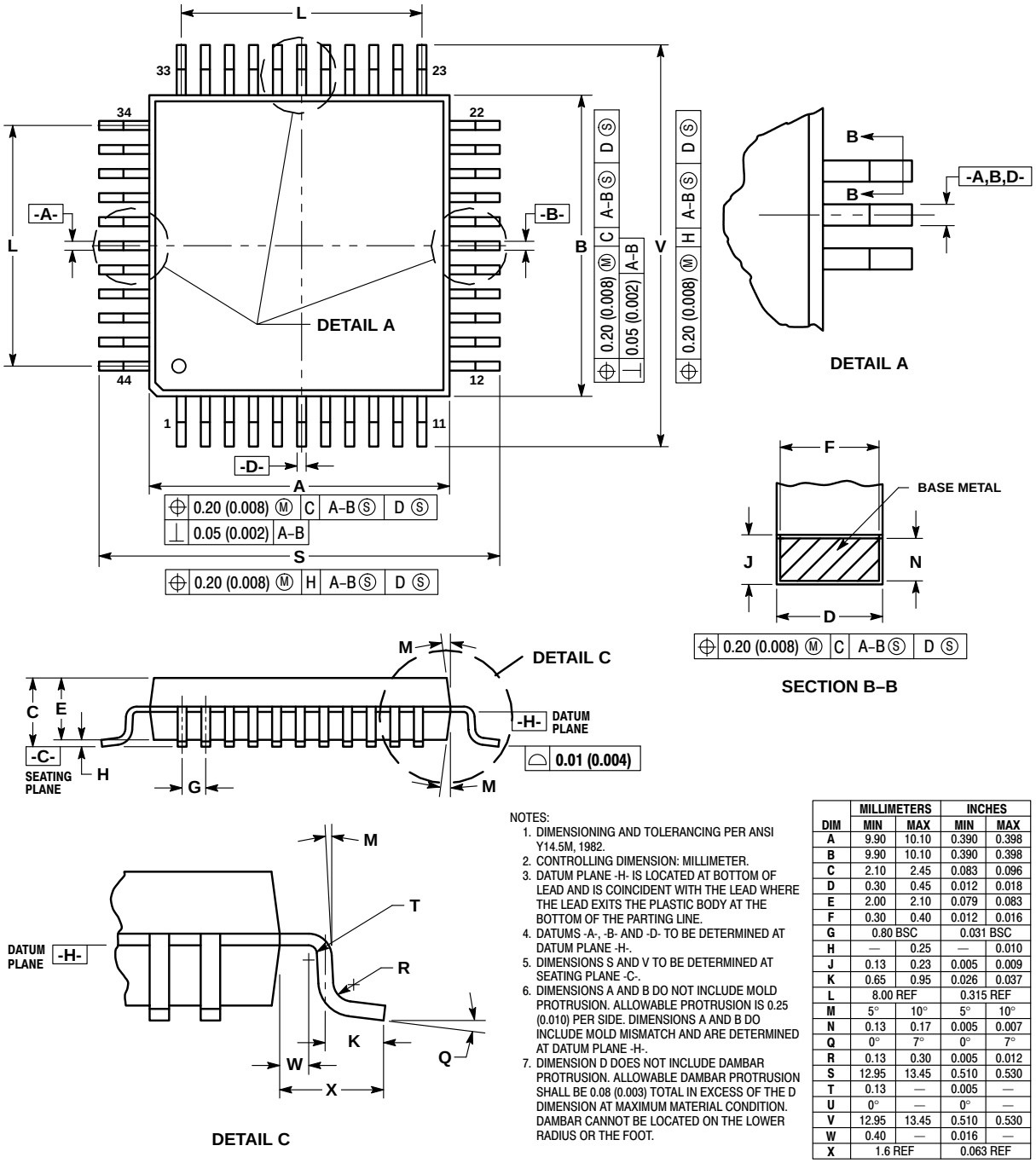


NOTES:
1. DATUMS -L-, -M-, AND -N- ARE DETERMINED WHERE TOP OF LEAD SHOLDERS EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSION R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.25) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF THE MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMINSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTUSION(S) SHALL NOT CAUSE THE H DIMINSION TO BE GREATER THAN 0.037 (0.9404). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMINISION TO SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.685	0.695	17.40	17.65
B	0.685	0.695	17.40	17.65
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.650	0.656	16.51	16.66
U	0.650	0.656	16.51	16.66
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.610	0.630	15.50	16.00
K1	0.040	—	1.02	—

Figure 14-3. 44-Lead PLCC (Case 777-02)

14.5 44-Lead Quad Flat Pack (QFP) (Case 824A-01)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.30	0.45	0.012	0.018
E	2.00	2.10	0.079	0.083
F	0.30	0.40	0.012	0.016
G	0.80 BSC		0.031 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	8.00 REF		0.315 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.40	—	0.016	—
X	1.6 REF		0.063 REF	

Figure 14-4. 44-Lead QFP (Case 824A-01)

SECTION 15
ORDERING INFORMATION

15.1 Introduction

This section contains instructions for ordering custom-masked ROM MCUs.

15.2 MCU Ordering Forms

To initiate an order for a ROM-based MCU, first obtain the current ordering form for the MCU from a Motorola representative. Submit the following items when ordering MCUs:

- A current MCU ordering form that is **completely filled out** (Contact your Motorola sales office for assistance.)
- A copy of the customer specification if the customer specification deviates from the Motorola specification for the MCU
- Customer's application program on one of the media listed in **15.3 Application Program Media**

The current MCU ordering form is also available through the Motorola Freeware Bulletin Board Service (BBS). The telephone number is (512) 891-FREE. After making the connection, type bbs in lowercase letters. Then press the return key to start the BBS software.

15.3 Application Program Media

Please deliver the application program to Motorola in one of the following media:

- Macintosh®[1] 3-1/2-inch diskette (double-sided 800 K or double-sided high-density 1.4 M)
- MS-DOS®[2] or PC-DOS™[3] 3-1/2-inch diskette (double-sided 720 K or double-sided high-density 1.44 M)
- MS-DOS® or PC-DOS™ 5-1/4-inch diskette (double-sided double-density 360 K or double-sided high-density 1.2 M)

Use positive logic for data and addresses.

1. Macintosh is a registered trademark of Apple Computer, Inc.
2. MS-DOS is a registered trademark of Microsoft Corporation.
3. PC-DOS is a trademark of International Business Machines Corporation.

When submitting the application program on a diskette, clearly label the diskette with the following information:

- Customer name
- Customer part number
- Project or product name
- File name of object code
- Date
- Name of operating system that formatted diskette
- Formatted capacity of diskette

On diskettes, the application program must be in Motorola's S-record format (S1 and S9 records), a character-based object file format generated by M6805 cross assemblers and linkers.
Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. **Write $00 in all non-user ROM locations or leave all non-user ROM locations blank**. Refer to the current MCU ordering form for additional requirements. Motorola may request pattern re-submission if non-user areas contain any non-zero code.

If the memory map has two user ROM areas with the same addresses, then write the two areas in separate files on the diskette. Label the diskette with both filenames.

In addition to the object code, a file containing the source code can be included. Motorola keeps this code confidential and uses it only to expedite ROM pattern generation in case of any difficulty with the object code. Label the diskette with the filename of the source code.

15.4 ROM Program Verification

The primary use for the on-chip ROM is to hold the customer's application program. The customer develops and debugs the application program and then submits the MCU order along with the application program.

Motorola inputs the customer's application program code into a computer program that generates a listing verify file. The listing verify file represents the memory map of the MCU. The listing verify file contains the user ROM code and may also contain non-user ROM code, such as self-check code. Motorola sends the customer a computer printout of the listing verify file along with a listing verify form.

To aid the customer in checking the listing verify file, Motorola will program the listing verify file into customer-supplied blank preformatted Macintosh or DOS disks. All original pattern media are filed for contractual purposes and are not returned.

Check the listing verify file thoroughly, then complete and sign the listing verify form and return the listing verify form to Motorola. The signed listing verify form constitutes the contractual agreement for the creation of the custom mask.

15.5 ROM Verification Units (RVUs)

After receiving the signed listing verify form, Motorola manufactures a custom photographic mask. The mask contains the customer's application program and is used to process silicon wafers. The application program cannot be changed after the manufacture of the mask begins. Motorola then produces 10 MCUs, called RVUs, and sends the RVUs to the customer. RVUs are usually packaged in unmarked ceramic and tested to 5 Vdc at room temperature. RVUs are not tested to environmental extremes because their sole purpose is to demonstrate that the customer's user ROM pattern was properly implemented. The 10 RVUs are free of charge with the minimum order quantity. These units are not to be used for qualification or production. RVUs are not guaranteed by Motorola Quality Assurance.

15.6 MC Order Numbers

Table 15-1 shows the MC order numbers for the available package types.

Table 15-1. MC Order Numbers

Package Type	Operating Temperature Range	MC Order Number
40-Pin Plastic Dual In-Line Package (DIP)	0 °C to 70 °C	MC68HC05C12AP
42-Pin Plastic Shrink Dual In-Line Package (SDIP)	0 °C to 70 °C	MC68HC05C12AB
44-Lead Plastic Leaded Chip Carrier (PLCC)	0 °C to 70 °C	MC68HC05C12AFN
44-Lead Quad Flat Pack (QFP)	0 °C to 70 °C	MC68HC05C12AFB
Extended Temperature Range		
40-Pin Plastic Dual In-Line Package (DIP)	–40 °C to +85 °C	MC68HC05C12ACP
42-Pin Plastic Shrink Dual In-Line Package (SDIP)	–40 °C to +85 °C	MC68HC05C12ACB
44-Lead Plastic Leaded Chip Carrier (PLCC)	–40 °C to +85 °C	MC68HC05C12ACFN
44-Lead Quad Flat Pack (QFP)	–40 °C to +85 °C	MC68HC05C12ACFB

APPENDIX A
MC68HCL05C12A

A.1 Introduction

Appendix A introduces the MC68HCL05C12A, a low-power version of the MC68HC05C12A. The technical data applying to the MC68HC05C12A applies to the MC68HCL05C12A with the exceptions given in this appendix.

A.2 DC Electrical Characteristics

The data in Table A-1 replaces the corresponding data in **Table 13-2 . Operating Temperature Range**.

Table A-1. Low-Power Operating Temperature Range

Rating	Symbol	Value	Unit
Operating Temperature Range MC68HCL05C12AP, FN, B, FB	T_A	T_L to T_H 0 to +70	°C

NOTES:
1. P = Plastic dual-in-line package (PDIP)
2. FN = Plastic-leaded chip carrier (PLCC)
3. B = Shrink dual-in-line-package (SDIP)
4. FB = Quad flat pack (QFP)

The data in Table 13-4 and Table 13-5 (MC68HC05C12A DC electrical characteristics data) applies to the MC68HCL05C12A with the exceptions given in the following tables.

Table A-2. Low-Power Output Voltage (V_{DD} = 1.8–2.4 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = –0.1 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP (I_{LOAD} = –0.2 mA) PD4–PD1 (I_{LOAD} = –0.75 mA) PC7	V_{OH} V_{OH} V_{OH}	V_{DD} – 0.3 V_{DD} – 0.3 V_{DD} – 0.3	— — —	— — —	V
Output Low Voltage (I_{LOAD} = 0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1, TCMP (I_{LOAD} = 2.0 mA) PC7	V_{OL} V_{OL}	— —	— —	0.3 0.3	V

Table A-3. Input Pullup Current (V_{DD} = 1.8–2.4 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Pullup Current PB7–PB0 (with pullup)	I_{in}	50	110	200	µA

Table A-4. Low-Power Output Voltage (V_{DD} = 2.5–3.6 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Output High Voltage (I_{LOAD} = –0.2 mA) PA7–PA0, PB7–PB0, PC6–PC0, TCMP (I_{LOAD} = –0.4 mA) PD4–PD1 (I_{LOAD} = –1.5 mA) PC7	V_{OH} V_{OH} V_{OH}	V_{DD} – 0.3 V_{DD} – 0.3 V_{DD} – 0.3	— — —	— — —	V
Output Low Voltage (I_{LOAD} = 0.4 mA) PA7–PA0, PB7–PB0, PC6–PC0, PD4–PD1, TCMP (I_{LOAD} = 5.0 mA) PC7	V_{OL} V_{OL}	— —	— —	0.3 0.3	V

Table A-5. Input Pullup Current (V_{DD} = 2.5–3.6 Vdc)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Pullup Current PB7–PB0 (with pullup)	I_{in}	50	160	300	µA

Table A-6. Low-Power Supply Current

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Supply Current (4.5–5.5 Vdc @ f_{BUS} = 2.1 MHz)					
Run	I_{DD}	—	3.50	4.25	mA
Wait		—	1.6	2.25	mA
Stop					
25 °C		—	1	15	µA
0 °C to +70 °C (Standard)		—	—	25	µA
Supply Current (2.4–3.6 Vdc @ f_{BUS} = 1.0 MHz)					
Run[2]	I_{DD}	—	1.00	1.4	mA
Wait[3]		—	0.7	1.0	mA
Stop[4]					
25 °C		—	1	5	µA
0 °C to +70 ° C (Standard)		—	—	10	µA
Supply Current (2.5–3.6 Vdc @ f_{BUS} = 500 kHz)					
Run	I_{DD}	—	500	750	µA
Wait		—	300	500	µA
Stop					
25 °C		—	1	5	µA
0 °C to +70 °C (Standard)		—	—	10	µA
Supply Current (1.8–2.4 Vdc @ f_{BUS} = 500 kHz)					
Run	I_{DD}	—	300	600	µA
Wait		—	250	400	µA
Stop					
25 °C		—	1	2	µA
0 °C to +70 °C (Standard)		—	—	5	µA

NOTES:

1. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.
2. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
3. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.
4. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V

APPENDIX B
MC68HSC05C12A

B.1 Introduction

Appendix B introduces the MC68HSC05C12A, a high-speed version of the MC68HC05C12A. The technical data applying to the MC68HC05C12A applies to the MC68HSC05C12A with the exceptions given in this appendix.

B.2 DC Electrical Characteristics

The data in Table B-1 replaces the corresponding data in **Table 13-2 . Operating Temperature Range**.

Table B-1. High-Speed Operating Temperature Range

Rating	Symbol	Value	Unit
Operating Temperature Range MC68HSC05C12AP, FN, B, FB MC68HSC05C12ACP, CFN, CB, CFB	T_A	T_L to T_H 0 to +70 –40 to +85	°C

NOTES:
1. P = Plastic dual-in-line package (PDIP)
2. FN = Plastic-leaded chip carrier (PLCC)
3. C = Extended temperature range (–40° to +85°)
4. B = Shrink dual-in-line-package (SDIP)
5. FB = Quad flat pack (QFP)

The data in Table 13-4 and Table 13-5 (MC68HC05C12A DC electrical characteristics data) applies to the MC68HSC05C12A with the exceptions given in Table B-2 and Table B-3.

Table B-2. High-Speed Supply Current

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Supply Current (4.5–5.5 Vdc @ f_{BUS} = 4.0 MHz)					
Run[2]		—	7.00	11.0	mA
Wait[3]		—	2.00	6.50	mA
Stop[4]	I_{DD}				
25°C		—	1	20	µA
0 °C to 70 °C (Standard)		—	—	40	µA
–40 °C to 85 °C (Standard)		—	—	50	µA
Supply Current (2.4–3.6 Vdc @ f_{BUS} = 2.0 MHz)					
Run[2]		—	2.50	4.00	mA
Wait[3]		—	1.00	2.00	mA
Stop[4]	I_{DD}				
25° C		—	1	8	µA
0 °C to 70° C (Standard)		—	—	16	µA
–40 °C to 85° C (Standard)		—	—	20	µA

NOTES:
1. Typical values reflect measurements taken on average processed devices at the midpoint of voltage range, 25 °C only.
2. Run (operating) I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
3. Wait I_{DD} measured using external square wave clock source; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V; no DC loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2. Wait I_{DD} is affected linearly by the OSC2 capacitance.
4. Stop I_{DD} measured with OSC1 = 0.2 V; all I/O pins configured as inputs, Port B = V_{DD}, all other inputs V_{IL} = 0.2 V, V_{IH} = V_{DD}–0.2 V

Table B-3. Input Pullup Current

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Input Pullup Current (V_{DD} = 4.5–5.5 V) PB7–PB0 (With Pullup)	I_{in}	175	385	750	µA
Input Pullup Current (V_{DD} = 2.4–3.6 V) PB7–PB0 (With Pullup)	I_{in}	50	160	350	µA

B.3 Control Timing

The data in Table 13-6, Table 13-7, Table 13-8, and Table 13-9 (MC68HC05C12A control timing data) applies to the MC68HSC05C12A with the exceptions given in Table B-4, Table B-5, Table B-6, and Table B-7.

Table B-4. High-Speed Control Timing (V_{DD} = 4.5–5.5 Vdc)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal External Clock	f_{OSC}	— dc	8.2 8.2	MHz
Internal Operating Frequency ($f_{OSC} \div 2$) Crystal External Clock	f_{OP}	— dc	4.1 4.1	MHz
Cycle Time	t_{cyc}	244	—	ns
Crystal Oscillator Startup Time	t_{OXOV}		100	ms
Stop Recovery Startup Time	t_{ILCH}		100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	—	t_{CYC}
Timer Resolution(1) Input Capture Pulse Width Input Capture Pulse Width	 t_{RESL} t_{TH} or t_{TL} t_{THTL}	 4.0 64 (2)	 — — —	 t_{CYC} ns t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	64	—	ns
Interrupt Pulse Period	t_{ILIL}	(3)	—	t_{CYC}
OSC1 Pulse Width	t_{OH} or t_{OL}	50	—	ns

1. Because a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.

Table B-5. High-Speed Control Timing (V_{DD} = 2.4–3.6 Vdc)

Characteristic	Symbol	Min	Max	Unit
Oscillator Frequency Crystal External Clock	f_{OSC}	— dc	4.2 4.2	MHz
Internal Operating Frequency ($f_{OSC} \div 2$) Crystal External Clock	f_{OP}	— dc	2.1 2.1	MHz
Cycle Time	t_{cyc}	480	—	ns
Crystal Oscillator Startup Time	t_{OXOV}		100	ms
Stop Recovery Startup Time	t_{ILCH}		100	ms
$\overline{\text{RESET}}$ Pulse Width	t_{RL}	1.5	—	t_{CYC}
Timer Resolution(1) Input Capture Pulse Width Input Capture Pulse Width	 t_{RESL} t_{TH} or t_{TL} t_{THTL}	 4.0 125 (2)	 — — —	 t_{CYC} ns t_{CYC}
Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	125	—	ns
Interrupt Pulse Period	t_{ILIL}	(3)	—	t_{CYC}
OSC1 Pulse Width	t_{OH} or t_{OL}	90	—	ns

1. Because a 2-bit prescaler in the timer must count four internal cycles (t_{CYC}), this is the limiting minimum factor in determining the timer resolution.
2. The minimum period t_{TLTL} should not be less than the number of cycle times it takes to execute the capture interrupt service routine plus 24 t_{CYC}.
3. The minimum t_{ILIL} should not be less than the number of cycle times it takes to execute the interrupt service routine plus 19 t_{CYC}.

Table B-6. High-Speed SPI Timing (V_{DD} = 4.5–5.5 Vdc)

Num	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 dc dc	 0.5 4.1	f_{OP} MHz
1	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 244	 — —	t_{CYC} ns
2	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 † 122	 — —	 ns ns
3	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 † 366	 — —	 ns ns
4	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 166 93	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 166 93	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 49 49	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 49 49	 — —	 ns ns
8	Slave Access Time (Time to Data Active from High-Impedance State)	t_A	0	61	ns
9	Slave Disable Time (Hold Time to High-Impedance State)	t_{DIS}	—	122	ns
10	Data Valid Master (Before Capture Edge) Slave (After Enable Edge)‡	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 122	$t_{CYC(M)}$ ns
11	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	$t_{CYC(M)}$ ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 50 1.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 50 1.0	 ns µs

† Signal production depends on software.
‡ Assumes 200 pF load on all SPI pins.

Table B-7. High-Speed SPI Timing (V_{DD} = 2.4–3.6 Vdc)

Num	Characteristic	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	 $f_{OP(M)}$ $f_{OP(S)}$	 dc dc	 0.5 2.1	f_{OP} MHz
1	Cycle Time Master Slave	 $t_{CYC(M)}$ $t_{CYC(S)}$	 2.0 480	 — —	t_{CYC} ns
2	Enable Lead Time Master Slave	 $t_{LEAD(M)}$ $t_{LEAD(S)}$	 † 240	 — —	 ns ns
3	Enable Lag Time Master Slave	 $t_{LAG(M)}$ $t_{LAG(S)}$	 † 720	 — —	 ns ns
4	Clock (SCK) High Time Master Slave	 $t_{W(SCKH)M}$ $t_{W(SCKH)S}$	 340 190	 — —	 ns ns
5	Clock (SCK) Low Time Master Slave	 $t_{W(SCKL)M}$ $t_{W(SCKL)S}$	 340 190	 — —	 ns ns
6	Data Setup Time (Inputs) Master Slave	 $t_{SU(M)}$ $t_{SU(S)}$	 100 100	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	 $t_{H(M)}$ $t_{H(S)}$	 100 100	 — —	 ns ns
8	Slave Access Time (Time to Data Active from High-Impedance State)	t_A	0	120	ns
9	Slave Disable Time (Hold Time to High-Impedance State)	t_{DIS}	—	240	ns
10	Data Master (Before Capture Edge) Slave (After Enable Edge)‡	 $t_{V(M)}$ $t_{V(S)}$	 0.25 —	 — 240	$t_{CYC(M)}$ ns
11	Data Hold Time (Outputs) Master (After Capture Edge) Slave (After Enable Edge)	 $t_{HO(M)}$ $t_{HO(S)}$	 0.25 0	 — —	$t_{CYC(M)}$ ns
12	Rise Time (20% V_{DD} to 70% V_{DD}, C_L = 200pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{RM} t_{RS}	 — —	 100 2.0	 ns µs
13	Fall Time (70% V_{DD} to 20% V_{DD}, C_L = 200 pF) SPI Outputs (SCK, MOSI, and MISO) SPI Inputs (SCK, MOSI, MISO, and $\overline{SS}$)	 t_{FM} t_{FS}	 — —	 100 2.0	 ns µs

† Signal production depends on software.
‡ Assumes 200 pF load on all SPI pins.

APPENDIX C
M68HC05Cx FAMILY FEATURE COMPARISONS

Refer to Table C-1 for a comparison of the features for all the M68HC05C Family members.

Table C-1. M68HC05Cx Feature Comparison

	C4	C4A	705C4A	C8	C8A	705C8	705C8A	C12	C12A	C9	C9A	705C9	705C9A
USER ROM	4160	4160	—	7744	7744	—	—	12,096	12,096	15,760-15,936	15,760-15,936	—	—
USER EPROM	—	—	4160	—	—	7596-7740	7596-7740	—	—	—	—	15,760-15,936	12,096-15,936
CODE SECURITY	NO	YES	YES	NO	YES	YES	YES	NO	YES	NO	YES	NO	YES
RAM	176	176	176	176	176	176-304	176-304	176	176	176-352	176-352	176-352	176-352
OPTION REGISTER (IRQ/RAM/SEC)	NO	NO	$1FDF (IRQ/SEC)	NO	NO	$1FDF (IRQ/RAM/SEC)	$1FDF (IRQ/RAM/SEC)	NO	NO	$3FDF (IRQ/RAM)	$3FDF (IRQ/RAM)	$3FDF (IRQ/RAM)	$3FDF (IRQ/RAM)
MASK OPTION REGISTER(S)	NO	NO	$1FF0-1	NO	NO	NO	$1FF0-1	NO	NO	NO	NO	NO	$3FF0-1
PORTB KEYSCAN (PULLUP/ INTERRUPT)	NO	YES MASK OPTION	YES MOR SELECTABLE	NO	YES MASK OPTION	NO	YES MOR SELECTABLE	YES MASK OPTION	YES MASK OPTION	NO	YES MASK OPTION	NO	YES MOR SELECTABLE
PC7 DRIVE	STANDARD	HIGH CURRENT	HIGH CURRENT	STANDARD	HIGH CURRENT	STANDARD	HIGH CURRENT	HIGH CURRENT	HIGH CURRENT	STANDARD	HIGH CURRENT	STANDARD	HIGH CURRENT
PORT D	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 INPUT ONLY	PD7, 5-0 BIDIRECTIONAL	PD7, 5-0 BIDIRECTIONAL	PD7, 5-0 BIDIRECTIONAL	PD7, 5-0 BIDIRECTIONAL
COP	NO	YES	YES	NO	YES	YES	TWO TYPES	YES	YES	YES	**YES**	**YES**	**TWO TYPES**
COP ENABLE	—	MASK OPTION	MOR	—	MASK OPTION	SOFTWARE	SOFTWARE+ MOR	MASK OPTION	MASK OPTION	SOFTWARE	**SOFTWARE**	**SOFTWARE**	**SOFTWARE+ MOR**
COP TIMEOUT	—	64 ms (@4 MHz osc)	64 ms (@4 MHz osc)	—	64 ms (@4 MHz osc)	SOFTWARE SELECTABLE	SOFTWARE+ MOR SELECTABLE	64 ms (@4 MHz osc)	64 ms (@4MHz osc)	SOFTWARE SELECTABLE	SOFTWARE SELECTABLE	SOFTWARE SELECTABLE	SOFTWARE+ MOR SELECTABLE
COP CLEAR	—	CLR $1FF0	CLR $1FF0	—	CLR $1FF0	WRITE $55/$AA TO $001D	WRITE $55/$AA TO $001D OR CLR $1FF0	CLR $3FF0	CLR $3FF0	WRITE $55/$AA TO $001D	WRITE $55/$AA TO $001D	WRITE $55/$AA TO $001D	WRITE $55/$AA TO $001D OR CLR $3FF0
CLOCK MONITOR	NO	NO	NO	NO	NO	YES	YES	NO	NO	YES	YES	YES	YES (C9A MODE)
ACTIVE RESET	NO	NO	NO	NO	NO	COP/CLOCK MONITOR	PROGRAMMABLE COP/CLOCK MONITOR	NO	NO	POR/COP/ CLOCK MONITOR	POR/COP/ CLOCK MONITOR	POR/COP/ CLOCK MONITOR	POR/C9A COP/ CLOCK MONITOR
STOP DISABLE	NO	MASK OPTION	MOR SELECTABLE	NO	MASK OPTION	NO	MOR SELECTABLE	MASK OPTION	MASK OPTION	NO	NO	NO	MOR SELECTABLE (C12A MODE)

NOTES:

1. The expanded RAM map (from $30–$4F and $100–$15F) available on the OTP devices MC68HC705C8 and MC68HC705C8A is not available on the ROM devices MC68HC05C8 and MC68HC05C8A.
2. The programmable COP available on the MC68HC705C8 and MC68HC705C8A is not available on the MC68HC05C8A. For ROM compatibility, use the non-programmable COP.

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