SIEMENS

1M x 16-Bit EDO- Dynamic RAM (1k & 4k -Refresh)

HYB3116165BSJ/BST(L)-50/-60/-70
HYB3118165BSJ/BST(L)-50/-60/-70

Advanced Information

- 1 048 576 words by 16-bit organization
- 0 to 70 °C operating temperature
- Performance:

		-50	-60	-70	
t_{RAC}	$\overline{RAS}$ access time	50	60	70	ns
t_{CAC}	$\overline{CAS}$ access time	13	15	20	ns
t_{AA}	Access time from address	25	30	35	ns
t_{RC}	Read/Write cycle time	84	104	124	ns
t_{HPC}	Hyper page mode (EDO) cycle time	20	25	30	ns

- Single + 3.3 V (± 0.3 V) supply
- Low power dissipation
  max. 720 active mW (HYB3118165BSJ/BST-50)
  max. 648 active mW (HYB3118165BSJ/BST-60)
  max. 576 active mW (HYB3118165BSJ/BST-70)
  max. 360 active mW (HYB3116165BSJ/BST-50)
  max. 324 active mW (HYB3116165BSJ/BST-60)
  max. 288 active mW (HYB3116165BSJ/BST-70)
  7.2 mW standby (LV-TTL)
  3.6 mW standby (LV-CMOS)
  720 µW standby for L-version
- Output unlatched at cycle end allows two-dimensional chip selection
- Read, write, read-modify-write, $\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only refresh, hidden refresh, self refresh
- Hyper page mode (EDO) capability
- 2 $\overline{CAS}$ / 1 $\overline{WE}$
- All inputs, outputs and clocks fully LV-TTL-compatible
- 1024 refresh cycles / 16 ms for HYB 3118165BSJ
- 4096 refresh cycles / 64 ms for HYB 3116165BSJ
- Plastic Package: P-SOJ-42-1 400 mil
  P-TSOPII-50/44-1 400mil

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- Plastic Package: P-SOJ-42-1 400 mil
  P-TSOPII-50/44-1 400mil

The HYB 3116(8)165BSJ/BST is a 16 MBit dynamic RAM organized as 1 048 576 words by 16 bits. The HYB 3116(8)165BSJ/BST utilizes a submicron CMOS silicon gate process technology, as well as advanced circuit techniques to provide wide operating margins, both internally and for the system user. Multiplexed address inputs permit the HYB 3116(8)165BSJ/BST to be packaged in standard SOJ-42 and TSOPII-50/44 plastic package with 400mil width. These packages provide high system bit densities and are compatible with commonly used automatic testing and insertion equipment. System-oriented features include single + 3.3 V (± 0.3 V) power supply, direct interfacing with high-performance logic device families. The HYB3116166BSTL parts have a very low power „sleep mode“ supported by Self Refresh.

Ordering Information

Type	Ordering Code	Package	Descriptions
HYB 3116165BSJ-50	on request	P-SOJ-42 400 mil	DRAM (access time 50 ns)
HYB 3116165BSJ-60	on request	P-SOJ-42 400 mil	DRAM (access time 60 ns)
HYB 3116165BSJ-70	on request	P-SOJ-42 400 mil	DRAM (access time 70 ns)
HYB 3118165BSJ-50	Q67100-Q1159	P-SOJ-42 400 mil	DRAM (access time 50 ns)
HYB 3118165BSJ-60	Q67100-Q1160	P-SOJ-42 400 mil	DRAM (access time 60 ns)
HYB 3118165BSJ-70		P-SOJ-42 400 mil	DRAM (access time 70 ns)
HYB 3116165BST-50	Q67100-Q1190	P-TSOPII-50/44 400 mil	DRAM (access time 50 ns)
HYB 3116165BST-60	Q67100-Q1192	P-TSOPII-50/44 400 mil	DRAM (access time 60 ns)
HYB 3116165BST-70		P-TSOPII-50/44 400 mil	DRAM (access time 70 ns)
HYB 3118165BST-50	Q67100-Q1167	P-TSOPII-50/44 400 mil	DRAM (access time 50 ns)
HYB 3118165BST-60	Q67100-Q1168	P-TSOPII-50/44 400 mil	DRAM (access time 60 ns)
HYB 3118165BST-70	Q67100-Q1188	P-TSOPII-50/44 400 mil	DRAM (access time 70 ns)

Pin Names

A0 to A9	Row Address Inputs for 1k-refresh version HYB3118165BSJ/BST
A0 to A9	Column Addess Inputs for 1k-refresh version HYB3118165BSJ/BST
A0 to A11	Row Address Inputs for 4k-refresh version HYB3116165BSJ/BST
A0 to A7	Column Address Inputs for 4k-refresh version HYB3116165BSJ/BST
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	not connected

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Ordering Information

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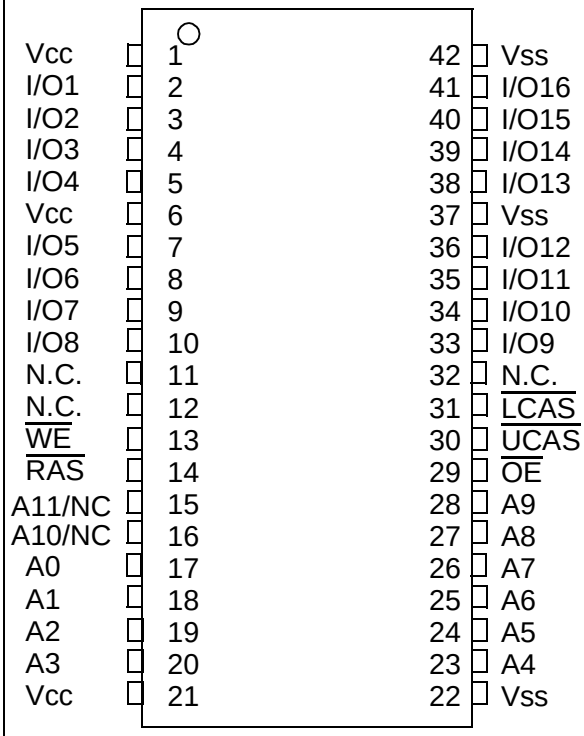
HYB 3116165BSJ-50	on request	P-SOJ-42 400 mil	DRAM (access time 50 ns)
HYB 3116165BSJ-60	on request	P-SOJ-42 400 mil	DRAM (access time 60 ns)
HYB 3116165BSJ-70	on request	P-SOJ-42 400 mil	DRAM (access time 70 ns)
HYB 3118165BSJ-50	Q67100-Q1159	P-SOJ-42 400 mil	DRAM (access time 50 ns)
HYB 3118165BSJ-60	Q67100-Q1160	P-SOJ-42 400 mil	DRAM (access time 60 ns)
HYB 3118165BSJ-70		P-SOJ-42 400 mil	DRAM (access time 70 ns)
HYB 3116165BST-50	Q67100-Q1190	P-TSOPII-50/44 400 mil	DRAM (access time 50 ns)
HYB 3116165BST-60	Q67100-Q1192	P-TSOPII-50/44 400 mil	DRAM (access time 60 ns)
HYB 3116165BST-70		P-TSOPII-50/44 400 mil	DRAM (access time 70 ns)
HYB 3118165BST-50	Q67100-Q1167	P-TSOPII-50/44 400 mil	DRAM (access time 50 ns)
HYB 3118165BST-60	Q67100-Q1168	P-TSOPII-50/44 400 mil	DRAM (access time 60 ns)
HYB 3118165BST-70	Q67100-Q1188	P-TSOPII-50/44 400 mil	DRAM (access time 70 ns)

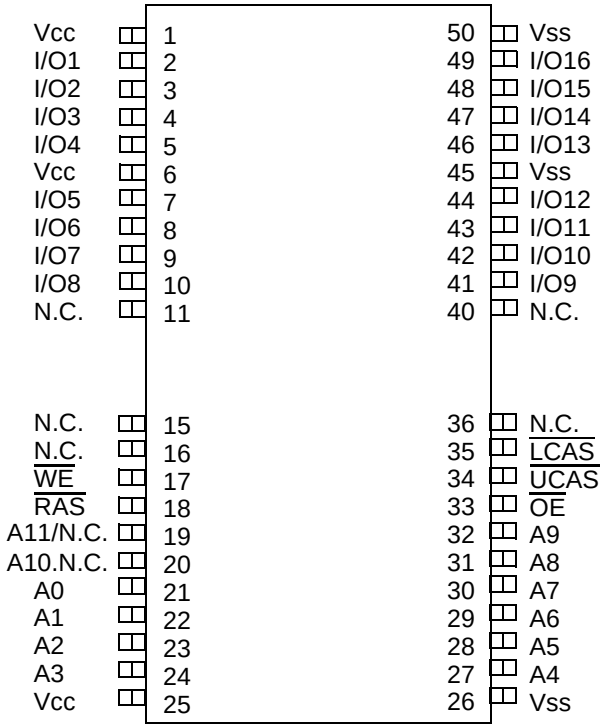
Pin Names

A0 to A9	Row Address Inputs for 1k-refresh version HYB3118165BSJ/BST
A0 to A9	Column Addess Inputs for 1k-refresh version HYB3118165BSJ/BST
A0 to A11	Row Address Inputs for 4k-refresh version HYB3116165BSJ/BST
A0 to A7	Column Address Inputs for 4k-refresh version HYB3116165BSJ/BST
$\overline{RAS}$	Row Address Strobe
$\overline{OE}$	Output Enable
I/O1-I/O16	Data Input/Output
$\overline{UCAS}$	Upper Column Address Strobe
$\overline{LCAS}$	Lower Column Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power Supply (+ 3.3 V)
V_{SS}	Ground (0 V)
N.C.	not connected

P-SOJ-42 (400 mil)



P-TSOPII-50/44 (400mil)

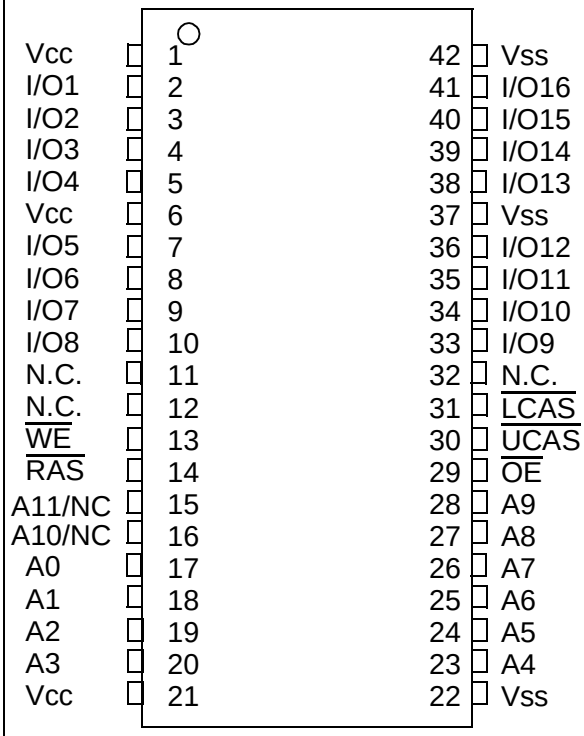


*) A11 and A10 are not connected for HYB3118165BSJ/BST (1k-refresh version)

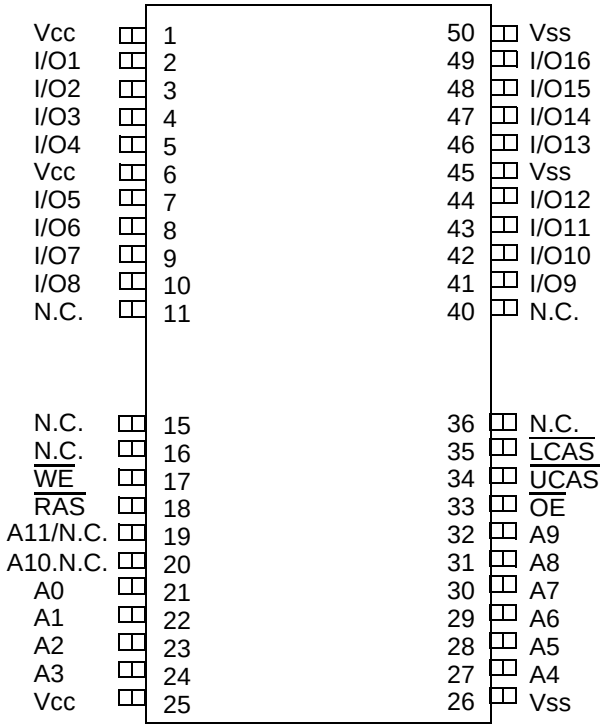
Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O1-I/O8	I/O9-I/O16	Operation
H	H	H	H	H	High-Z	High-Z	Standby
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	NOP

P-SOJ-42 (400 mil)



P-TSOPII-50/44 (400mil)



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Truth Table

$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O1-I/O8	I/O9-I/O16	Operation
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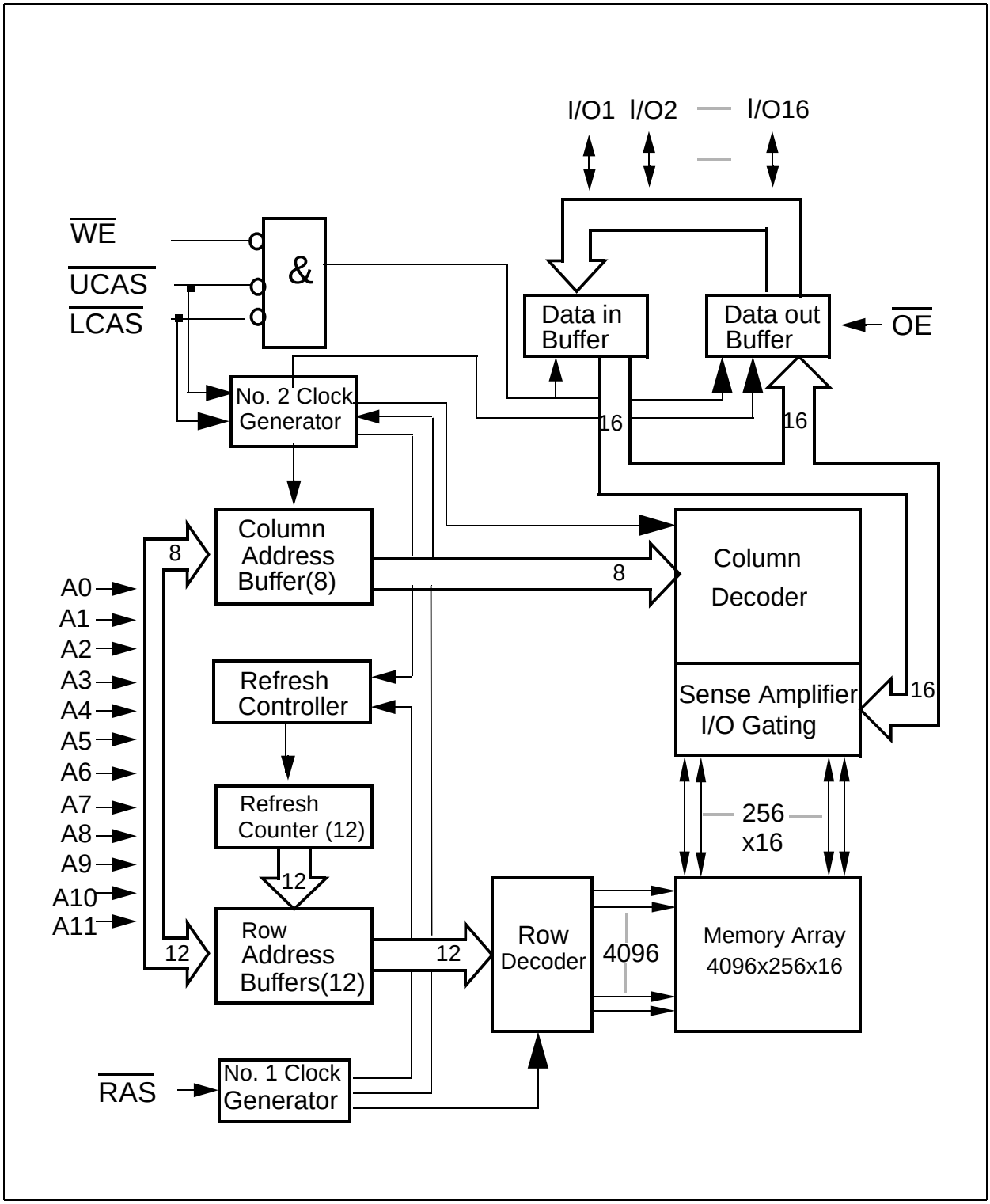
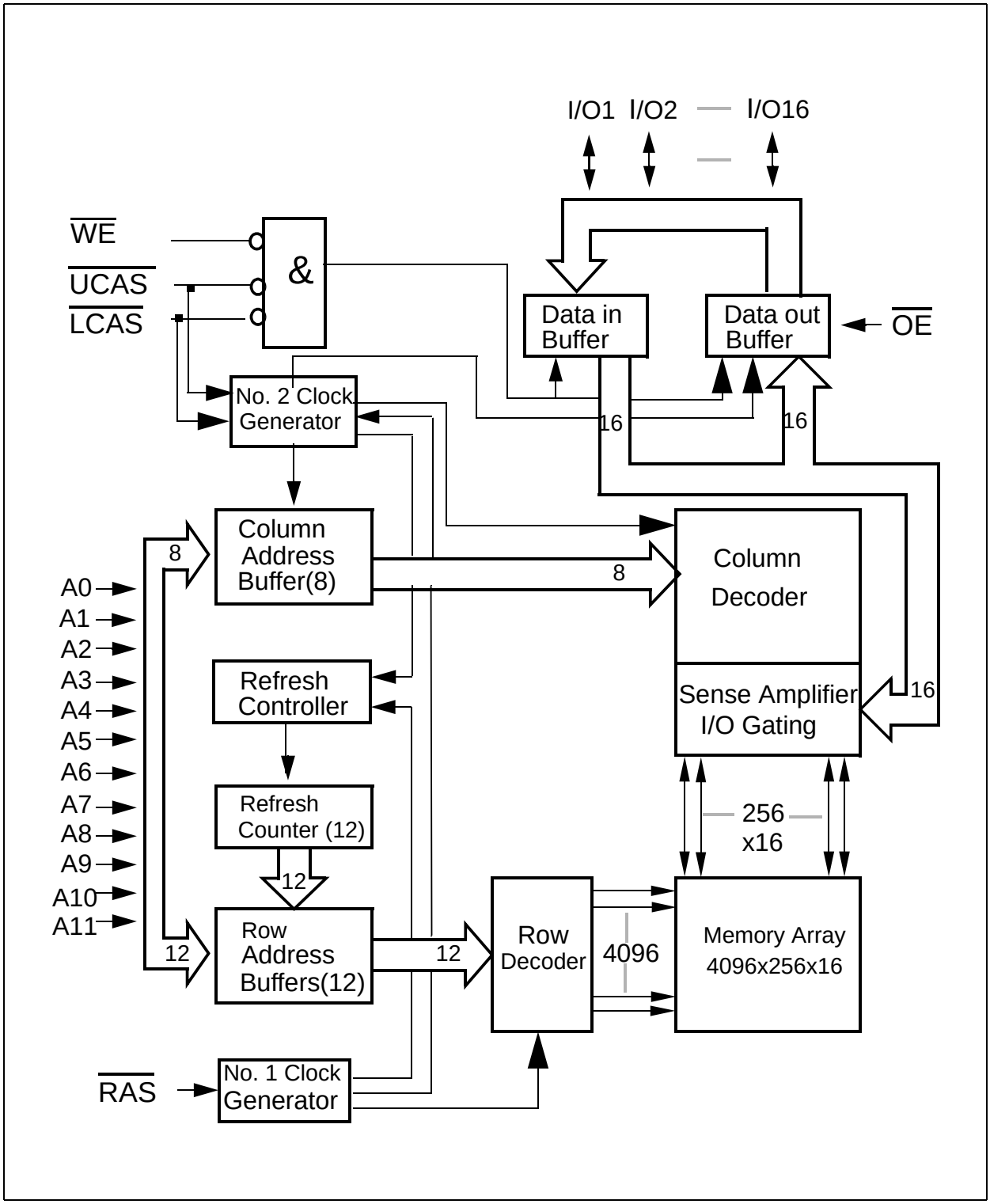
L	H	H	H	H	High-Z	High-Z	Refresh
L	L	H	H	L	Dout	High-Z	Lower byte read
L	H	L	H	L	High-Z	Dout	Upper byte read
L	L	L	H	L	Dout	Dout	Word read
L	L	H	L	H	Din	Don't care	Lower byte write
L	H	L	L	H	Don't care	Din	Upper byte write
L	L	L	L	H	Din	Din	Word write
L	L	L	H	H	High-Z	High-Z	NOP



Block Diagram for HYB 3116165BSJ



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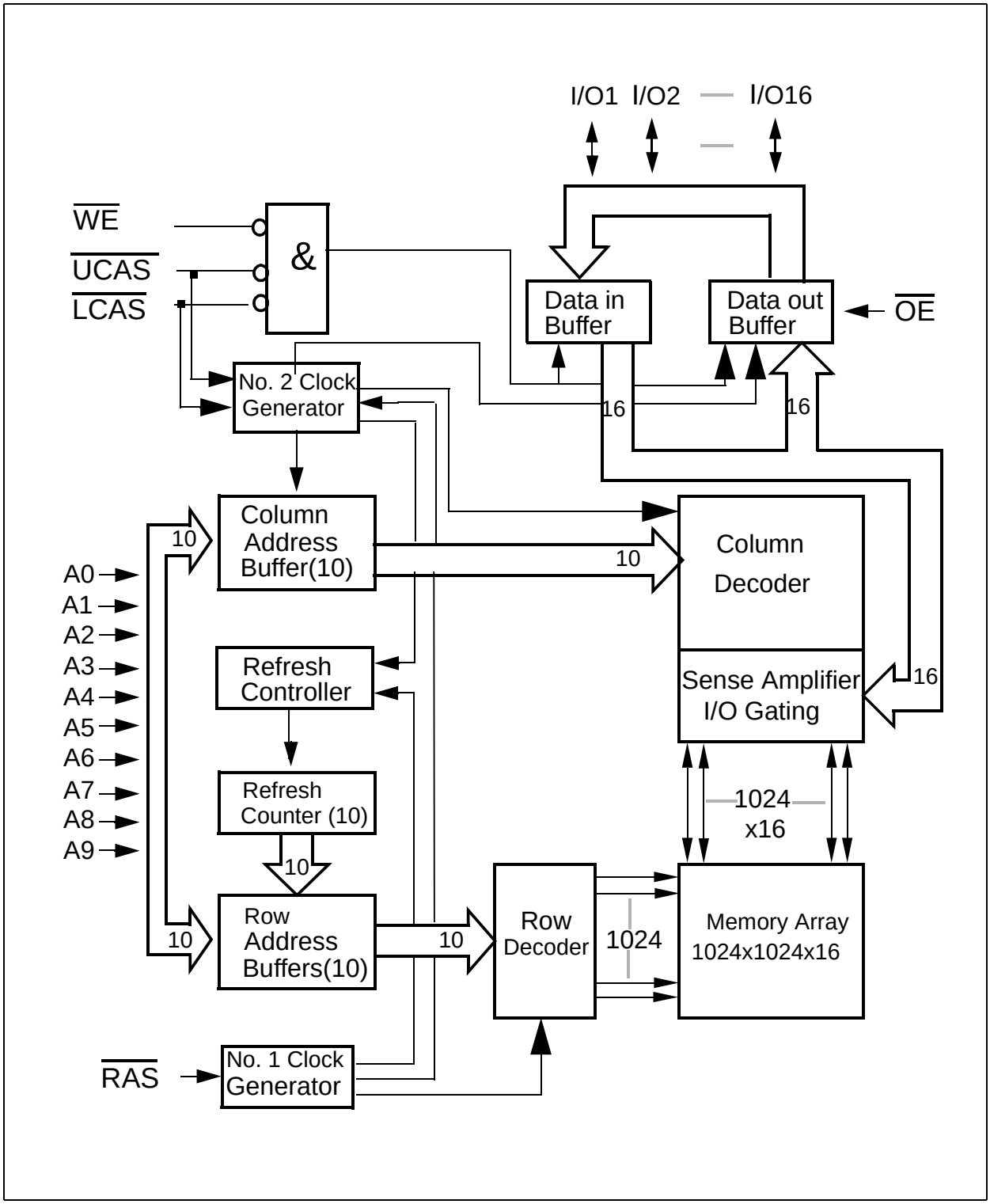

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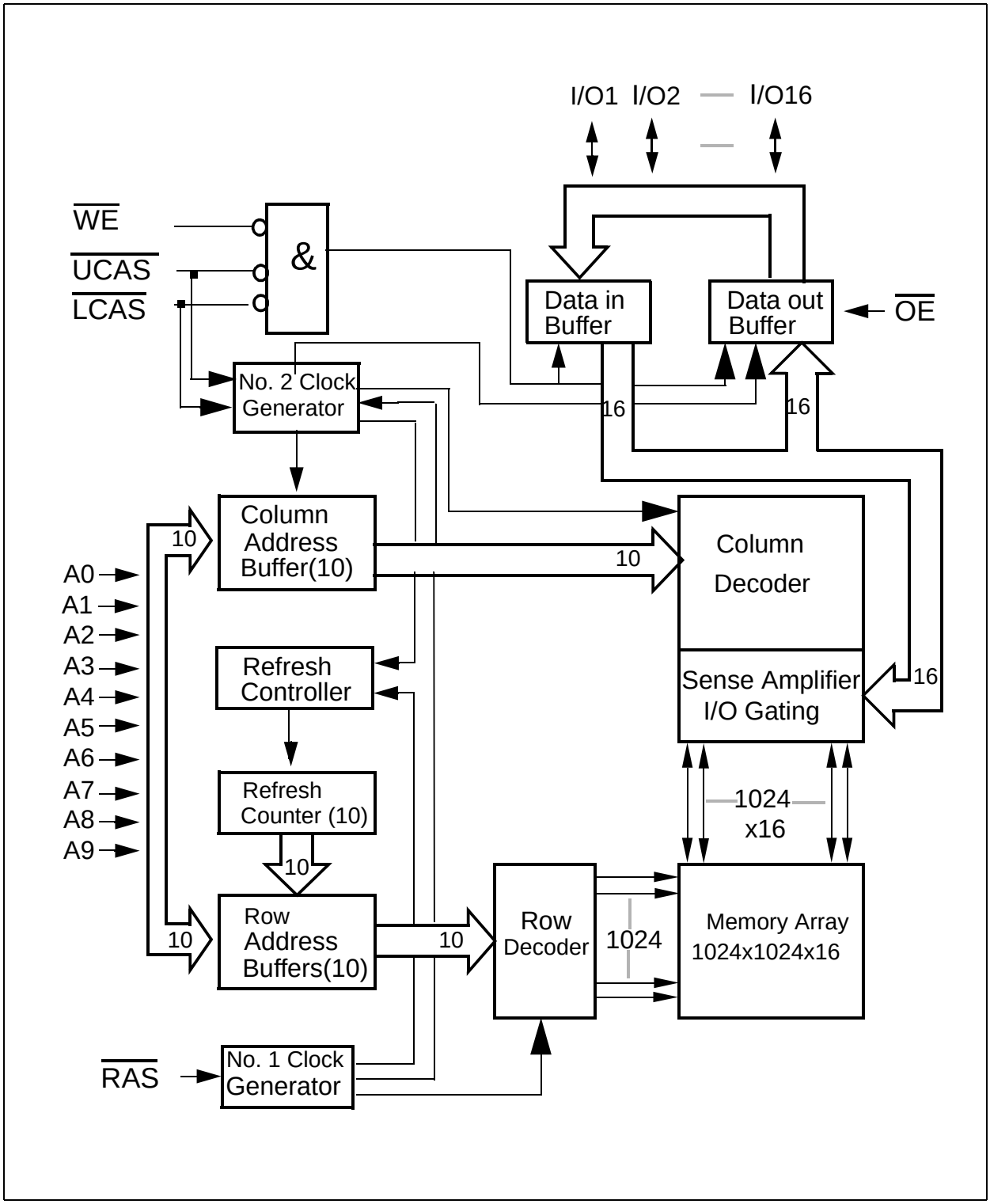


Block Diagram for HYB 3118165BSJ

Absolute Maximum Ratings

Operating temperature range .....0 to 70 °C

Storage temperature range.....– 55 to 150 ℃

Soldering time.....10 s

Input/output voltage .....-0.5 to min (Vcc+0.5,4.6) V

Power supply voltage.....-0.5 V to 4.6 V

Power dissipation..... 1.0 W

Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (values in brackets for HYB3116165BSJ)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = – 100 µA)	V_{OH}	Vcc-0.2	–	V	1)
CMOS Output low voltage (I_{OUT} = 100 µA)	V_{OL}	–	0.2	V	1)
Input leakage current,any input (0 V ≤ V_{IH} ≤ Vcc + 0.3V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ Vcc + 0.3V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	I_{CC1}	 – – –	 200(100) 180 (90) 160 (80)	 mA mA mA	 2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

Absolute Maximum Ratings

Operating temperature range .....0 to 70 °C

Storage temperature range.....– 55 to 150 ℃

Soldering time.....10 s

Input/output voltage .....-0.5 to min (Vcc+0.5,4.6) V

Power supply voltage.....-0.5 V to 4.6 V

Power dissipation..... 1.0 W

Data out current (short circuit) ..... 50 mA

Note:

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (values in brackets for HYB3116165BSJ)

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input high voltage	V_{IH}	2.0	Vcc+0.5	V	1)
Input low voltage	V_{IL}	– 0.5	0.8	V	1)
TTL Output high voltage (I_{OUT} = – 2 mA)	V_{OH}	2.4	–	V	1)
TTL Output low voltage (I_{OUT} = 2 mA)	V_{OL}	–	0.4	V	1)
CMOS Output high voltage (I_{OUT} = – 100 µA)	V_{OH}	Vcc-0.2	–	V	1)
CMOS Output low voltage (I_{OUT} = 100 µA)	V_{OL}	–	0.2	V	1)
Input leakage current,any input (0 V ≤ V_{IH} ≤ Vcc + 0.3V, all other pins = 0 V)	$I_{I(L)}$	– 10	10	µA	1)
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ Vcc + 0.3V)	$I_{O(L)}$	– 10	10	µA	1)
Average V_{CC} supply current: -50 ns version -60 ns version -70 ns version ($\overline{RAS}$, $\overline{CAS}$, address cycling, t_{RC} = t_{RC} min.)	I_{CC1}	 – – –	 200(100) 180 (90) 160 (80)	 mA mA mA	 2) 3) 4) 2) 3) 4) 2) 3) 4)
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	–	2	mA	–

DC Characteristics (values in brackets for HYB3116165BSJ) *(cont'd)*

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: -50 ns version	I_{CC3}	–	200(100)	mA	2) 4)
-60 ns version		–	180 (90)	mA	2) 4)
-70 ns version		–	160 (80)	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					
Average V_{CC} supply current, during hyper page mode EDO): -50 ns version	I_{CC4}	–	90 (70)	mA	2) 3) 4)
-60 ns version		–	75 (55)	mA	2) 3) 4)
-70 ns version		–	60 (45)	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
			200	µA	L-version
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	200(100)	mA	2) 4)
-60 ns version		–	180 (90)	mA	2) 4)
-70 ns version		–	160 (80)	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current	I_{CC7}	–	1	mA	
			250	µA	L-version
(CBR cycle with tRAS>TRASSmin., $\overline{CAS}$ held low, $\overline{WE}$=Vcc-0.2V, Address and Din=Vcc--0.2V or 0.2V)					

Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

DC Characteristics (values in brackets for HYB3116165BSJ) *(cont'd)*

T_A = 0 to 70 °C, V_{SS} = 0 V, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Average V_{CC} supply current, during $\overline{RAS}$-only refresh cycles: -50 ns version	I_{CC3}	–	200(100)	mA	2) 4)
-60 ns version		–	180 (90)	mA	2) 4)
-70 ns version		–	160 (80)	mA	2) 4)
($\overline{RAS}$ cycling: $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min.)					
Average V_{CC} supply current, during hyper page mode EDO): -50 ns version	I_{CC4}	–	90 (70)	mA	2) 3) 4)
-60 ns version		–	75 (55)	mA	2) 3) 4)
-70 ns version		–	60 (45)	mA	2) 3) 4)
($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, address cycling, t_{PC} = t_{PC} min.)					
Standby V_{CC} supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	–	1	mA	1)
			200	µA	L-version
Average V_{CC} supply current, during $\overline{CAS}$-before-RAS refresh mode: -50 ns version	I_{CC6}	–	200(100)	mA	2) 4)
-60 ns version		–	180 (90)	mA	2) 4)
-70 ns version		–	160 (80)	mA	2) 4)
($\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = t_{RC} min.)					
Average Self Refresh Current	I_{CC7}	–	1	mA	
			250	µA	L-version
(CBR cycle with tRAS>TRASSmin., $\overline{CAS}$ held low, $\overline{WE}$=Vcc-0.2V, Address and Din=Vcc--0.2V or 0.2V)					

Capacitance

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A11)	C_{I1}	–	5	pF
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	–	7	pF
I/O capacitance (I/O1-I/O16)	C_{IO}	–	7	pF

AC Characteristics [5][6] 16E

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
common parameters									
Random read or write cycle time	t_{RC}	84	–	104	–	124	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10k	10	10k	12	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	8	–	10	–	12	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	14	53	ns	
$\overline{RAS}$ to column address delay	t_{RAD}	10	25	12	30	12	35	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	17	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50	–	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	7
Refresh period for HYB3116165	t_{REF}	–	64	–	64	–	64	ms	
Refresh period for HYB3118165	t_{REF}	–	16	–	16	–	16	ms	
Refresh period for L-versions	t_{REF}	–	256	–	256	–	256	ms	
Read Cycle									
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	17	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	t_{OEA}	–	13	–	15	–	17	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	ns	8

AC Characteristics [5][6] 16E

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
common parameters									
Random read or write cycle time	t_{RC}	84	–	104	–	124	–	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	–	40	–	50	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10k	60	10k	70	10k	ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10k	10	10k	12	10k	ns	
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	8	–	10	–	10	–	ns	
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	8	–	10	–	12	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	14	53	ns	
$\overline{RAS}$ to column address delay	t_{RAD}	10	25	12	30	12	35	ns	
$\overline{RAS}$ hold time	t_{RSH}	13		15	–	17	–	ns	
$\overline{CAS}$ hold time	t_{CSH}	40		50	–	60	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	7
Refresh period for HYB3116165	t_{REF}	–	64	–	64	–	64	ms	
Refresh period for HYB3118165	t_{REF}	–	16	–	16	–	16	ms	
Refresh period for L-versions	t_{REF}	–	256	–	256	–	256	ms	
Read Cycle									
Access time from $\overline{RAS}$	t_{RAC}	–	50	–	60	–	70	ns	8, 9
Access time from $\overline{CAS}$	t_{CAC}	–	13	–	15	–	17	ns	8, 9
Access time from column address	t_{AA}	–	25	–	30	–	35	ns	8,10
$\overline{OE}$ access time	t_{OEA}	–	13	–	15	–	17	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	–	30	–	35	–	ns	
Read command setup time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	11
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	11
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	–	0	–	0	–	ns	8

AC Characteristics *(cont'd)* 5)6) 16E

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	17	ns	12
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	17	ns	12
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	0	–	ns	13
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	10	–	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	10	–	13	–	15	–	ns	14
Write Cycle									
Write command hold time	t_{WCH}	8	–	10	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	17	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	17	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	8	–	10	–	12	–	ns	16
Read-modify-Write Cycle									
Read-write cycle time	t_{RWC}	113	–	138	–	162	–	ns	
$\overline{RAS}$ to WE delay time	t_{RWD}	64	–	77	–	89	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	27	–	32	–	36	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	39	–	47	–	54	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	10	–	13	–	15	–	ns	
Hyper Page Mode (EDO) Cycle									
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	27	–	32	–	37	ns	7
Output data hold time	t_{COH}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width in EDO mode	t_{RAS}	50	200k	60	200k	70	200k	ns	

AC Characteristics *(cont'd)* 5)6) 16E

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
Output buffer turn-off delay	t_{OFF}	0	13	0	15	0	17	ns	12
Output turn-off delay from $\overline{OE}$	t_{OEZ}	0	13	0	15	0	17	ns	12
Data to $\overline{CAS}$ low delay	t_{DZC}	0	–	0	–	0	–	ns	13
Data to $\overline{OE}$ low delay	t_{DZO}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ high to data delay	t_{CDD}	10	–	13	–	15	–	ns	14
$\overline{OE}$ high to data delay	t_{ODD}	10	–	13	–	15	–	ns	14
Write Cycle									
Write command hold time	t_{WCH}	8	–	10	–	10	–	ns	
Write command pulse width	t_{WP}	8	–	10	–	10	–	ns	
Write command setup time	t_{WCS}	0	–	0	–	0	–	ns	15
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	–	15	–	17	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	–	15	–	17	–	ns	
Data setup time	t_{DS}	0	–	0	–	0	–	ns	16
Data hold time	t_{DH}	8	–	10	–	12	–	ns	16
Read-modify-Write Cycle									
Read-write cycle time	t_{RWC}	113	–	138	–	162	–	ns	
$\overline{RAS}$ to WE delay time	t_{RWD}	64	–	77	–	89	–	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	27	–	32	–	36	–	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	39	–	47	–	54	–	ns	15
$\overline{OE}$ command hold time	t_{OEH}	10	–	13	–	15	–	ns	
Hyper Page Mode (EDO) Cycle									
Hyper page mode (EDO) cycle time	t_{HPC}	20	–	25	–	30	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	8	–	10	–	10	–	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	27	–	32	–	37	ns	7
Output data hold time	t_{COH}	5	–	5	–	5	–	ns	
$\overline{RAS}$ pulse width in EDO mode	t_{RAS}	50	200k	60	200k	70	200k	ns	

AC Characteristics *(cont'd)* 5)6) 16E

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHPC}	27	–	32	–	37	–	ns	
Hyper Page Mode (EDO) Read-modify-Write Cycle									
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	58	–	68	–	77	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	41	–	49	–	56	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	10	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle									
$\overline{CAS}$ precharge time	t_{CPT}	35	–	40	–	40	–	ns	
Self Refresh Cycle									
$\overline{RAS}$ pulse width	t_{RASS}	100k	–	100k	–	100k	–	ns	17
$\overline{RAS}$ precharge	t_{RPS}	95	–	110	–	130	–	ns	17
$\overline{CAS}$ hold time	t_{CHS}	-50	–	-50	–	-50	–	ns	17

AC Characteristics *(cont'd)* 5)6) 16E

T_A = 0 to 70 °C, V_{CC} = 3.3 V ± 0.3 V, t_T = 2 ns

Parameter	Symbol	Limit Values						Unit	Note
		-50		-60		-70			
		min.	max.	min.	max.	min.	max.		
$\overline{CAS}$ precharge to $\overline{RAS}$ Delay	t_{RHPC}	27	–	32	–	37	–	ns	
Hyper Page Mode (EDO) Read-modify-Write Cycle									
Hyper page mode (EDO) read-write cycle time	t_{PRWC}	58	–	68	–	77	–	ns	
$\overline{CAS}$ precharge to $\overline{WE}$	t_{CPWD}	41	–	49	–	56	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle									
$\overline{CAS}$ setup time	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ hold time	t_{CHR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5	–	5	–	5	–	ns	
Write to $\overline{RAS}$ precharge time	t_{WRP}	10	–	10	–	10	–	ns	
Write hold time referenced to $\overline{RAS}$	t_{WRH}	10	–	10	–	10	–	ns	
$\overline{CAS}$-before-$\overline{RAS}$ Counter Test Cycle									
$\overline{CAS}$ precharge time	t_{CPT}	35	–	40	–	40	–	ns	
Self Refresh Cycle									
$\overline{RAS}$ pulse width	t_{RASS}	100k	–	100k	–	100k	–	ns	17
$\overline{RAS}$ precharge	t_{RPS}	95	–	110	–	130	–	ns	17
$\overline{CAS}$ hold time	t_{CHS}	-50	–	-50	–	-50	–	ns	17

Notes:

1) All voltages are referenced to VSS.

2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.

3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = VIL. In the case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle (tHPC).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume tT = 2 ns.

7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.

8) Measured with the specified current load and 100 pF at Vol = 0.8 V and Voh = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}, t_{OEA}. t_{CAC} is measured from tristate.

9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.

11) Either tRCH or tRRH must be satisfied for a read cycle.

12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

13) Either tDZC or tDZO must be satisfied.

14) Either tCDD or tODD must be satisfied.

15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

Notes:

1) All voltages are referenced to VSS.

2) ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.

3) ICC1 and ICC4 depend on output loading. Specified values are measured with the output open.

4) Address can be changed once or less while $\overline{RAS}$ = VIL. In the case of ICC4 it can be changed once or less during a hyper page mode (EDO) cycle (tHPC).

5) An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles of which at least one cycle has to be a refresh cycle, before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.

6) AC measurements assume tT = 2 ns.

7) VIH (min.) and VIL (max.) are reference levels for measuring timing of input signals. Transition times are also measured between VIH and VIL.

8) Measured with the specified current load and 100 pF at Vol = 0.8 V and Voh = 2.0 V. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{AA}, t_{CPA}, t_{OEA}. t_{CAC} is measured from tristate.

9) Operation within the tRCD (max.) limit ensures that tRAC (max.) can be met. tRCD (max.) is specified as a reference point only: If tRCD is greater than the specified tRCD (max.) limit, then access time is controlled by tCAC.

10) Operation within the tRAD (max.) limit ensures that tRAC (max.) can be met. tRAD (max.) is specified as a reference point only: If tRAD is greater than the specified tRAD (max.) limit, then access time is controlled by tAA.

11) Either tRCH or tRRH must be satisfied for a read cycle.

12) tOFF (max.) and tOEZ (max.) define the time at which the outputs achieve the open-circuit condition and are not referenced to output voltage levels.

13) Either tDZC or tDZO must be satisfied.

14) Either tCDD or tODD must be satisfied.

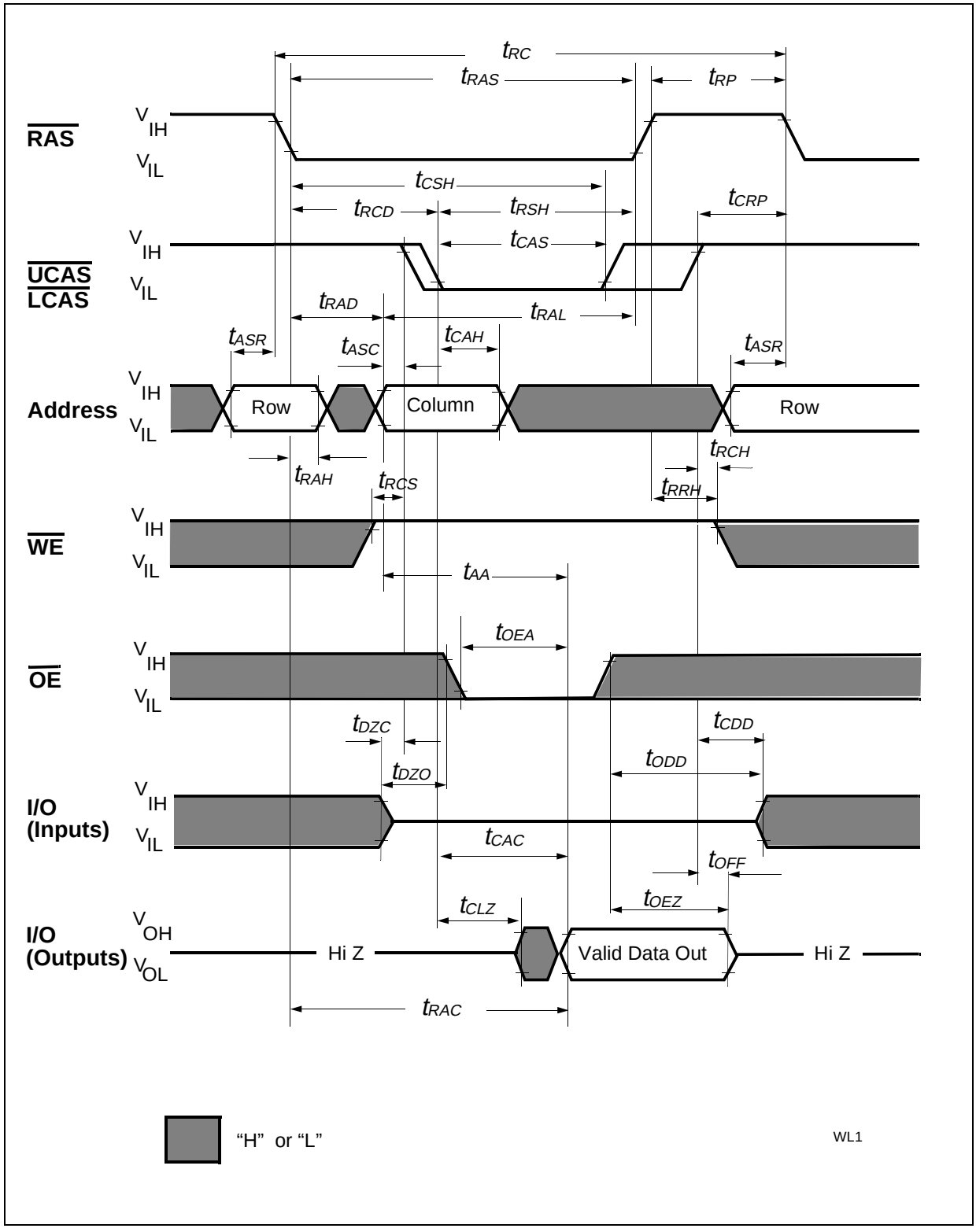
15) tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS > tWCS (min.), the cycle is an early write cycle and the I/O pin will remain open-circuit (high impedance) through the entire cycle; if tRWD > tRWD (min.), tCWD > tCWD (min.), tAWD > tAWD (min.) and tCPWD > tCPWD (min.) , the cycle is a read-write cycle and I/O pins will contain data read from the selected cells. If neither of the above sets of conditions is satisfied, the condition of the I/O pins (at access time) is indeterminate.

16) These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles and to the $\overline{WE}$ leading edge in read-write cycles.

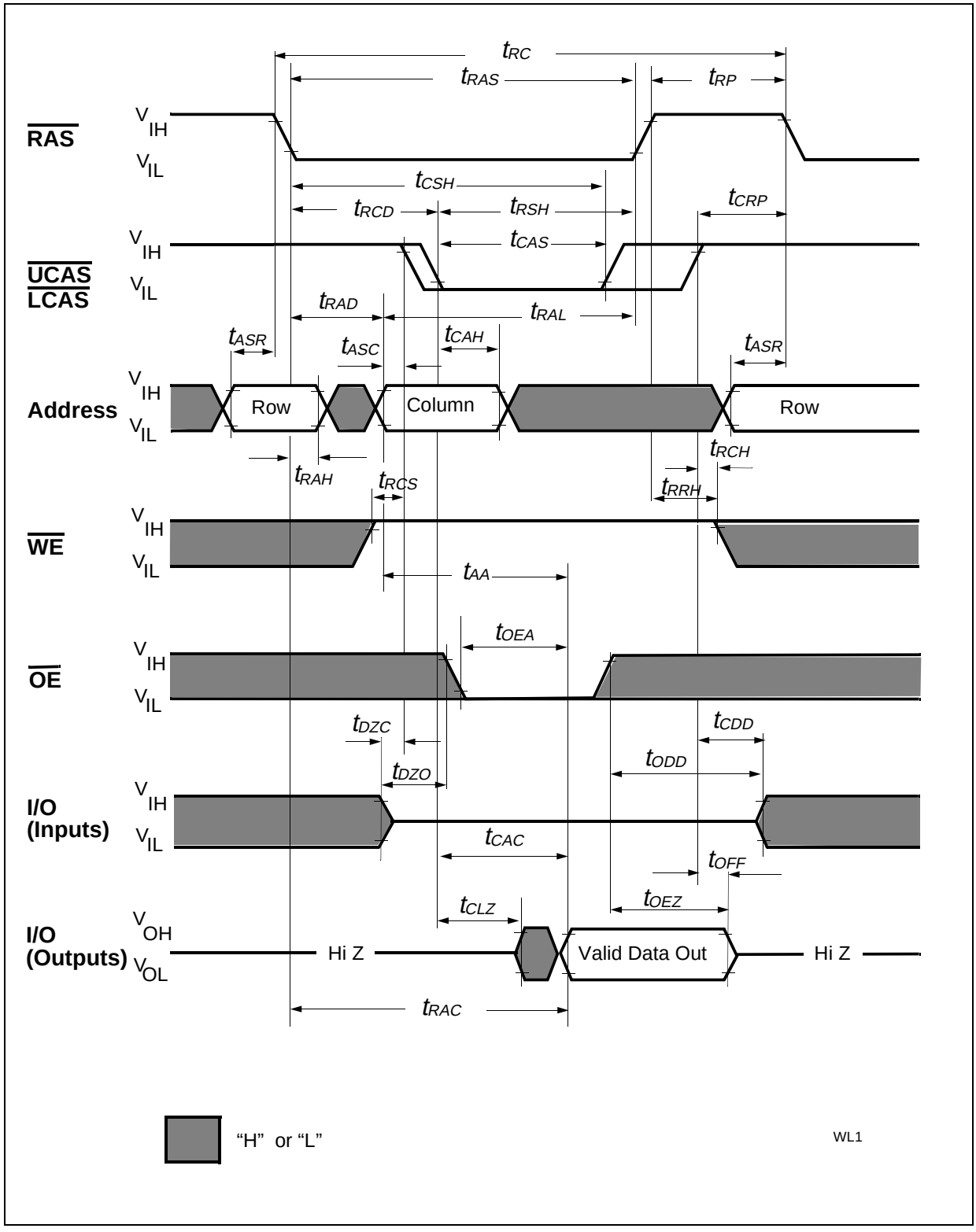
17) When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:

    If row addresses are being refreshed on an evenly distributed manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.

    If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
UCAS
LCAS
tRAD
tRAL
tASR
tASC
tCAH
tASR
Address
Row
Column
Row
tRAH
tRCS
tRCH
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O
(Inputs)
tCAC
tOFF
tOEZ
tCLZ
VOH
VOL
I/O
(Outputs)
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"
WL1

Read Cycle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tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
tCAS
UCAS
LCAS
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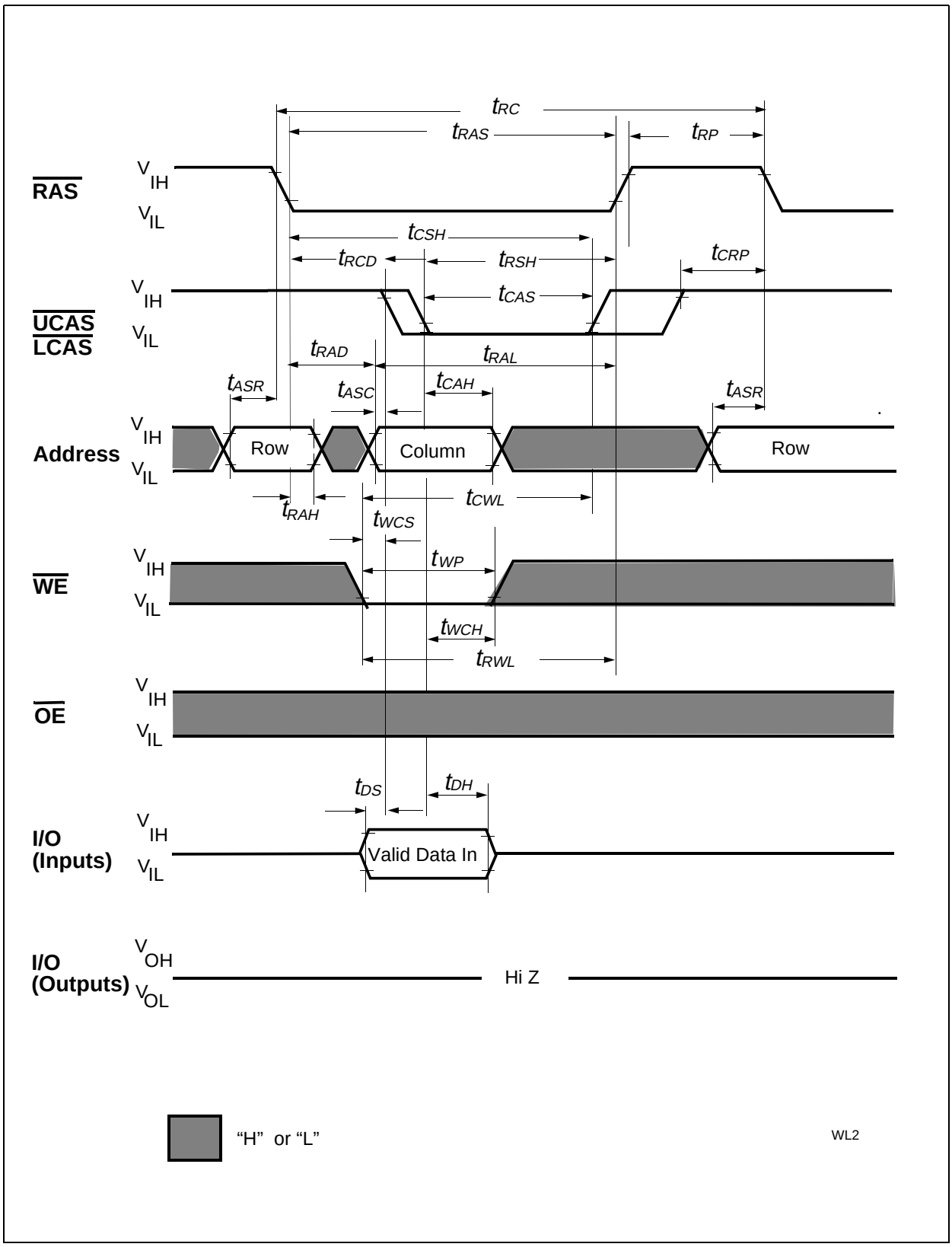
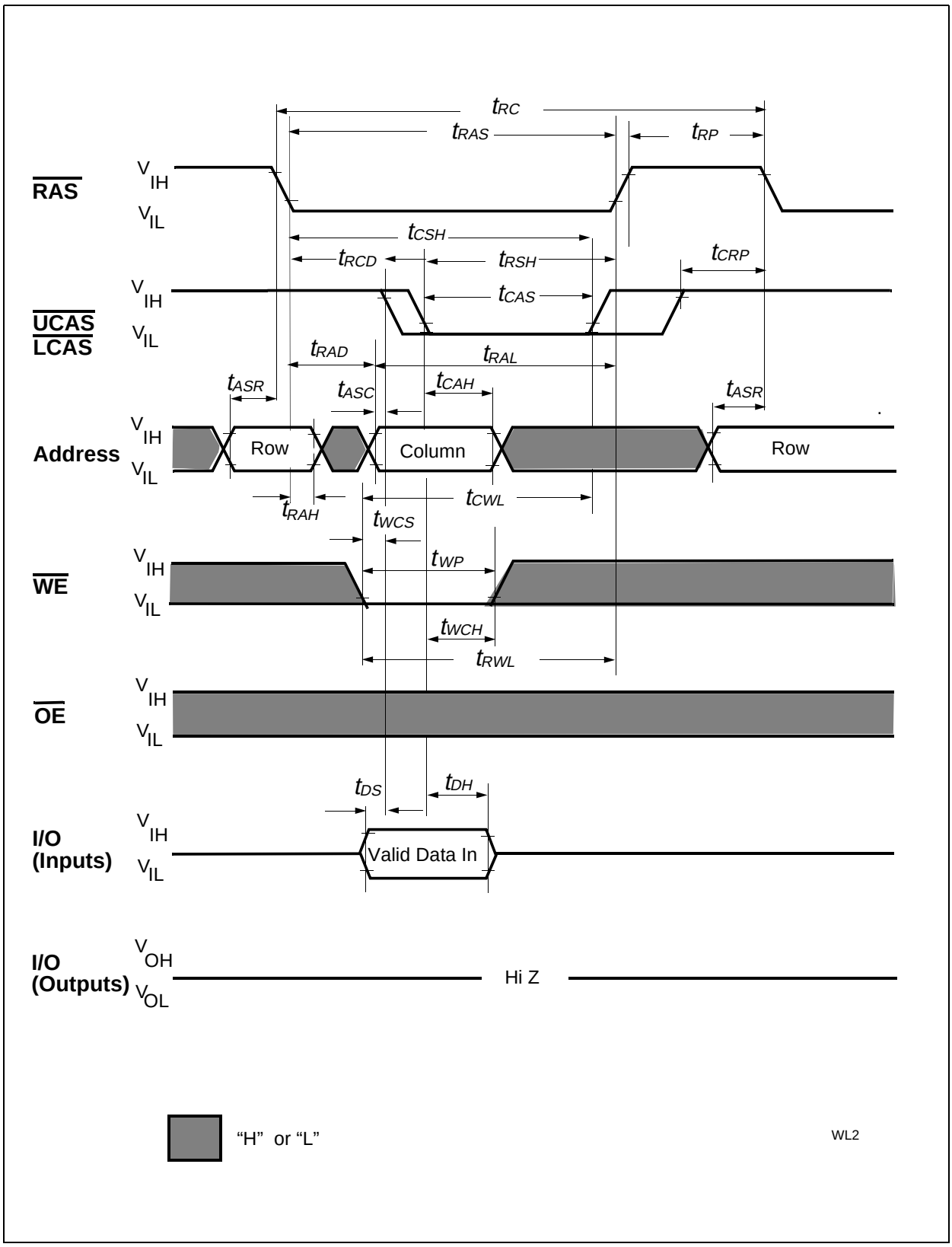
tASR
tASC
tCAH
tASR
Address
Row
Column
Row
tRAH
tRCS
tRCH
tRRH
WE
tAA
tOEA
OE
tDZC
tCDD
tDZO
tODD
I/O
(Inputs)
tCAC
tOFF
tOEZ
tCLZ
VOH
VOL
I/O
(Outputs)
Hi Z
Valid Data Out
Hi Z
tRAC
"H" or "L"
WL1

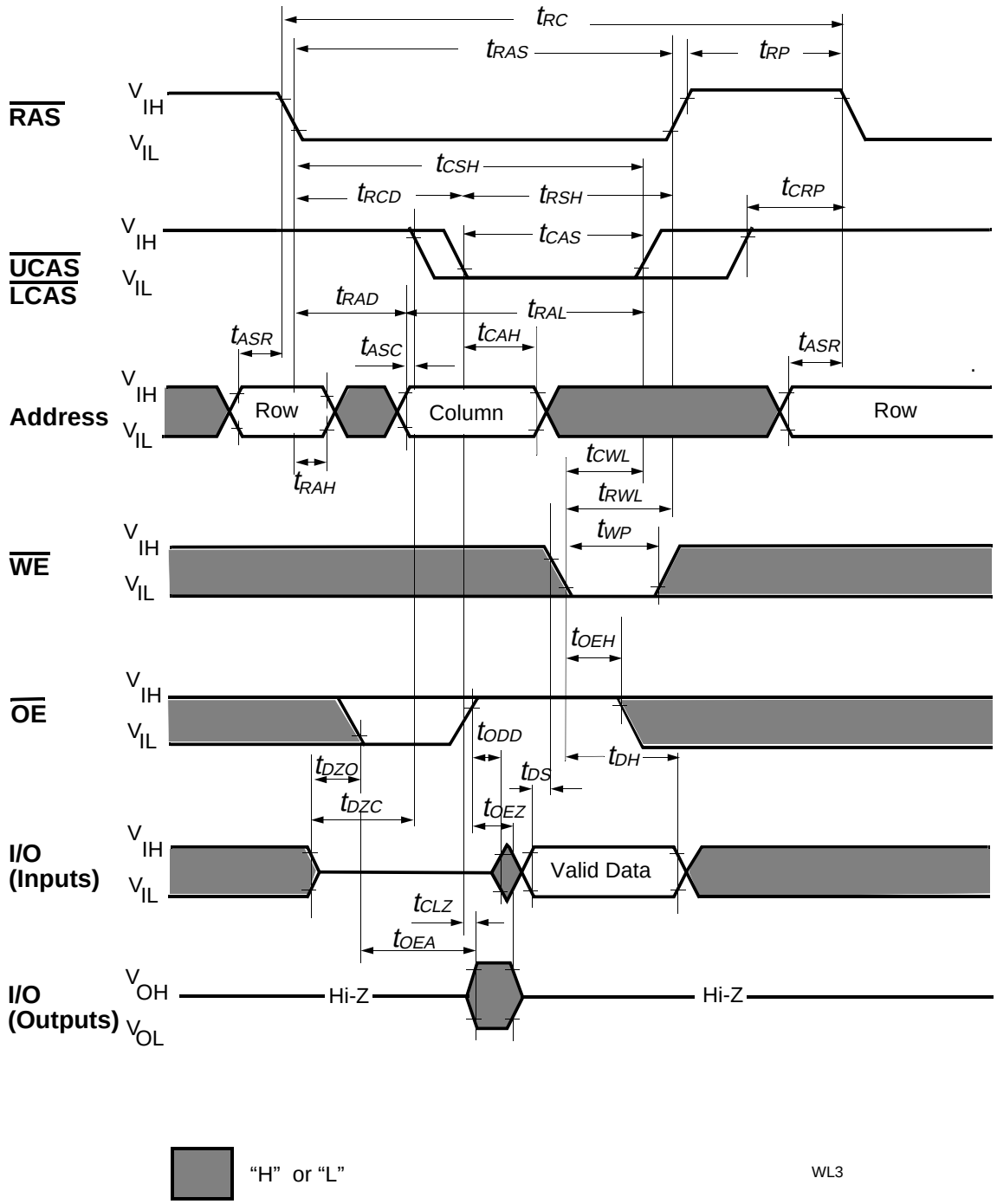
Read Cycle



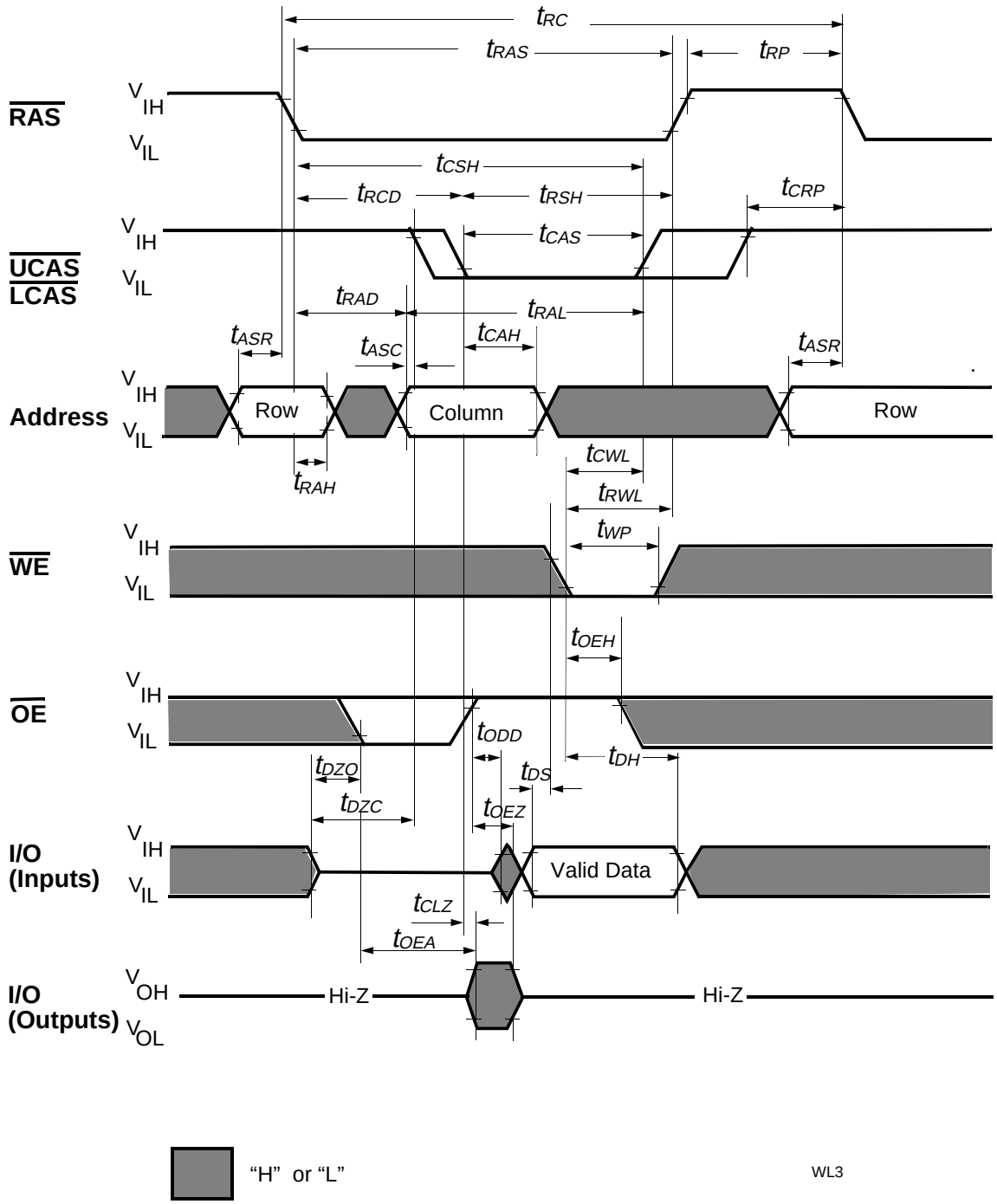
Write Cycle (Early Write)



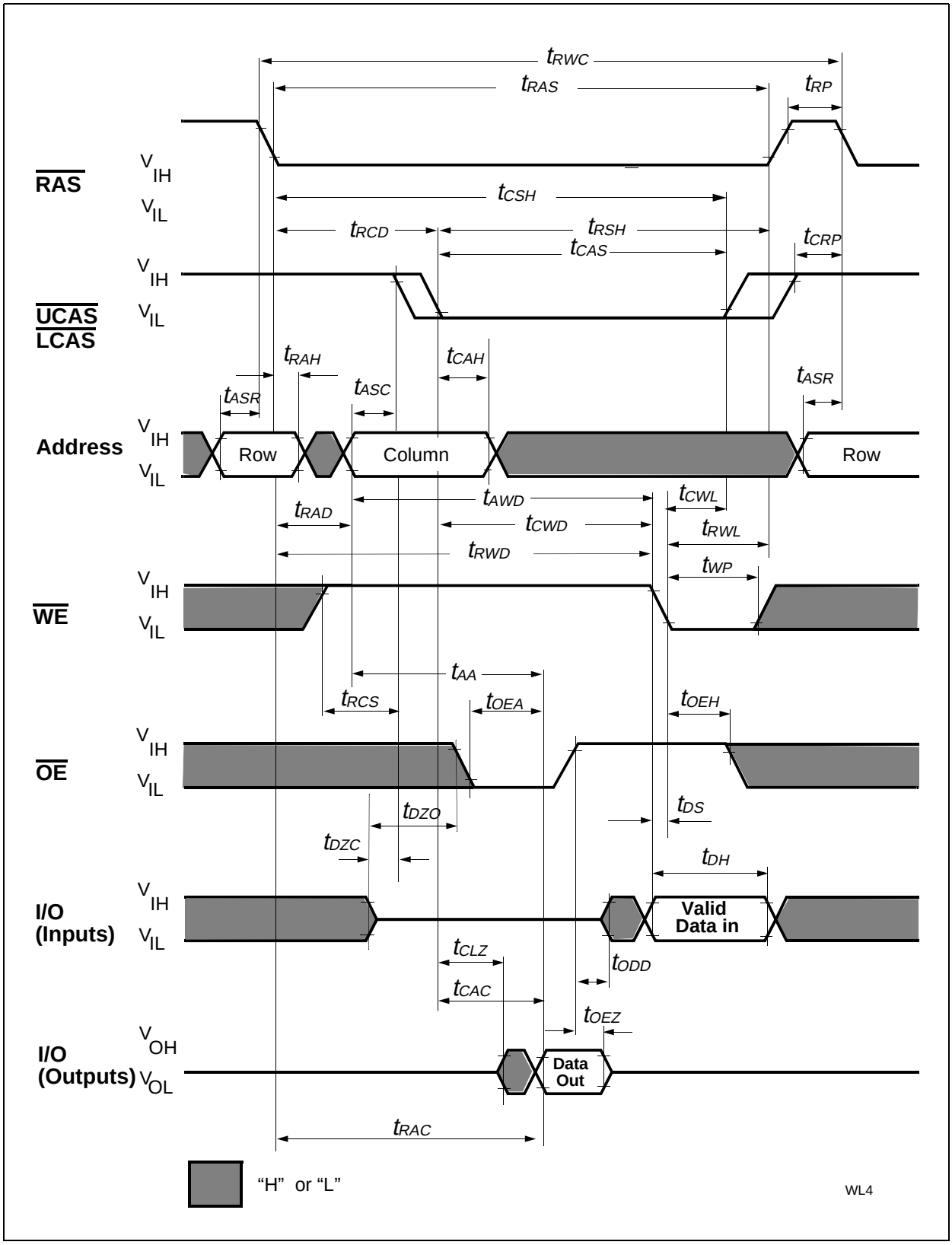
Write Cycle (Early Write)



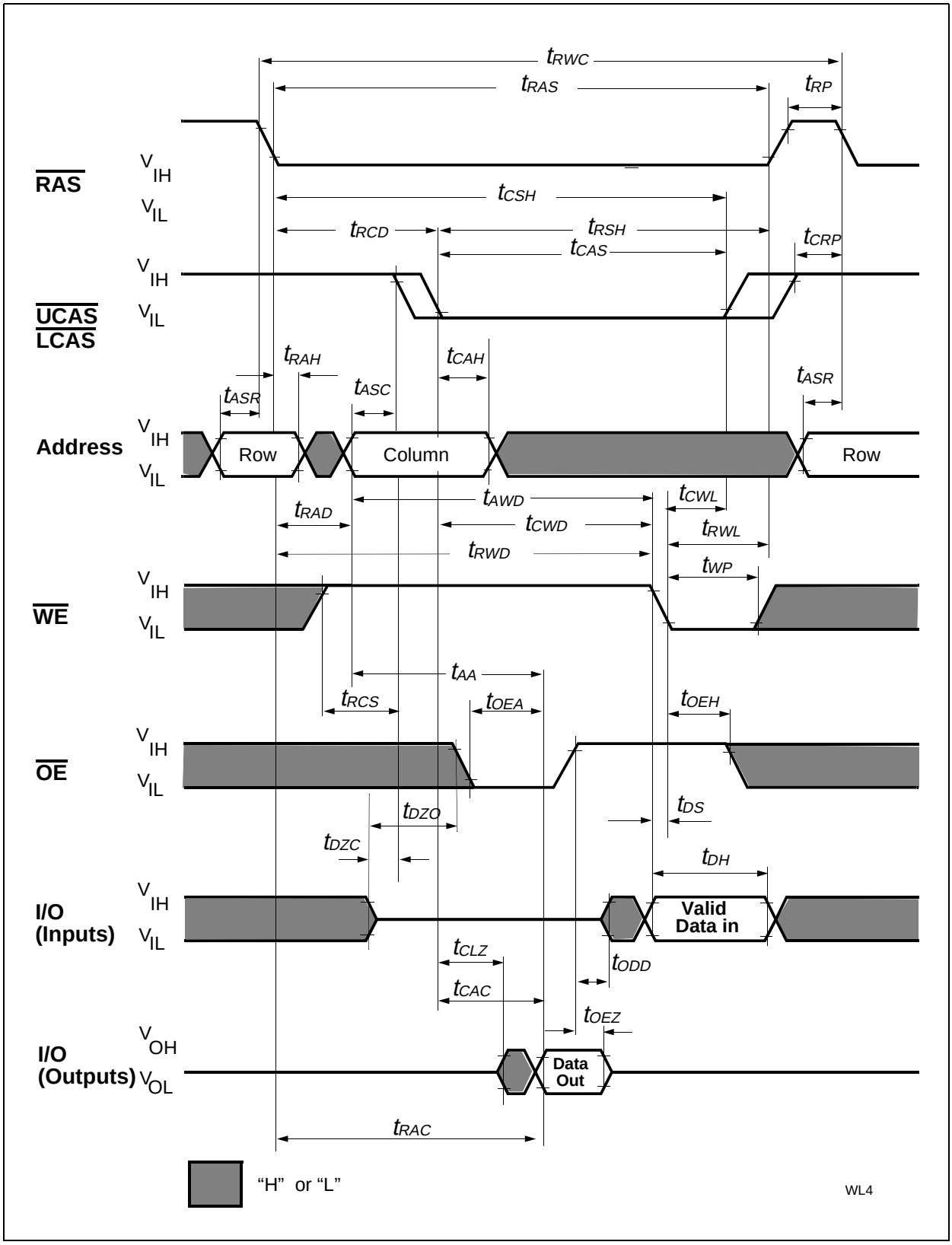
Write Cycle ($\overline{OE}$ Controlled Write)



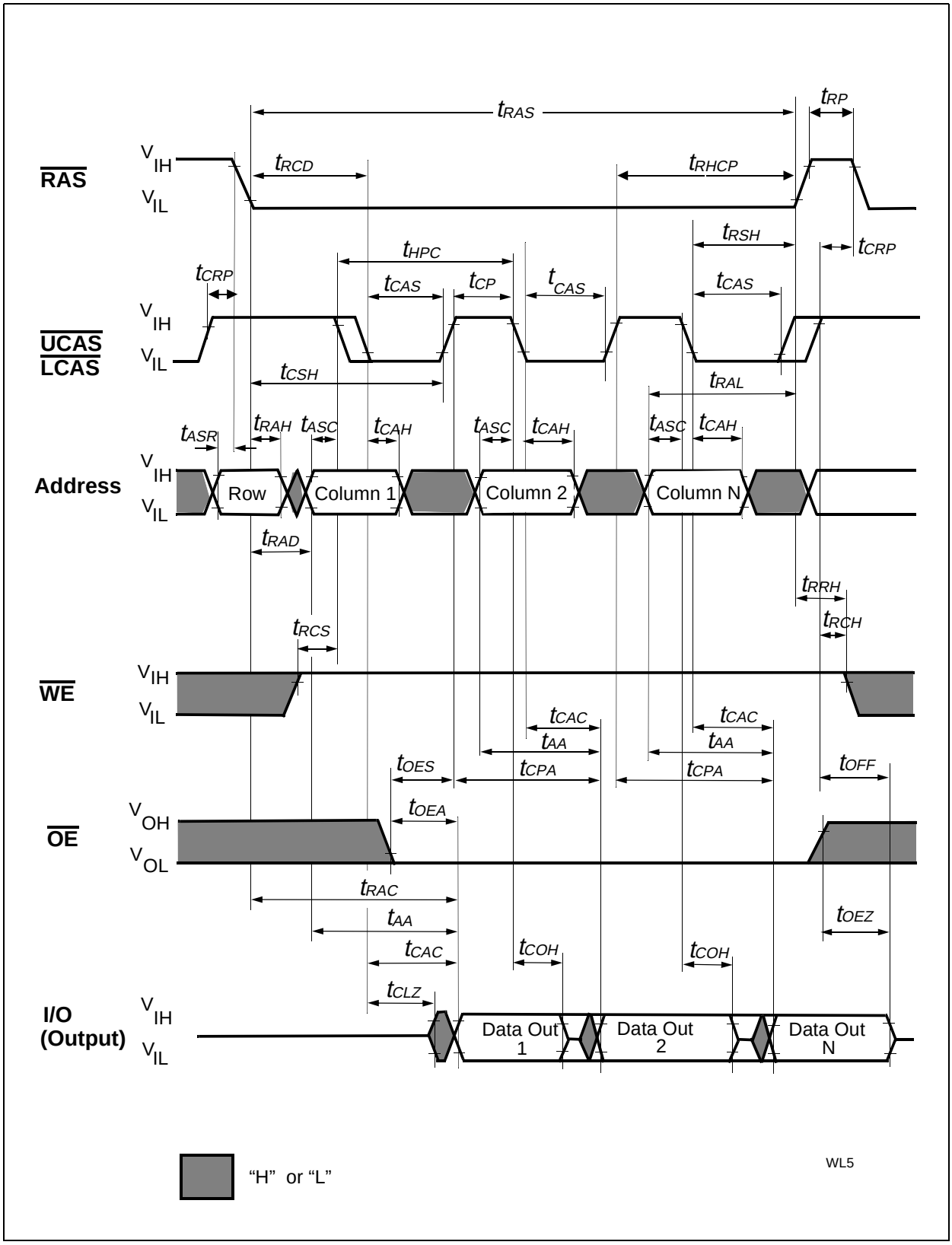
Write Cycle ($\overline{OE}$ Controlled Write)



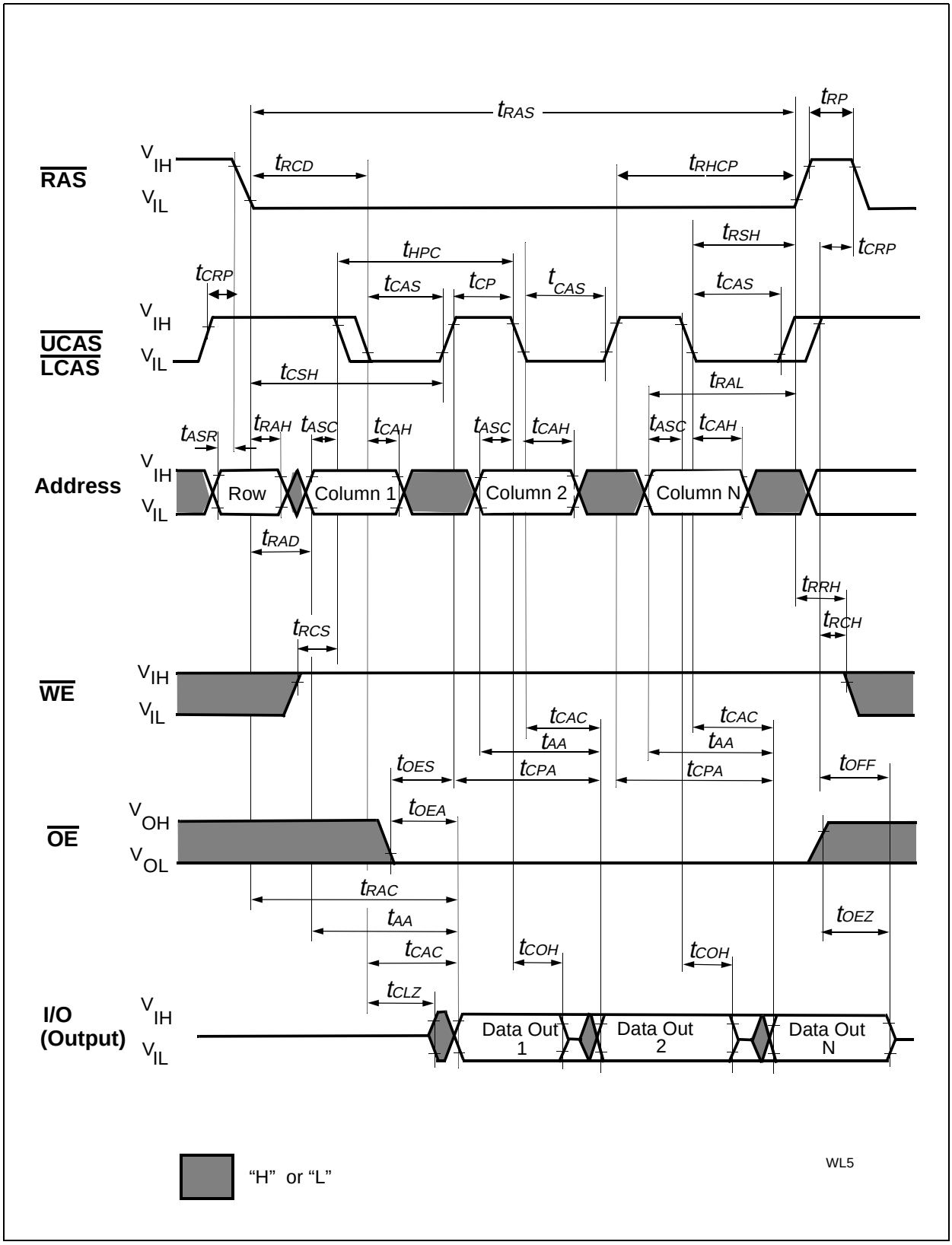
Read-Write (Read-Modify-Write) Cycle



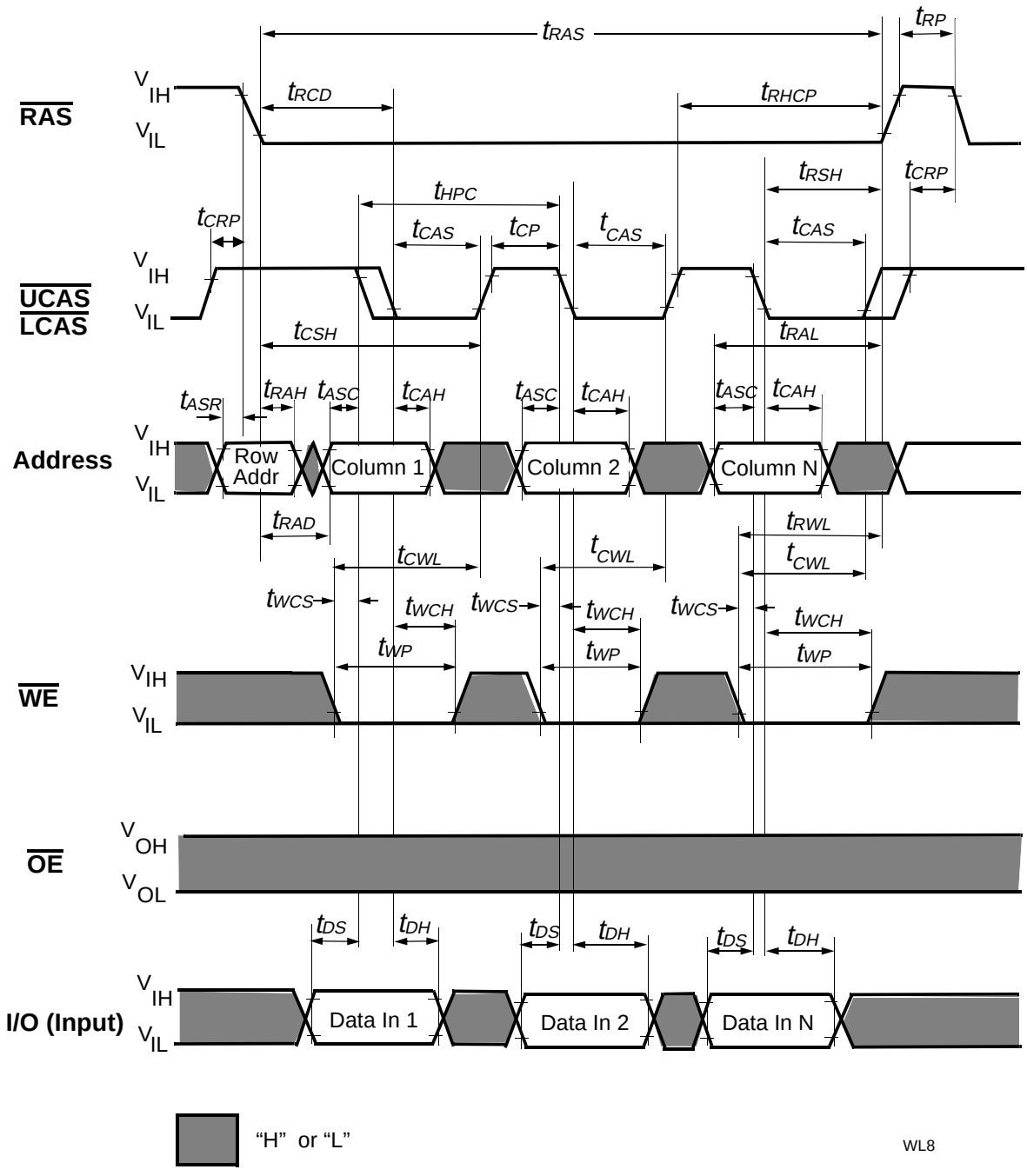
Read-Write (Read-Modify-Write) Cycle



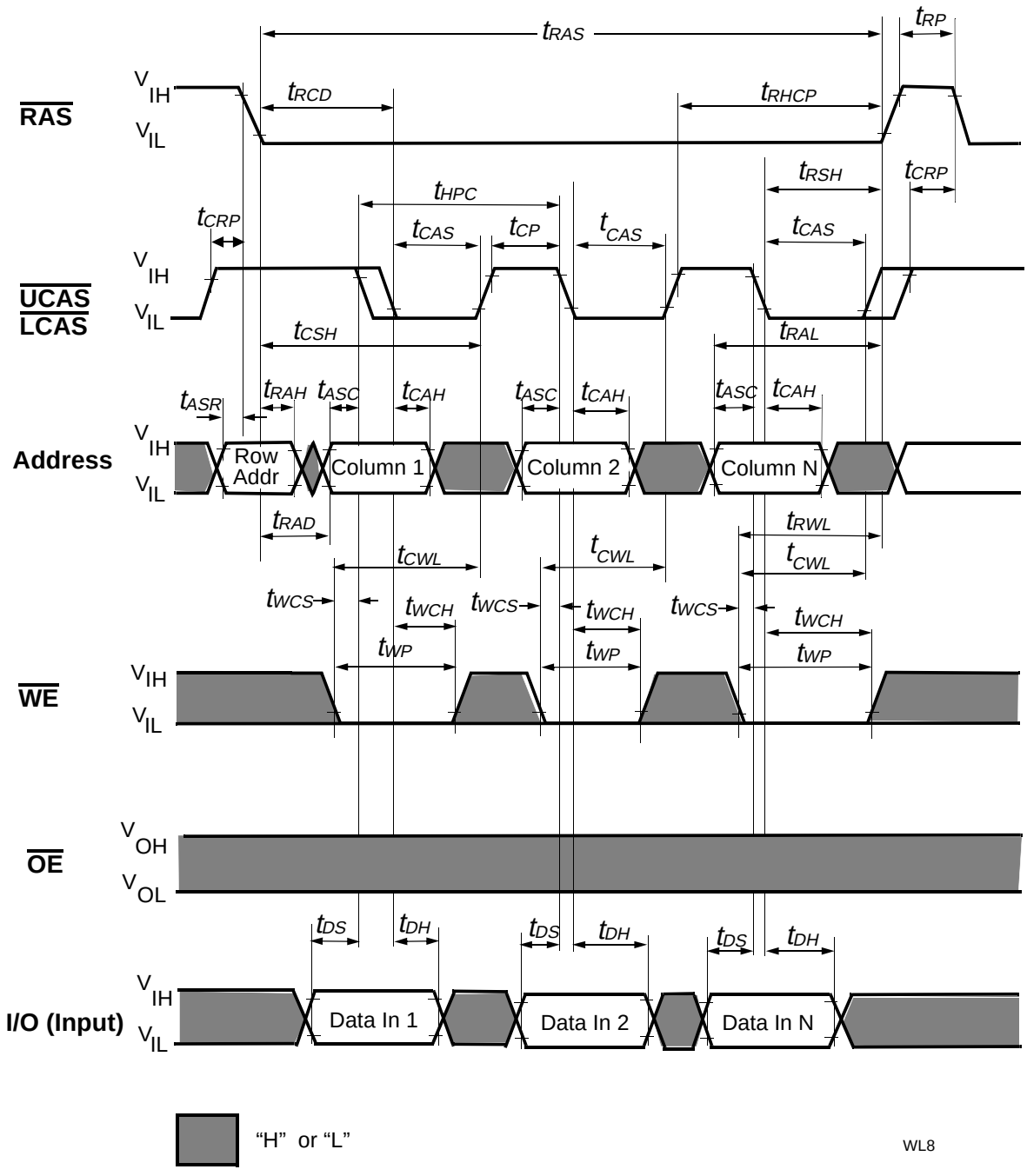
Hyper Page Mode (EDO) Read Cycle



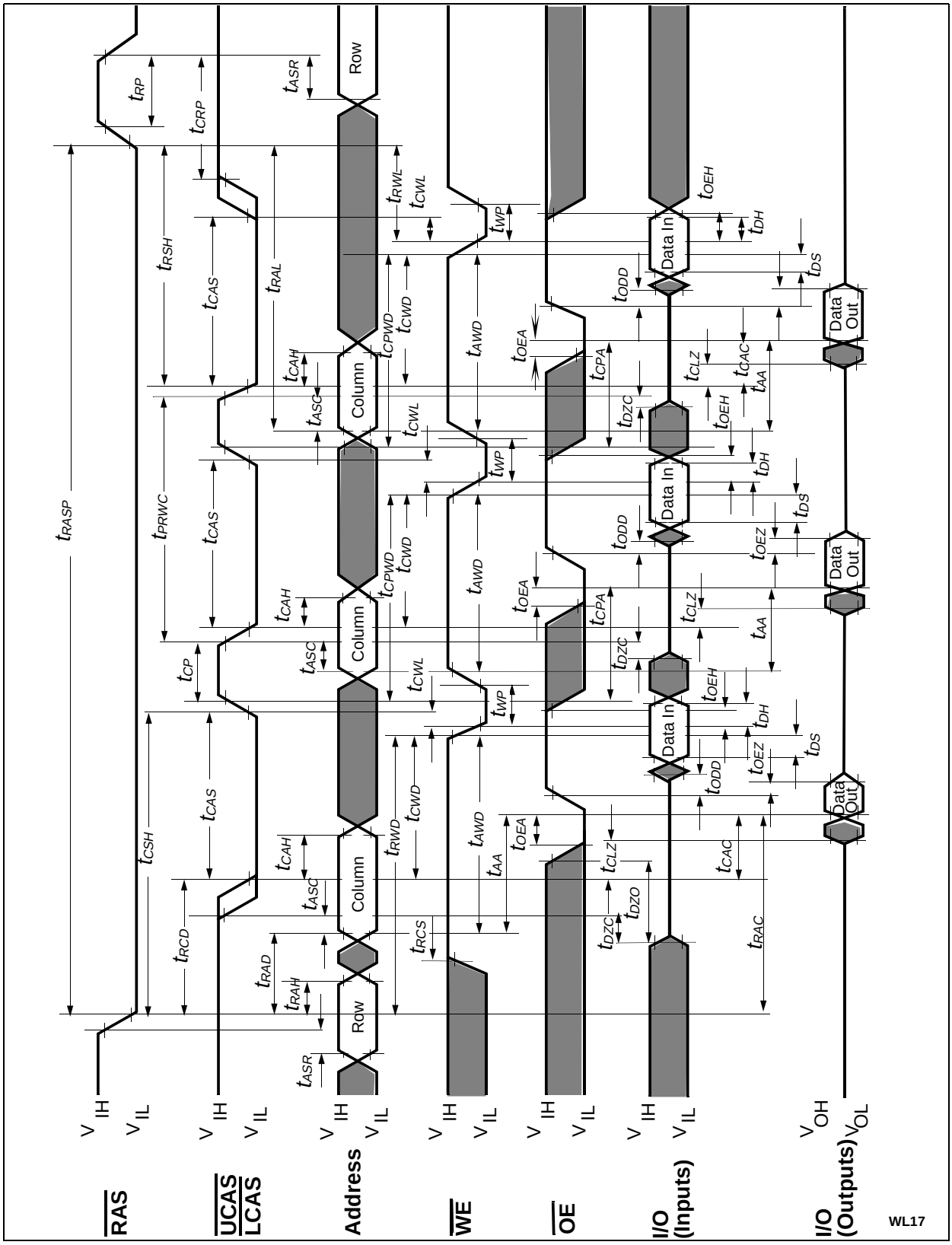
Hyper Page Mode (EDO) Read Cycle



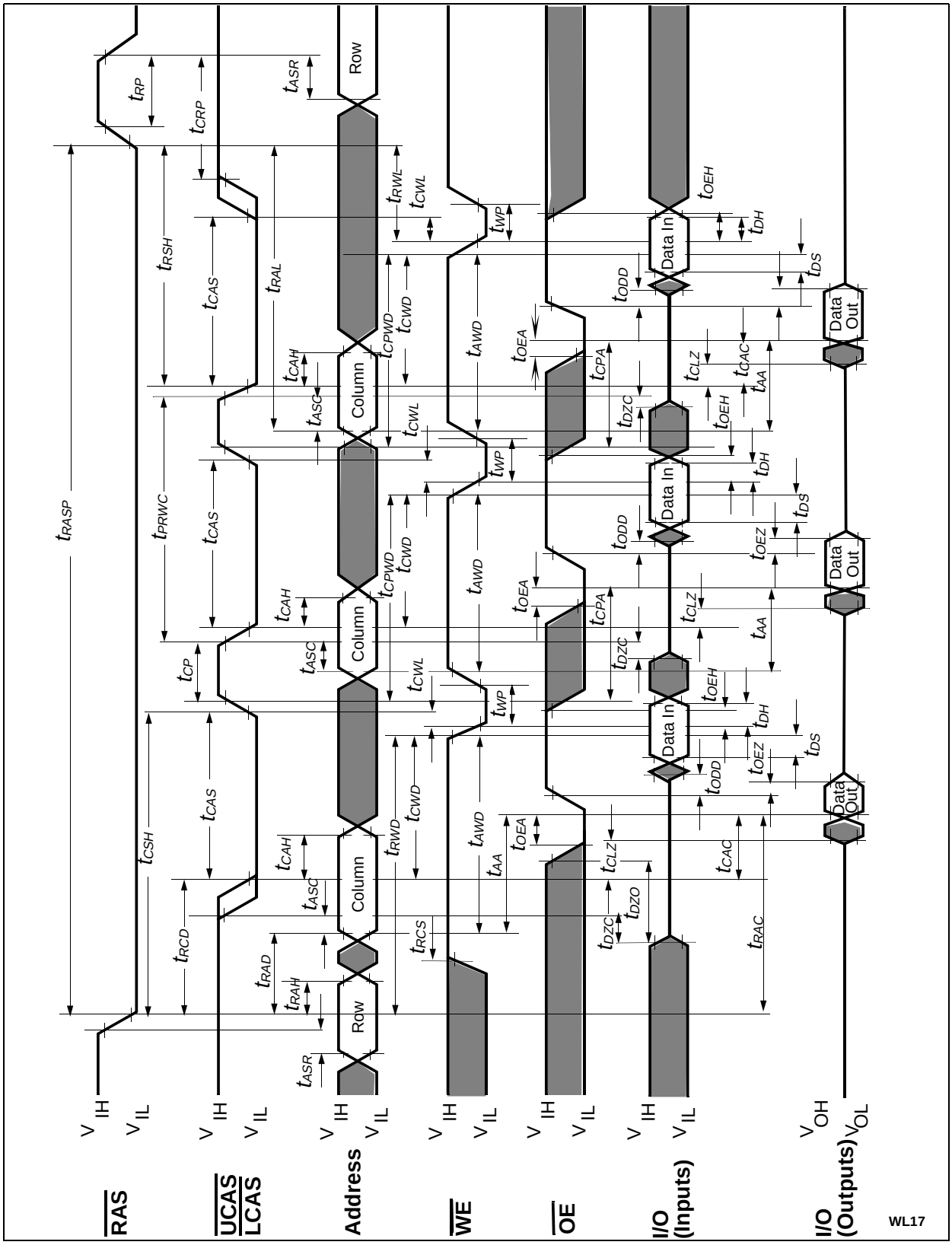
Hyper Page Mode (EDO) Early Write Cycle



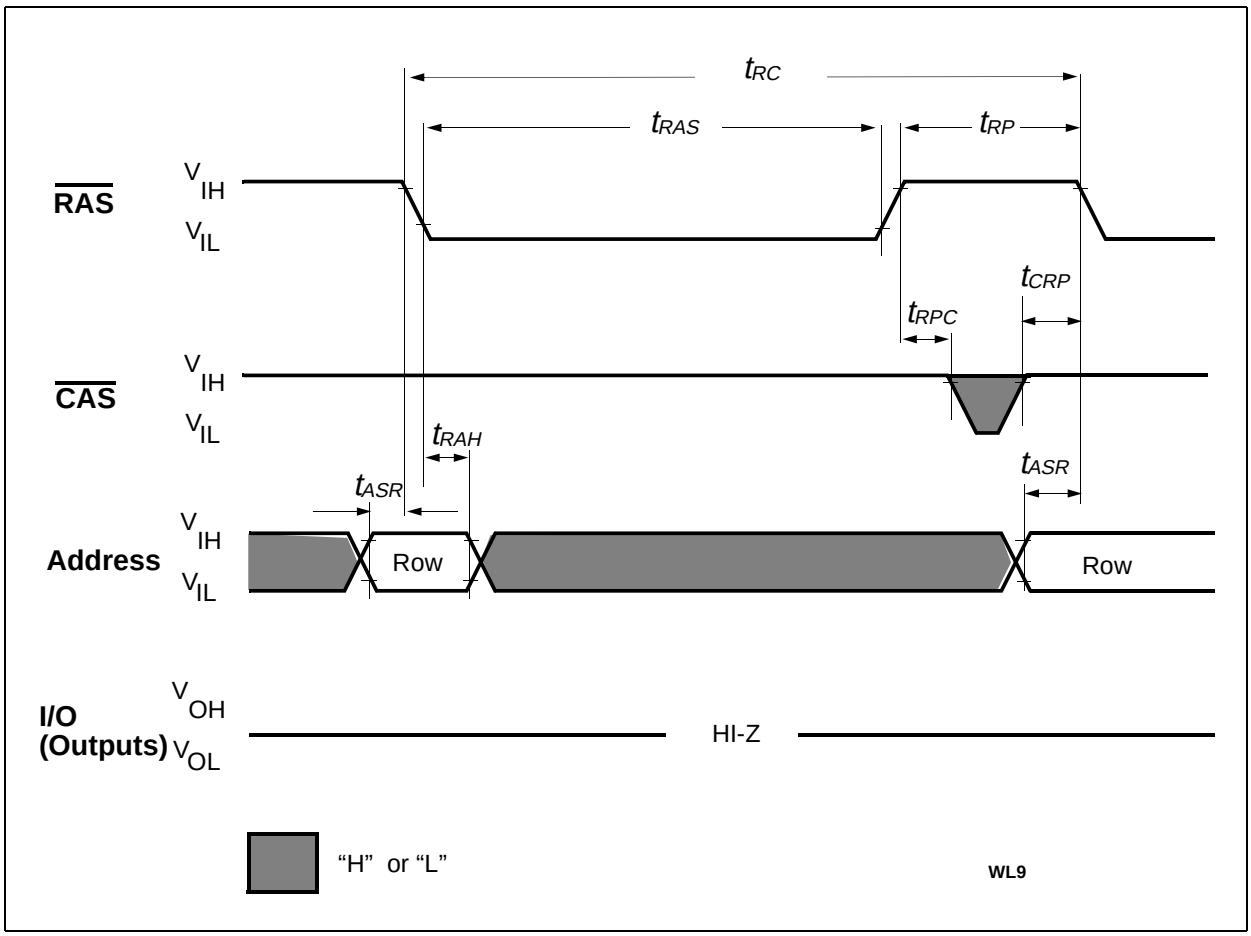
Hyper Page Mode (EDO) Early Write Cycle



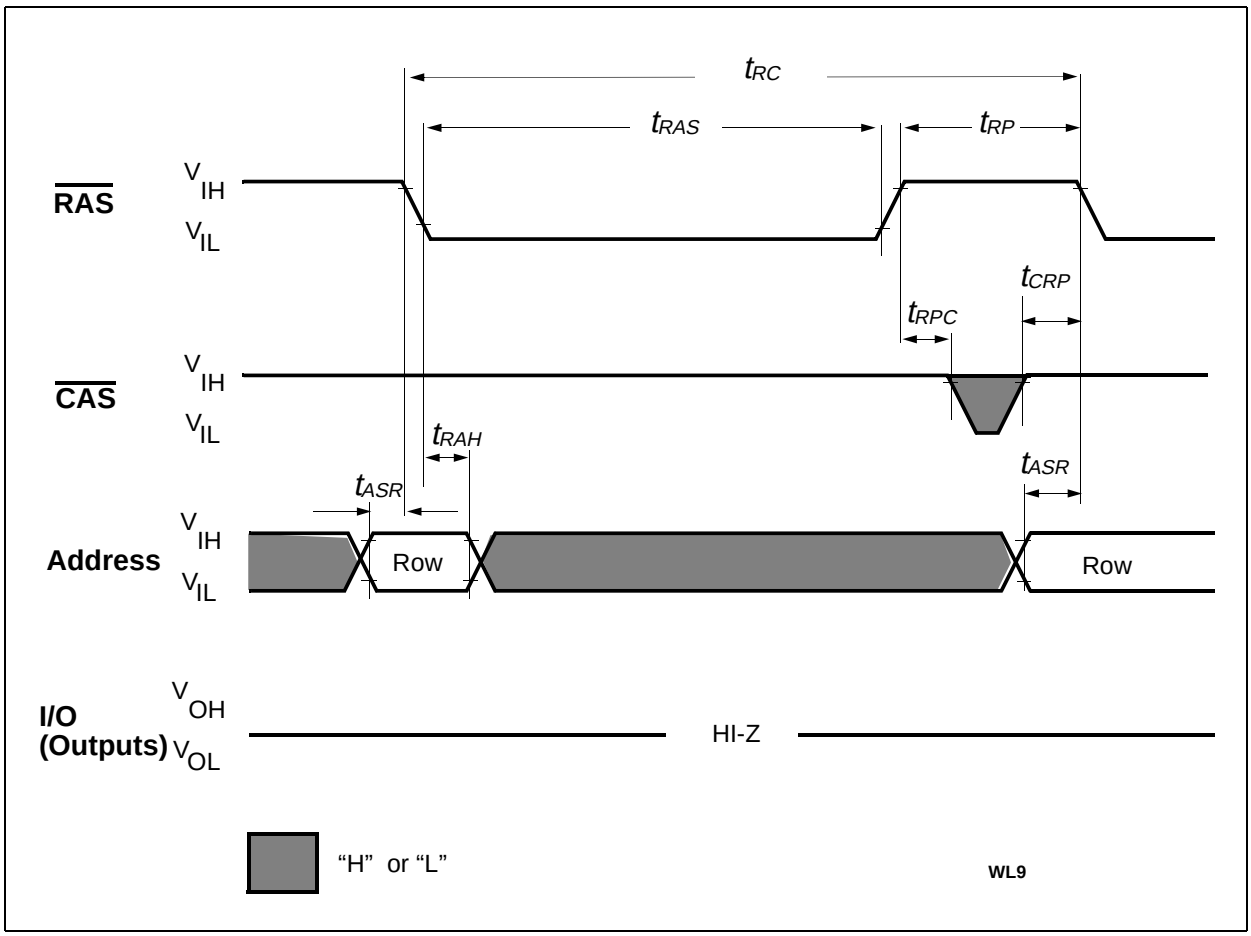
Hyper Page Mode (EDO) Late Write and Read-Modify- Write Cycle



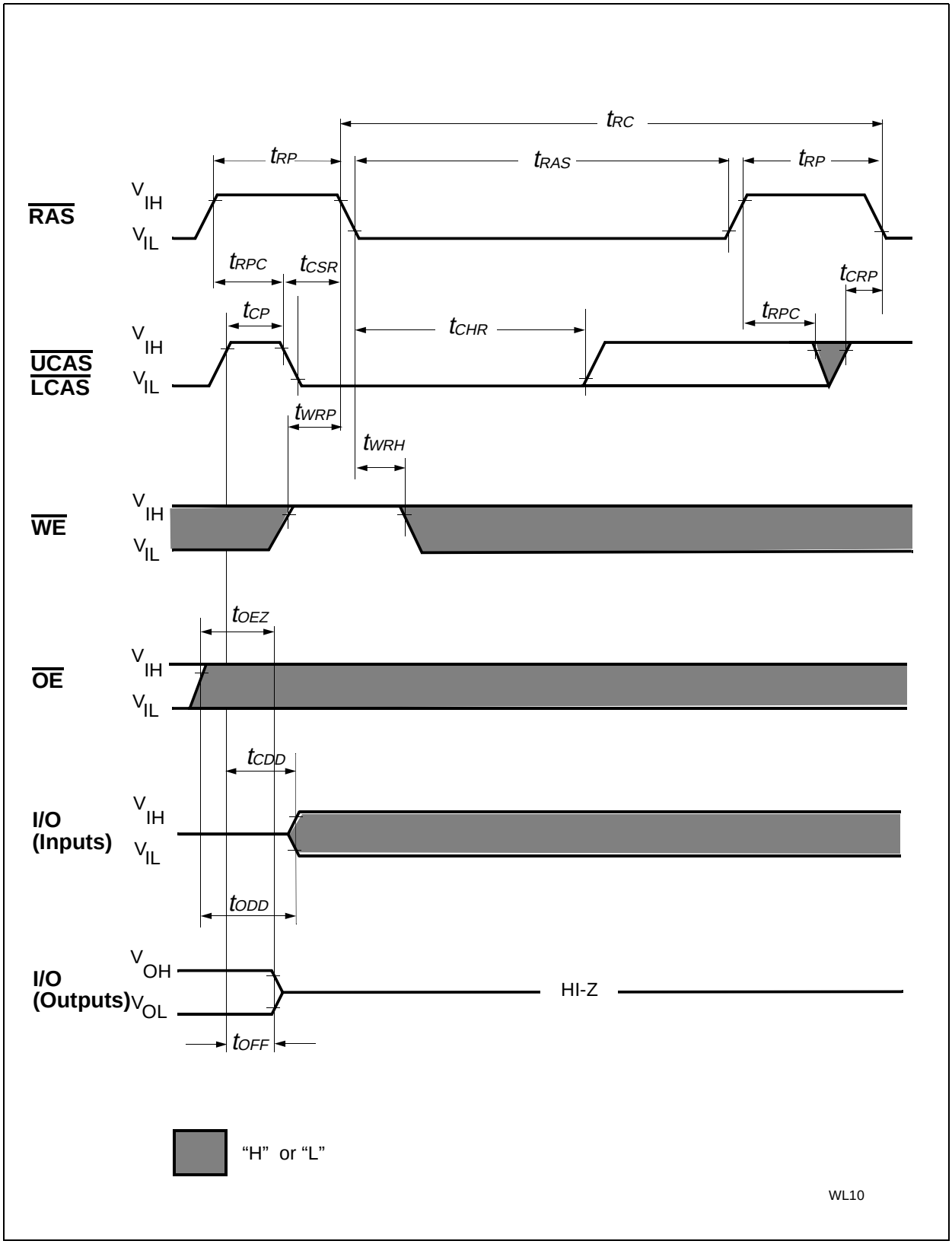
Hyper Page Mode (EDO) Late Write and Read-Modify- Write Cycle



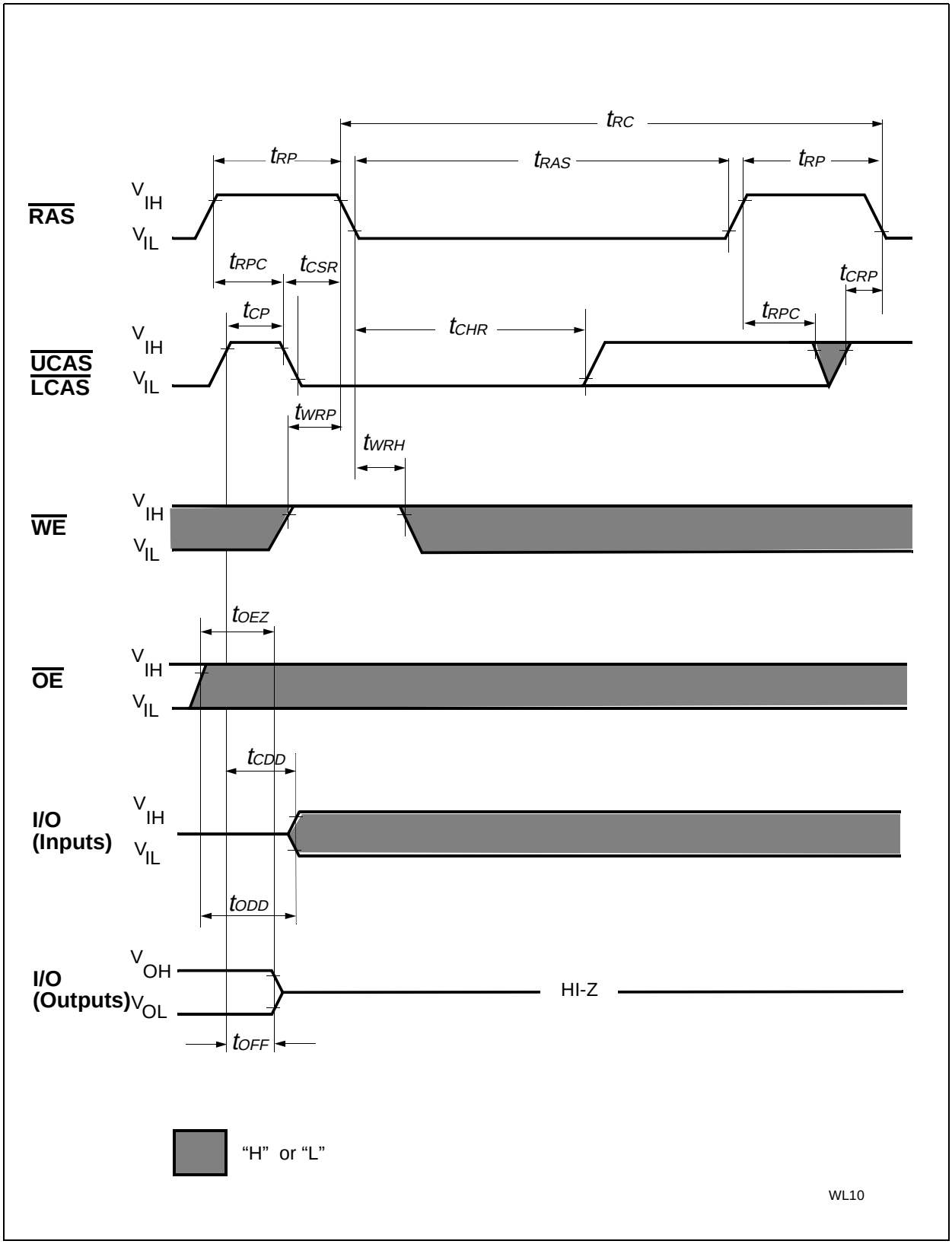
RAS-Only Refresh Cycle



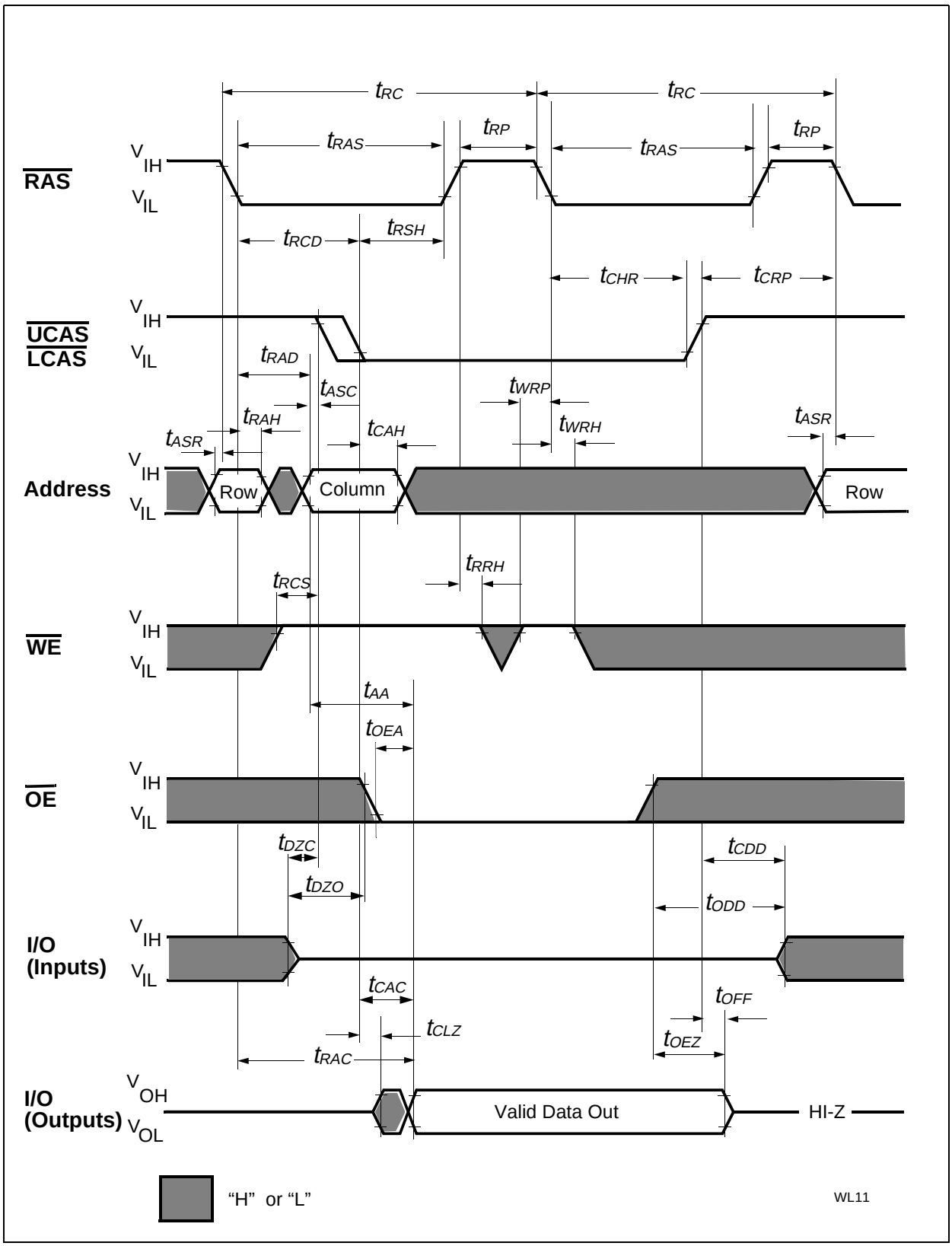
RAS-Only Refresh Cycle



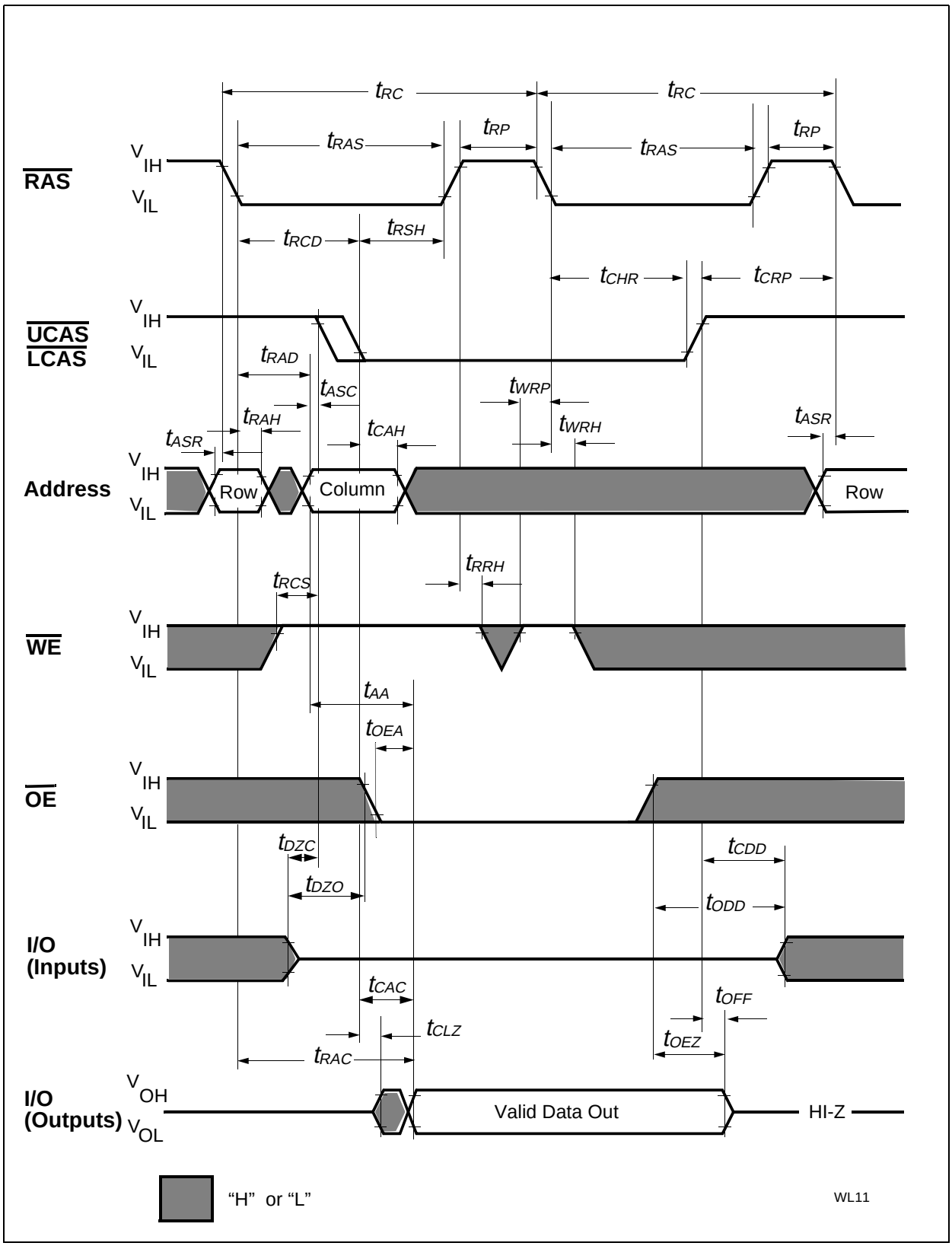
CAS-Before-RAS Refresh Cycle



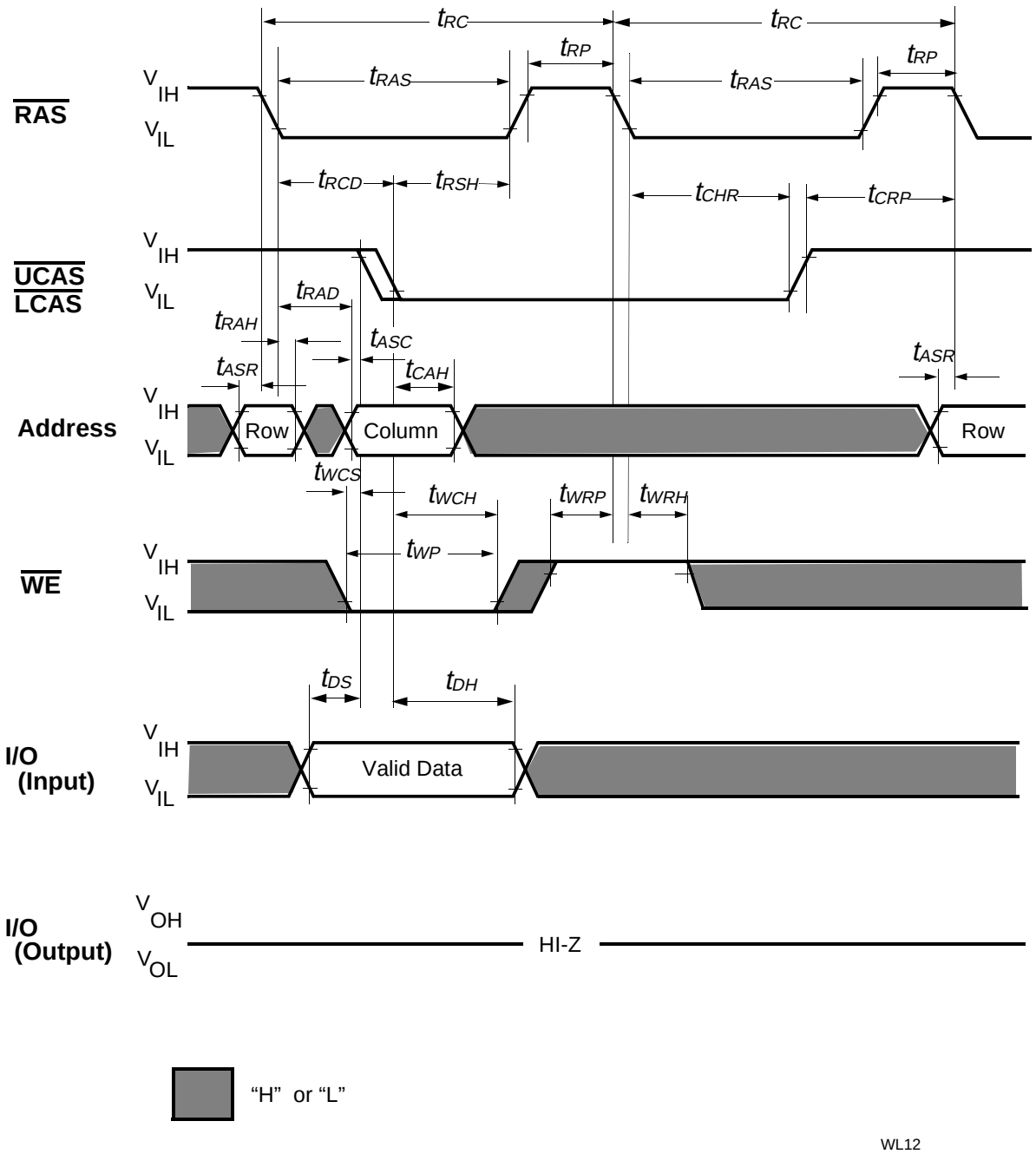
CAS-Before-RAS Refresh Cycle



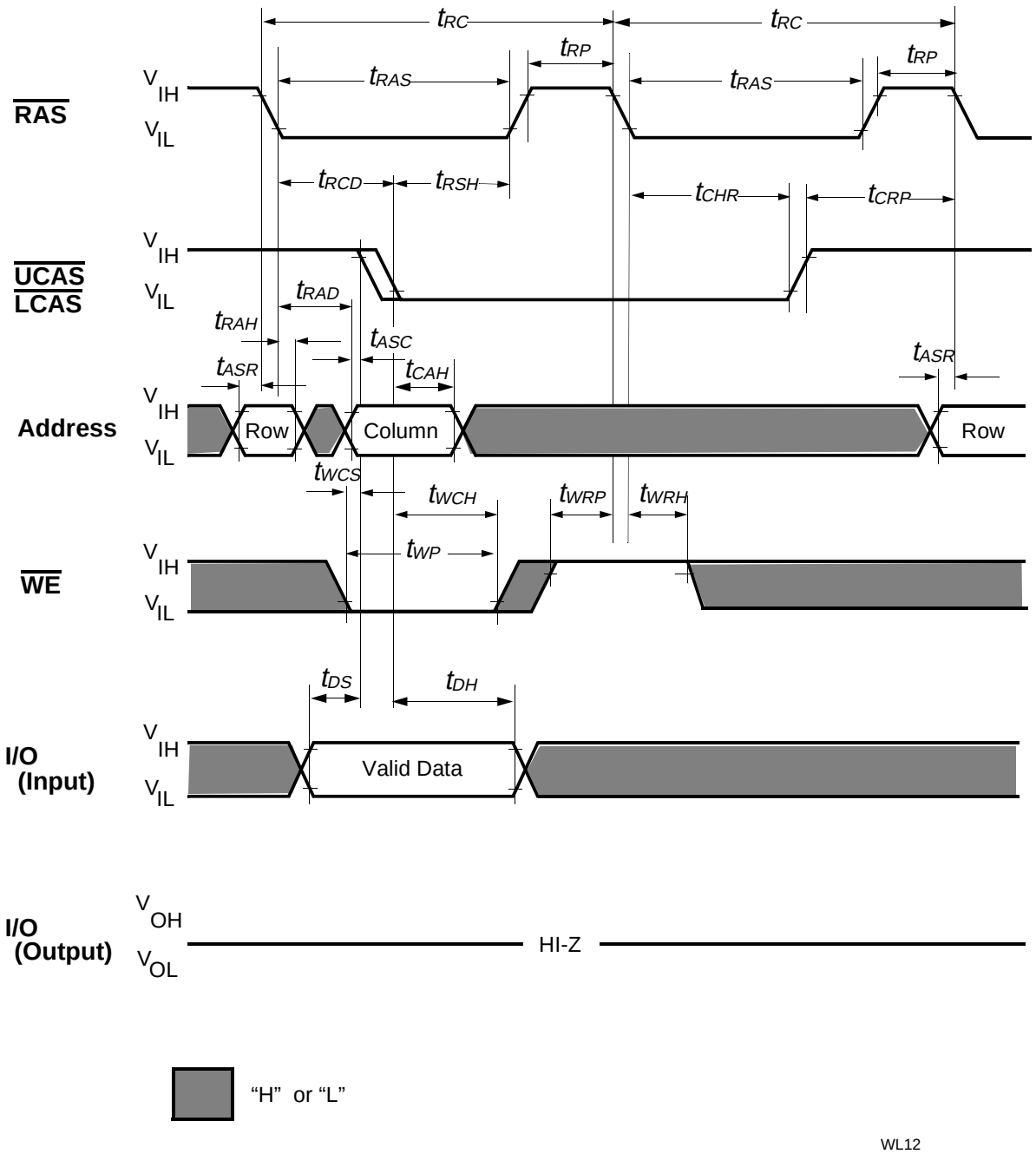
Hidden Refresh Cycle (Read)



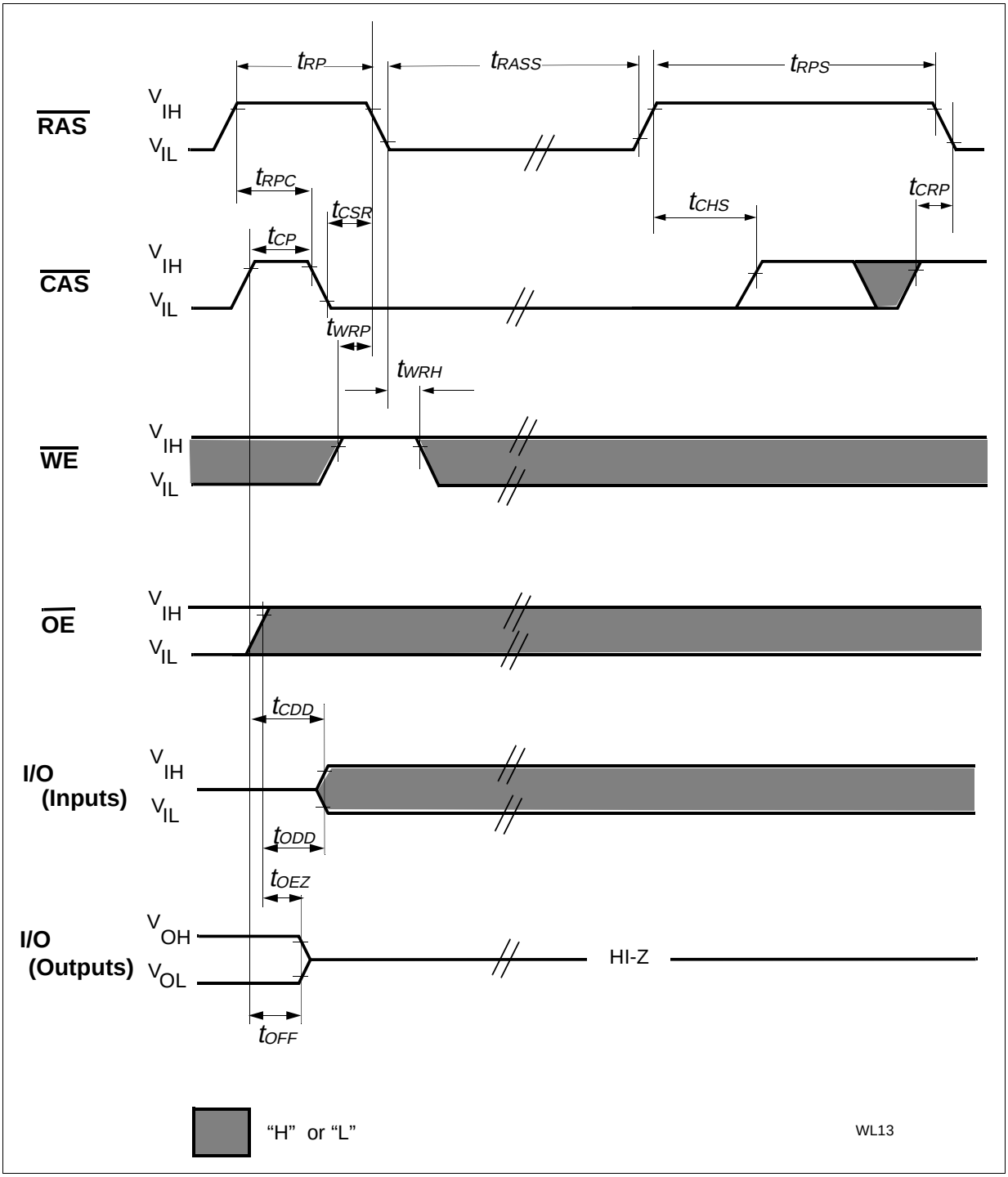
Hidden Refresh Cycle (Read)



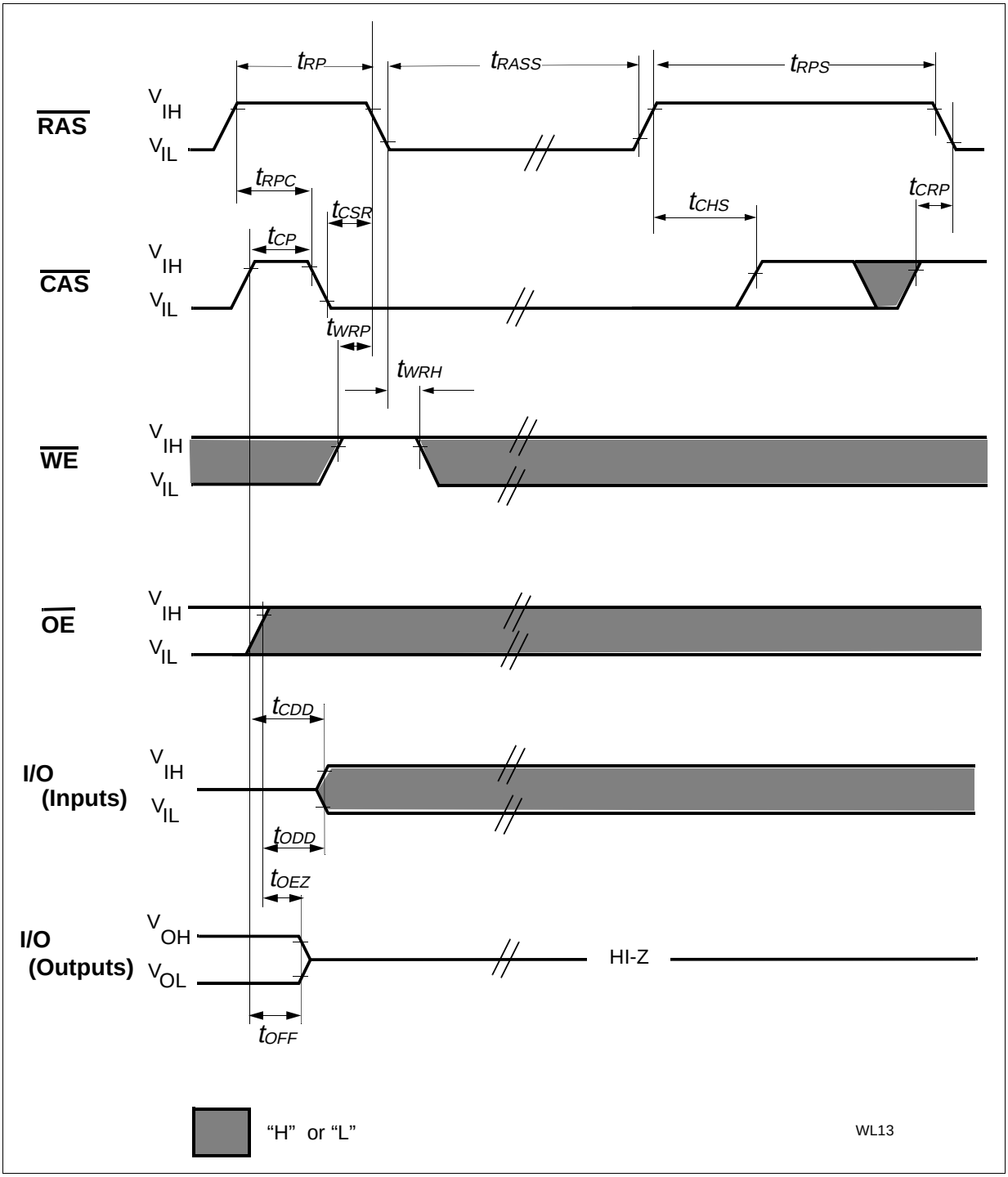
Hidden Refresh Cycle (Early Write)



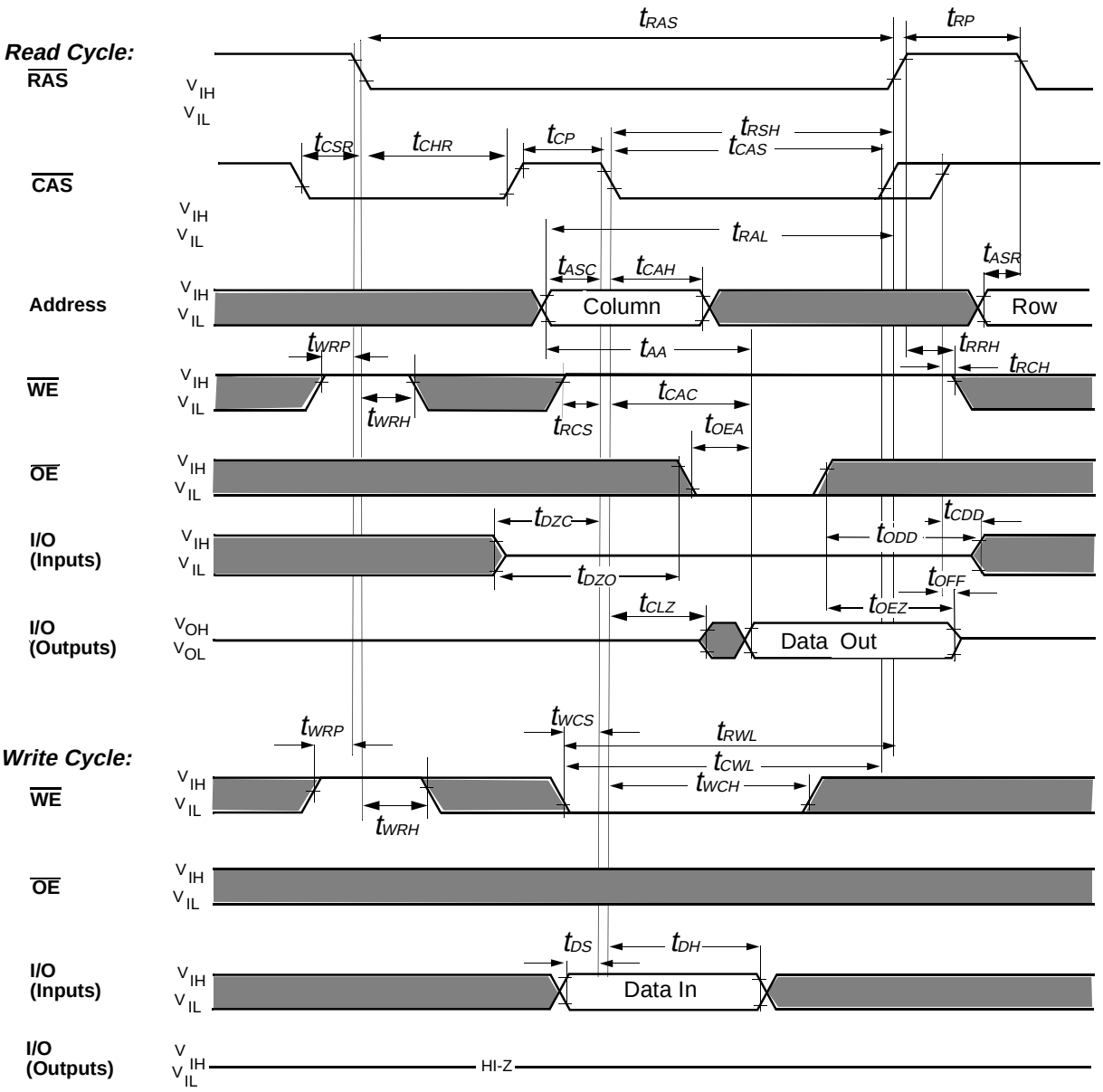
Hidden Refresh Cycle (Early Write)



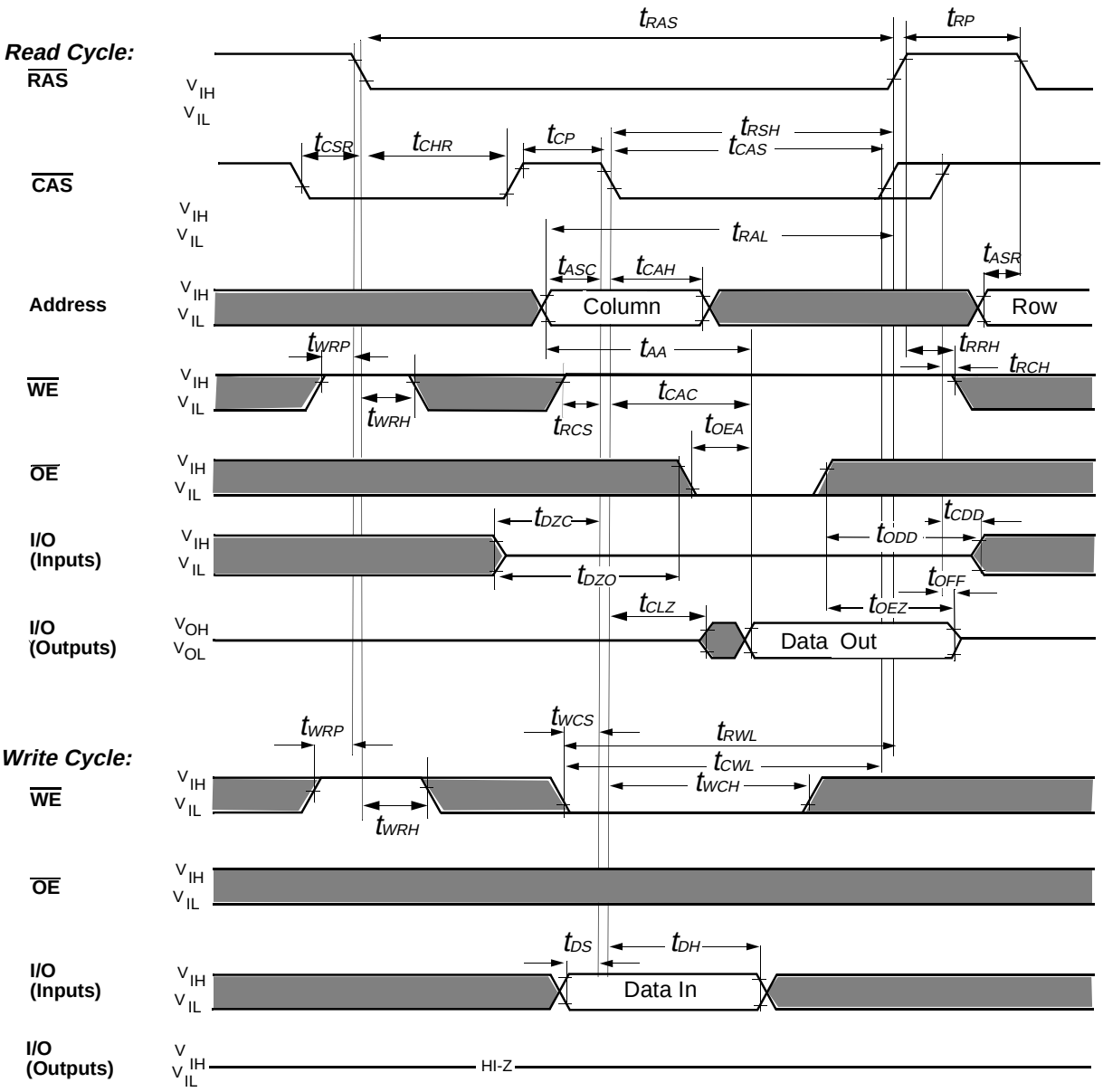
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle



$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Self Refresh Cycle



$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle

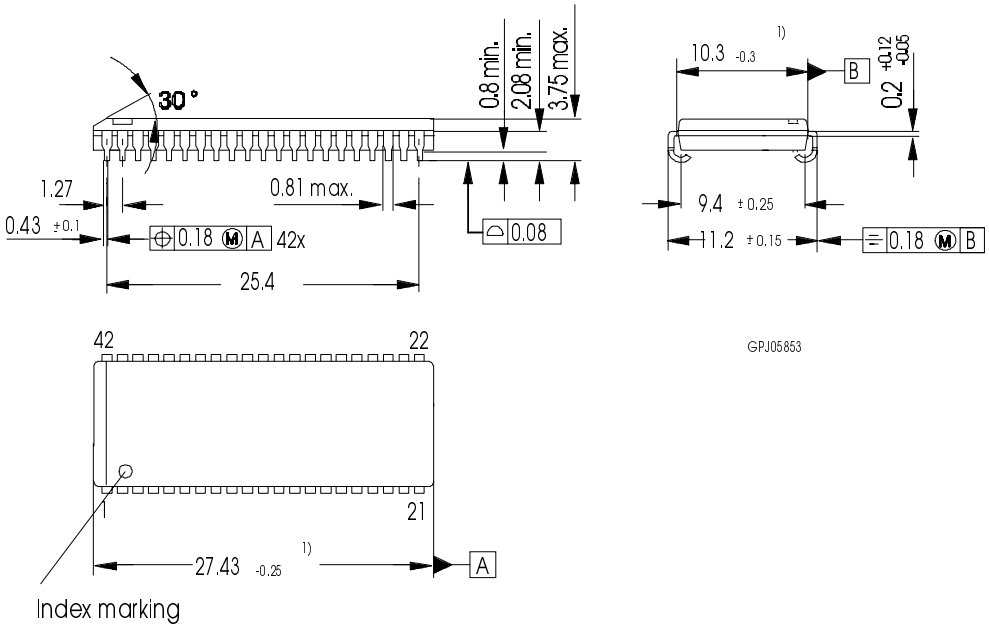


$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Counter Test Cycle

Package Outlines

Plastic Package P-SOJ-42 (400 mil)

(Small Outline J-lead, SMD)

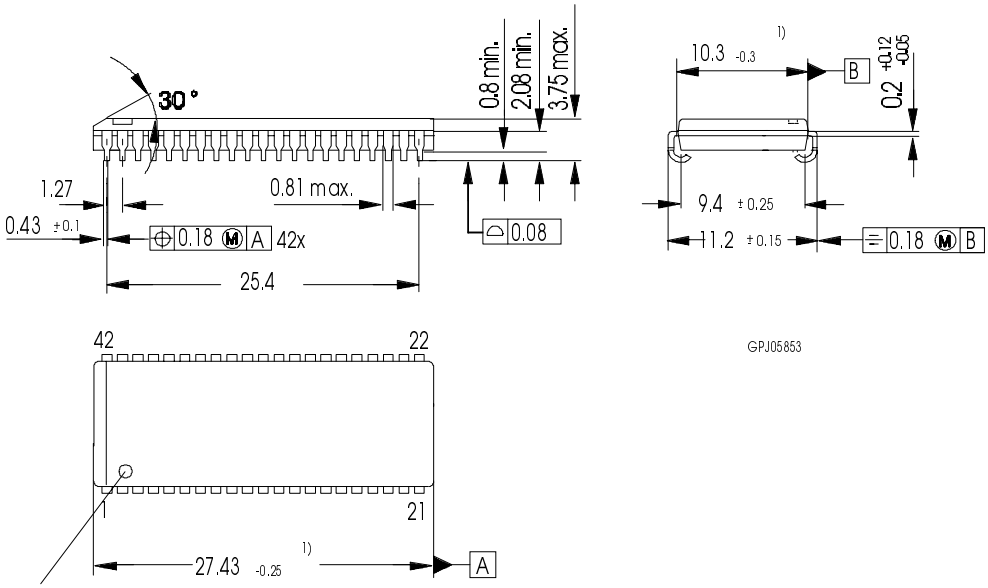


1) does not include plastic or metal protusion of 0.15 max per side

Package Outlines

Plastic Package P-SOJ-42 (400 mil)

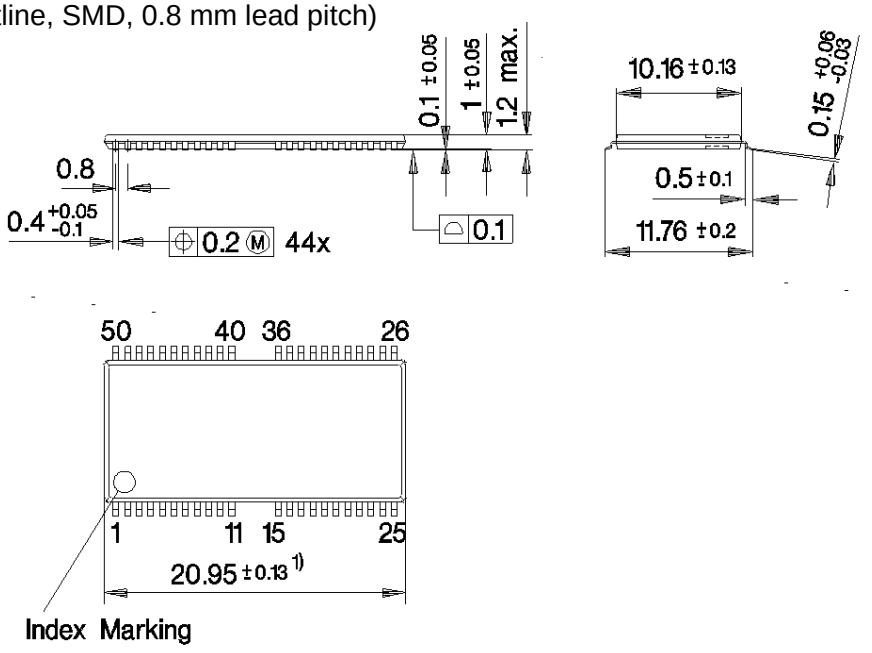
(Small Outline J-lead, SMD)



1) does not include plastic or metal protusion of 0.15 max per side

Plastic Package P-TSOPII-50/44 (400 mil)

(Thin Small Outline, SMD, 0.8 mm lead pitch)



1) Does not include plastic or metal protrusion of 0.25 max. per side