Logic level and sensitive gate triacs

Introduction

Triacs have been available since the early 1970s. They could be regarded as a mature technology. However, they remain an extremely popular power control device for AC mains applications because of their low cost and the simplicity of their control circuits. Nothing can better them in these two respects. There has even been an upsurge in their use in the 1990s due partly to the proliferation of domestic appliances with electronic controls. Common examples of these include air and water heaters, vacuum cleaners, refrigerators, washing machines, dishwashers and most small kitchen appliances.

Despite their maturity, triacs have not "stood still" since their first invention. They have evolved to meet the changing demands of the applications. One important change in triac requirements is the gate sensitivity specification I_{GT}. Early triac trigger circuits were built using discrete components which could supply high currents up to 100mA peak or more. Triacs therefore did not require sensitive gates. This is still relevant today for phase control circuits which use a diac such as the BR100/03 to trigger the triac. However, Integrated Circuit control is becoming ever more popular for two main reasons:

1. Stringent Electro Magnetic Compatibility regulations limit the harmonic currents that can be drawn from the mains and also limit the amount of Radio Frequency Interference that can be generated by appliances. This requires the use of either a dedicated zero crossing triac power control IC such as the OM1654 or OM1682 from Philips Australia, or a microcontroller which has been programmed to perform a similar function in which a high harmonic and RFI-generating phase control circuit is replaced by an electrically "quieter" alternative. An example might be Binary Rate Modulation power control, where varying full and half mains cycles are conducted symmetrically to ensure very low harmonic currents and zero DC component in the current waveform.

2. More intelligent appliance controls are now being demanded such as remote control, soft start, variable timing, automatic power ramp-up & ramp-down, and power reduction after full power startup for energy conservation measures (applicable to refrigerator compressors in particular). These would be very complicated, expensive or even impossible to implement using discrete components.
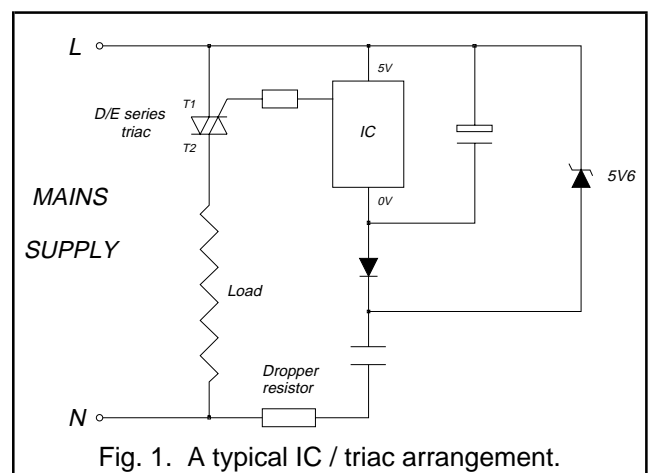

Fig. 1. A typical IC / triac arrangement.

Integrated circuits such as the dedicated triac controller ICs and microcontrollers possess a limited drive current capability which ranges from 10mA to 15mA typically. Moreover, since the IC's supply is usually derived from the mains via a resistive/capacitive dropper and simple half wave rectifier, power dissipation in the resistor can very easily become unacceptably high if the load current is not kept to an absolute minimum. This means that the average current demand from the IC's power supply must usually be minimised. This can impose a limit on the current amplitude and duration available for triggering the triac. This is even more relevant if several triacs are controlled by one microcontroller. Examples where this holds true are fridge freezers and washing machines. This can mean that the drive current available for triac triggering is even less than the 10mA to 15mA suggested above.

Figure 1 shows a simple IC-triac arrangement. The 5.6V zener diode combined with the forward voltage drop of the rectifier diode produce an IC supply close to 5V. The advantages of connecting the zener as shown instead

of directly across the IC are that full wave current is drawn from the mains supply (no DC component), and the forward conduction of the zener means that the rectifier never has to support full mains voltage. A cheap, low voltage diode can therefore be used. Attention must be paid, however, to the additional power dissipation in the resistor due to the forward zener current.

These IC-triac power control applications could not be implemented without sensitive triacs. Philips logic level D series and sensitive gate E series triacs are designed to meet fully the requirements in this burgeoning market. For a full selection guide of available types, see Tables 1 and 2.

Gate trigger current I_{GT}

Philips D and E series triacs are specified to trigger in all four quadrants. However, a feature of four-quadrant triacs is that they are less sensitive and more difficult to trigger in the 4th (T2-, G+) quadrant. (For example, for the D series, max I_{GT} in quadrant 1,2,3,4 is 5,5,5,10mA, and for the E series it is 10,10,10,25mA.) The ability of triacs to support a high rate of rise of load current (dI_T/dt) after turn-on is also limited in the 4th quadrant. (dI_T/dt is 10A/μs compared with 50A/μs in the other three quadrants). For these two reasons, operation in the 4th quadrant is not recommended if it can be avoided.
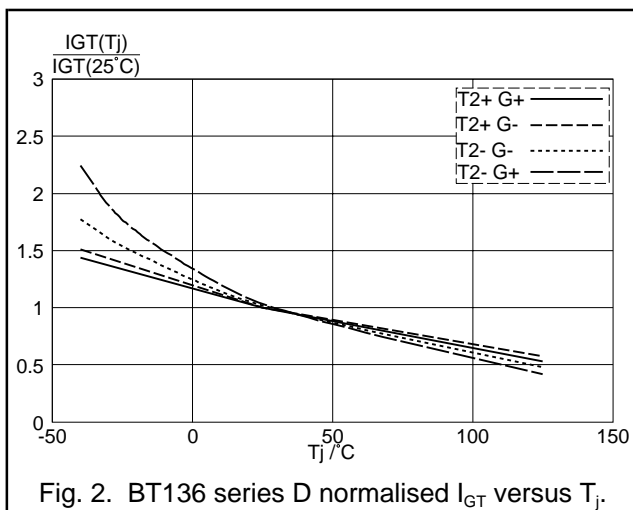

Fig. 2. BT136 series D normalised I_{GT} versus T_j.

Since the control IC operates on a single rail supply (usually +5V), its outputs are unipolar. It can be referenced to the mains circuit in order to source current (positive gate drive) or to sink current (negative gate drive). Since 4th quadrant triggering should be avoided, optimum performance will be obtained with negative gate current - i.e operation in the 2nd (T2+, G-) and 3rd (T2-, G-) quadrants (see Fig. 1).

A triac's I_{GT} varies with junction temperature. At lower temperature the I_{GT} increases. It is therefore important to ensure that the circuit supplies enough gate current at the lowest expected operating temperature for guaranteed triggering. Figure 2 shows an example of normalised I_{GT} versus T_j for the BT136 series D.

Latching current I_L

If the triac is triggered by a gate current at the beginning of a mains half cycle, the load current will build up gradually from zero. The gate current must not be removed before the triac is latched ON otherwise it will return to the blocking state. Latching occurs when the load current reaches I_L. The gate pulse must therefore be present until the load current has reached I_L.

Just as for I_{GT}, I_L also increases at lower temperature. The gate pulse duration must be specified at the lowest expected operating temperature for guaranteed triggering. Figure 3 shows an example of normalised I_L versus T_j for the BT136 series D.
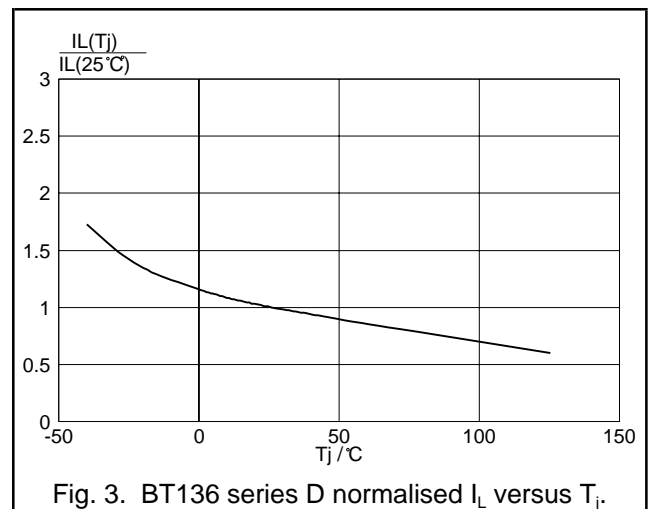

Fig. 3. BT136 series D normalised I_L versus T_j.

How quickly the load current reaches the triac's I_L will depend on the peak load current and mains frequency. Taken to the extreme case, if the load current is so low that its peak value is equivalent to I_L, it will take one quarter cycle, or 5ms for 50Hz mains, before the triac is latched and the gate pulse can cease.

It is also important to be aware that higher current triacs have a higher I_L. This could compound problems or even lead to the triac never latching ON if the load current is lower than the triac's I_L. So, apart from the higher component cost, it would not be a good idea to use a triac whose current rating is very much higher than the load current when a lower current type is available. Tables 1 and 2 illustrate how I_L varies with the triggering quadrant and triac current rating.

Minimum triac drive current calculation

Because the current demand must be minimised in many IC applications, it is necessary to calculate the gate pulse duration to be just long enough to guarantee triac triggering while avoiding unnecessary burden on the IC's power supply. The time to reach I_L, hence the gate pulse duration, can be calculated using the equation:

$I_L = I_{pk} \times \sin(2\pi ft)$. Transposing gives:

$$t = 1/(2\pi f) \times \sin^{-1}(I_L/I_{pk}).$$

The average gate current supplied by the IC is calculated by multiplying its peak gate current with t/T. Hence:

$$I_{G(ave)} = I_{G(pk)} \times t/T.$$

I_L = triac latching current at the lowest expected operating temperature,

I_{pk} = peak load current,

t = gate pulse duration,

T = gate pulse cycle time.

Note:- Since triac latching current is higher in the 2nd and 4th quadrants, and normal operation for IC triggering is in the 2nd and 3rd quadrants, the gate current calculations must always be based on the worst case quadrant 2 I_L condition.

If the load current is very low and the necessary gate pulse duration imposes too great a burden on the IC's power supply, triggering could be delayed for a few degrees to allow the supply voltage to build up a little. The time to reach I_L will then be shortened by the delay time (true for resistive loads). Now that switching occurs further from the zero crossing, there will be a slightly increased risk of RFI generation, even if the load current is very low as in this case. RFI measurements will show if filtering is necessary to meet the relevant EMC legislation.

Holding current I_H

As the load current reduces towards the end of a mains half cycle, a current, I_H, will be reached when the triac is no longer latched. It will cease to conduct in the absence of a gate current. I_H also increases with reducing temperature. Figure 4 shows an example of normalised I_H versus T_j for the BT136 series D.

In some IC applications where the triac is used as a power switch, for example a precision electronic thermostat for a refrigerator compressor, continuous conduction must be maintained through the current zero crossing. (This is essential to prevent glitches and RFI generation.) Continuous conduction is achieved by monitoring the load current and applying a gate pulse

before the triac's I_H is reached, and maintaining the pulse until the current has passed through zero and risen to the triac's I_L in the alternate quadrant. This condition must be met at the lowest expected operating temperature for continuous glitch-free conduction under worst case conditions.
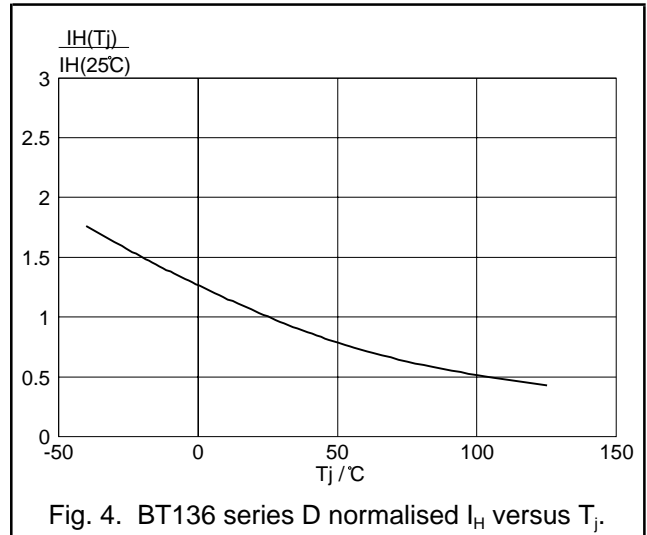

Fig. 4. BT136 series D normalised I_H versus T_j.

I_H increases for the larger E series triacs. The most sensitive D series triacs, however, are designed to maintain a consistent, low I_H of 10mA @ 25°C even for the higher 8A current rating.

Figure 5 illustrates triac load current zero crossing and the minimum gate pulse required for continuous conduction through the max I_H and I_L points. The diagram illustrates how I_H remains constant in different quadrants. The point made earlier about how I_L varies in different quadrants is illustrated by the higher I_L in the 2nd quadrant (T2+, G-). I_G duration must meet this worst case condition.
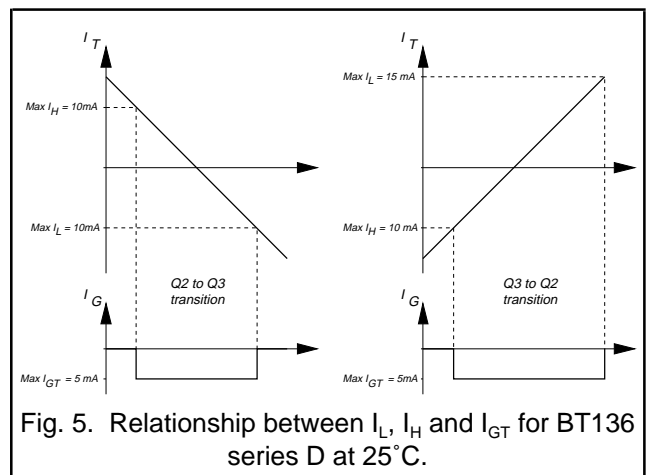

Fig. 5. Relationship between I_L, I_H and I_{GT} for BT136 series D at 25°C.

Selection guide

Type number	$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} max (mA)	I_L max (mA)	I_H max (mA)	Package
BT134W-...D BT134-...D BT136-...D BT136F-...D BT136X-...D	1 4 4 4 4	500,600	5,5,5,10	10,15,10,15	10	SOT223 SOT82 SOT78 SOT186 SOT186A
BT137-...D BT137F-...D BT137X-...D	8 8 8	500,600	5,5,5,10	15,20,15,20	10	SOT78 SOT186 SOT186A

Tabe 1. Philips D series logic level triacs.

Type number	$I_{T(RMS)}$ (A)	V_{DRM} (V)	I_{GT} max (mA)	I_L max (mA)	I_H max (mA)	Package
BT134W-...E BT134-...E BT136-...E BT136F-...E BT136X-...E	1 4 4 4 4	500,600 500,600,800	10,10,10,25	15,20,15,20	15	SOT223 SOT82 SOT78 SOT186 SOT186A
BT137-...E BT137F-...E BT137X-...E	8 8 8	500,600,800	10,10,10,25	25,35,25,35	20	SOT78 SOT186 SOT186A
BT138-...E BT138F-...E BT138X-...E BT139-...E BT139F-...E BT139X-...E	12 12 12 16 16 16	500,600,800	10,10,10,25	30,40,30,40	30	SOT78 SOT186 SOT186A SOT78 SOT186 SOT186A

Table 2. Philips E series sensitive gate triacs.

NOTE: SOT78 is equivalent to TO220AB.