

# DATA SHEET

## **FBL2031**

9-bit BTL 3.3V latched/registered/pass-thru  
Futurebus+ transceiver

Product specification  
Supersedes data of 1998 Sep 04

2000 Apr 18

# 9-bit BTL 3.3V latched/registered/pass-thru Futurebus+ transceiver

## FBL2031

### FEATURES

- Latched, registered or straight through in either A to B or B to A path
- Drives heavily loaded backplanes with equivalent load impedances down to 10Ω.
- High drive 100mA BTL open collector drivers on B-port
- Allows incident wave switching in heavily loaded backplane buses
- Reduced BTL voltage swing produces less noise and reduces power consumption
- Built-in precision band-gap reference provides accurate receiver thresholds and improved noise immunity
- Compatible with IEEE Futurebus+ or proprietary BTL backplanes
- Each BTL driver has a dedicated Bus GND for a signal return
- Controlled output ramp and multiple GND pins minimize ground bounce

- Glitch-free power up/power down operation
- Low  $I_{CC}$  current
- Tight output skew
- Supports live insertion
- Pins for the optional JTAG boundary scan function are provided
- High density packaging in plastic Quad Flatpack
- 5V compatible I/O on A-port

### DESCRIPTION

The FBL2031 is a 9-bit latched/registered transceiver featuring a latched, registered or pass-thru mode in either the A-to-B or B-to-A direction.

The FBL2031 is intended to provide the electrical interface to a high performance wired-OR bus.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER		TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to $\overline{Bn}$		2.7	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay $\overline{Bn}$ to An		4.4 4.2	ns
$C_O$	Output capacitance ( $\overline{B0} - \overline{Bn}$ only)		6	pF
$I_{OL}$	Output current ( $\overline{B0} - \overline{Bn}$ only)		100	mA
$I_{CC}$	Supply current	AIn to $\overline{Bn}$ (outputs Low or High)	11	mA
		$\overline{Bn}$ to AOn (outputs Low)	22	
		$\overline{Bn}$ to AOn (outputs High)	18	

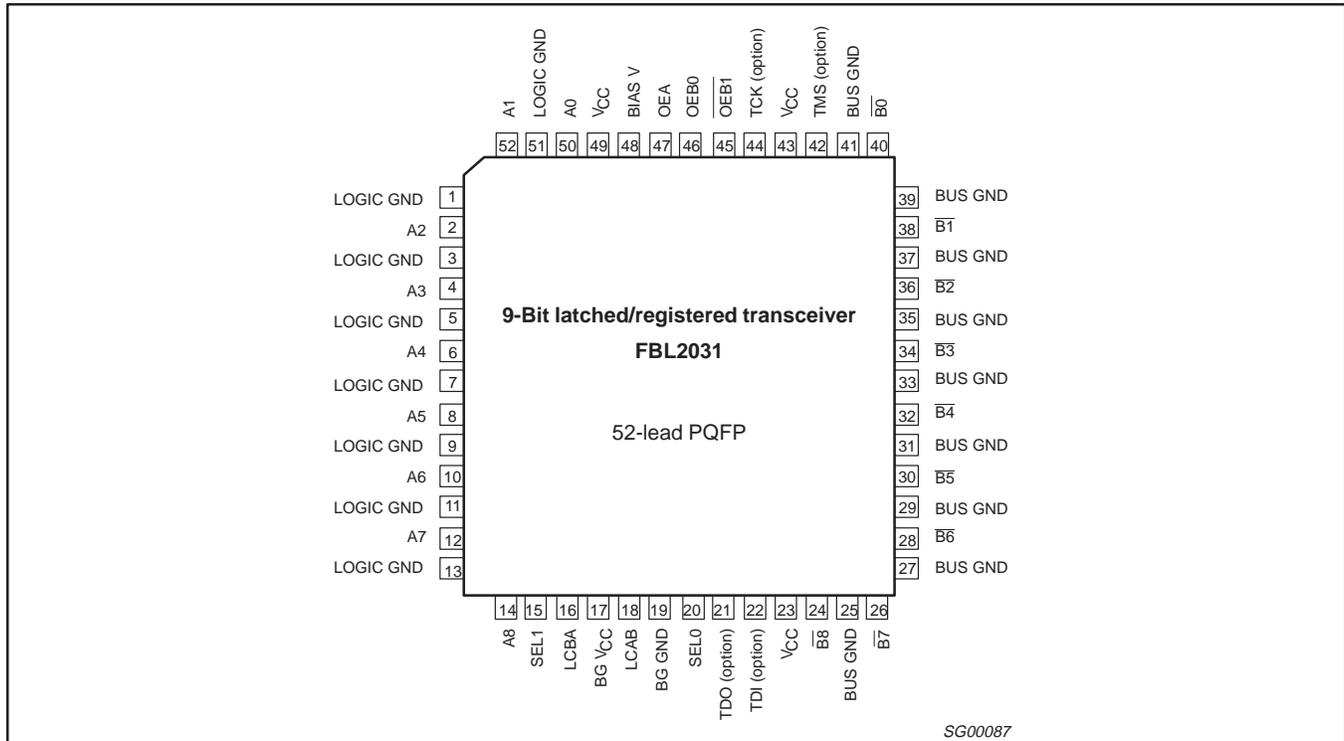
### ORDERING INFORMATION

PACKAGE	$V_{CC} = 3.3V \pm 10\%$ ; $T_{amb} = -40^\circ C$ to $+85^\circ C$	DWG No.
52-pin Plastic Quad Flat Pack (PQFP)	FBL2031BB	SOT379-1

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## PIN CONFIGURATION



## PIN DESCRIPTION

SYMBOL	PIN NUMBER	TYPE	NAME AND FUNCTION
A0 – A8	50, 52, 2, 4, 6, 8, 10, 12, 14	I/O	BiCMOS data inputs/3-State outputs (TTL)
$\overline{B0} - \overline{B8}$	40, 38, 36, 34, 32, 30, 28, 26, 24	I/O	Data inputs/Open Collector outputs, High current drive (BTL)
OEB0	46	Input	Enables the B outputs when High
$\overline{OEB1}$	45	Input	Enables the B outputs when Low
OEA	47	Input	Enables the A outputs when High
BUS GND	25, 27, 29, 31, 33, 35, 37, 39, 41	GND	Bus ground (0V)
LOGIC GND	51, 1, 3, 5, 7, 9, 11, 13	GND	Logic ground (0V)
V <sub>CC</sub>	23, 43, 49	Power	Positive supply voltage
BIAS V	48	Power	Live insertion pre-bias pin
BG V <sub>CC</sub>	17	Power	Band Gap threshold voltage reference
BG GND	19	GND	Band Gap threshold voltage reference ground
SEL0	20	Input	Mode select
SEL1	15	Input	Mode select
LCAB	18	Input	A to B clock/latch enable (transparent latch when Low)
LCBA	16	Input	B to A clock/latch enable (transparent latch when Low)
TMS	42	Input	Test Mode Select (optional, if not implemented then no connect)
TCK	44	Input	Test Clock (optional, if not implemented then no connect)
TDI	22	Input	Test Data In (optional, if not implemented then no connect)
TDO	21	Output	Test Data Out (optional, if not implemented then shorted to TDI)

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## DESCRIPTION

The TTL-level side (A port) has a common I/O. The common I/O, open collector B port operates at BTL signal levels. The logic element for data flow in each direction is controlled by two mode select inputs (SEL0 and SEL1). A "00" configures latches in both directions. A "10" configures thru mode in both directions. A "01" configures register mode in both directions. A "11" configures register mode in the A-to-B direction and latch mode in the B-to-A direction.

When configured in the buffer mode, the inverse of the input data appears at the output port. In the register mode, data is stored on the rising edge of the appropriate clock input (LCAB or LCBA). In the latch mode, clock pins serve as transparent-Low latch enables. Regardless of the mode, data is inverted from input to output.

The 3-State A port is enabled by asserting a High level on OEA. The B port has two output enables, OEB0 and  $\overline{\text{OEB1}}$ . Only when OEB0 is High and  $\overline{\text{OEB1}}$  is Low is the output enabled.

When either OEB0 is Low or  $\overline{\text{OEB1}}$  is High, the B port is inactive and is pulled to the level of the pull-up voltage. New data can be entered in the register and latched modes or can be retained while the associated outputs are in 3-State (A port) or inactive (B port).

The B-port drivers are Low-capacitance open collectors with controlled ramp and are designed to sink 100mA. Precision band gap references on the B-port insure very good noise margins by limiting the switching threshold to a narrow region centered at 1.55V.

The B-port interfaces to "Backplane Transceiver Logic" (see the IEEE 1194.1 BTL standard). BTL features low power consumption by reducing voltage swing (1V p-p, between 1V and 2V) and reduced capacitive loading by placing an internal series diode on the

drivers. BTL also provides incident wave switching, a necessity for high performance backplanes.

Output clamps are provided on the BTL outputs to further reduce switching noise. The " $V_{OH}$ " clamp reduces inductive ringing effects during a Low-to-High transition. The " $V_{OH}$ " clamp is always active. The other clamp, the "trapped reflection" clamp, clamps out ringing below the BTL 0.5V  $V_{OL}$  level. This clamp remains active for approximately 100ns after a High-to-Low transition.

To support live insertion, OEB0 is held Low during power on/off cycles to insure glitch-free B port drivers. Proper bias for B port drivers during live insertion is provided by the BIAS V pin when at a 3.3V level while  $V_{CC}$  is Low. The BIAS V pin is a low current input which will reverse-bias the BTL driver series Schottky diode, and also bias the B port output pins to a voltage between 1.62V and 2.1V. This bias function is in accordance with IEEE BTL Standard 1194.1. If live insertion is not a requirement, the BIAS V pin should be tied to a  $V_{CC}$  pin.

The LOGIC GND and BUS GND pins are isolated inside the package to minimize noise coupling between the BTL and TTL sides. These pins should be tied to a common ground external to the package.

Each BTL driver has an associated BUS GND pin that acts as a signal return path and these BUS GND pins are internally isolated from each other. In the event of a ground return fault, a "hard" signal failure occurs instead of a pattern dependent error that may be infrequent and impossible to troubleshoot.

As with any high power device, thermal considerations are critical. It is recommended that airflow (300lfpm) and/or thermal mounting be used to ensure proper junction temperature.

## PACKAGE THERMAL CHARACTERISTICS

PARAMETER	CONDITION	52-PIN PLASTIC QFP
$\theta_{ja}$	Still air	80°C/W
$\theta_{ja}$	300 Linear feet per minute air flow	58°C/W
$\theta_{jc}$	Thermally mounted on one side to heat sink	20°C/W

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FUNCTION TABLE

MODE	INPUTS									OUTPUTS	
	An	Bn*	OEB0	OEB1	OEA	LCAB	LCBA	SEL0	SEL1	An	Bn
An to Bn thru mode	L	—	H	L	L	X	X	H	L	input	H**
	H	—	H	L	L	X	X	H	L	input	L
An to Bn transparent latch	L	—	H	L	L	L	X	L	L	input	H**
	H	—	H	L	L	L	X	L	L	input	L
An to Bn latch and read	l	—	H	L	L	↑	X	L	L	input	H**
	h	—	H	L	L	↑	X	L	L	input	L
Bn outputs latched and read (preconditioned latch)	X	—	H	L	X	H	X	L	L	X	latched data
An to Bn register	l	—	H	L	L	↑	X	X	H	input	H**
	h	—	H	L	L	↑	X	X	H	input	L
Bn to An thru mode	—	L	Disable		H	X	X	H	L	H	input
	—	H	Disable		H	X	X	H	L	L	input
Bn to An transparent latch	—	L	Disable		H	X	L	L	L	H	input
	—	H	Disable		H	X	L	L	L	L	input
	—	L	Disable		H	X	L	H	H	H	input
	—	H	Disable		H	X	L	H	H	L	input
	—	l	Disable		H	X	↑	L	L	H	input
Bn to An latch and read	—	h	Disable		H	X	↑	L	L	L	input
	—	l	Disable		H	X	↑	H	H	H	input
	—	h	Disable		H	X	↑	H	H	L	input
	—	l	Disable		H	X	↑	H	H	L	input
An outputs latched and read (preconditioned latch)	—	X	X	X	H	X	H	L	L	latched data	X
	—	X	X	X	H	X	H	H	H	latched data	X
Bn to An register	—	l	Disable		H	X	↑	L	H	H	input
	—	h	Disable		H	X	↑	L	H	L	input
Disable Bn outputs	X	X	L	X	X	X	X	X	X	X	H**
	X	X	X	H	X	X	X	X	X	X	H**
Disable An outputs	X	X	X	X	L	X	X	X	X	Z	X

FUNCTION SELECT TABLE

MODE SELECTED	SEL0	SEL1
Thru mode	H	L
Register mode (An to Bn)	X	H
Latch mode (An to Bn)	L	L
Register mode (Bn to An)	L	H
Latch mode (Bn to An)	L	L
	H	H

NOTES:

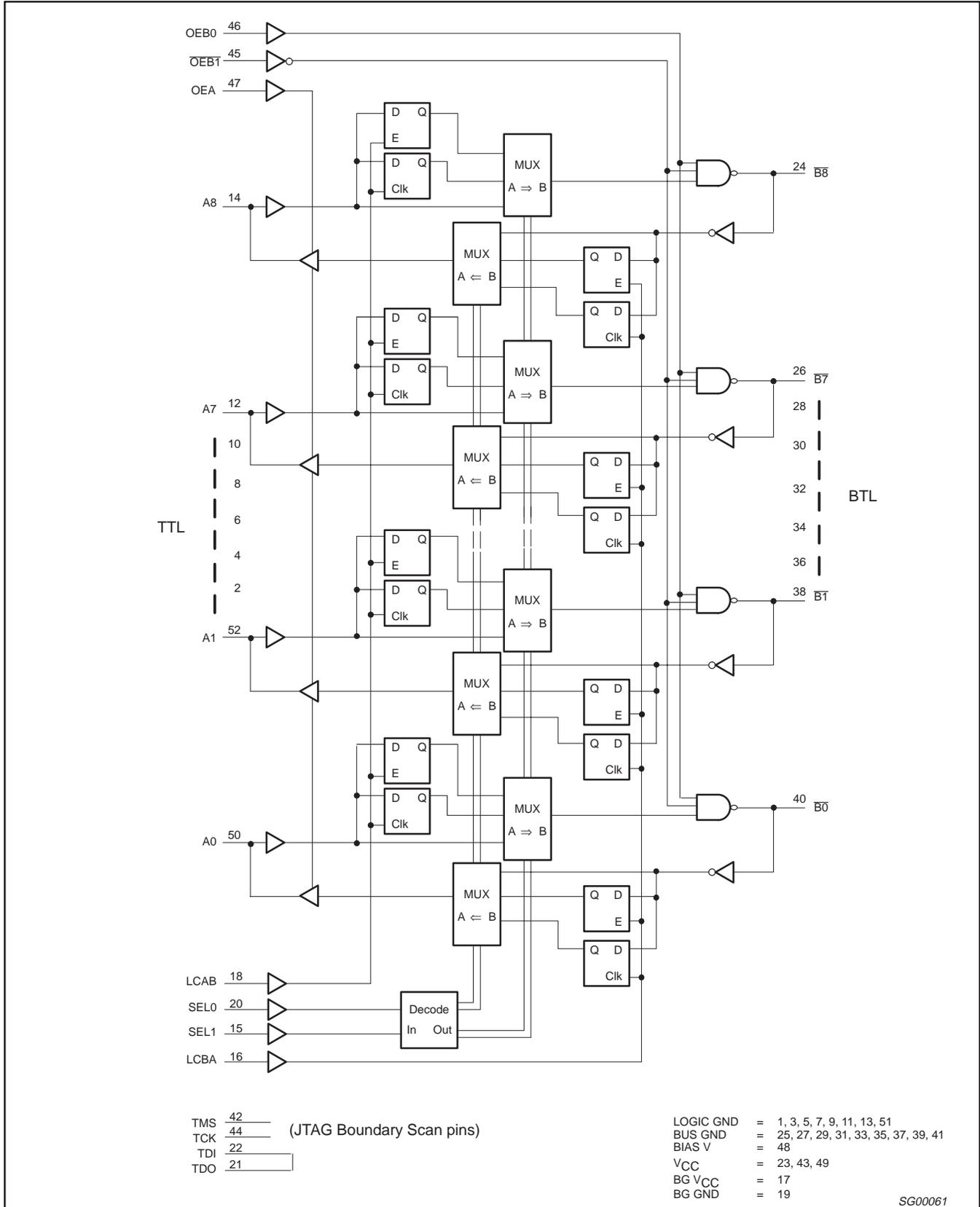
- H = High voltage level
- L = Low voltage level
- l = Low voltage level one set-up time prior to the Low-to-High LCXX transition
- h = High voltage level one set-up time prior to the Low-to-High LCXX transition
- X = Don't care

- Z = High-impedance (OFF) state
- = Input not externally driven
- ↑ = Low-to-High transition
- H\*\* = Goes to level of pull-up voltage
- Bn\* = Precaution should be taken to ensure B inputs do not float. If they do, they are equal to Low state.
- Disable = OEB0 is Low or OEB1 is High.

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## LOGIC DIAGRAM



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## ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
$V_{CC}$	Supply voltage		-0.5 to +4.6	V
$V_{IN}$	Input voltage	A10 – A16, OE $\overline{B}$ 0, OE $\overline{B}$ $\overline{n}$ , OEAn	-0.5 to +7.0	V
		$\overline{B}$ 0 – $\overline{B}$ 8	-0.5 to +3.5	
$I_{IN}$	Input current	$V_{IN} < 0$	-50	
$V_{OUT}$	Voltage applied to output in High output state		-0.5 to +7.0	V
$I_{OUT}$	Current applied to output in Low output state/High output state	A00 – A08	64, -64	mA
		$\overline{B}$ 0 – $\overline{B}$ 8	200	
$T_{STG}$	Storage temperature		-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	COMMERCIAL LIMITS $V_{CC} = 3.3V \pm 10\%$ ; $T_{amb} = -40$ to $+85^\circ C$			UNIT
		MIN	TYP	MAX	
$V_{CC}$	Supply voltage	3.0	3.3	3.6	V
$V_{IH}$	High-level input voltage	Except $\overline{B}$ 0– $\overline{B}$ 8	2.0		V
		$\overline{B}$ 0 – $\overline{B}$ 8	1.62	1.55	
$V_{IL}$	Low-level input voltage	Except $\overline{B}$ 0– $\overline{B}$ 8		0.8	V
		$\overline{B}$ 0 – $\overline{B}$ 8		1.47	
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current	A00 – A08		-32	mA
$I_{OL}$	Low-level output current	A00 – A08		+32	mA
		$\overline{B}$ 0 – $\overline{B}$ 8		100	
$C_{OB}$	Output capacitance on B port		6	7	pF
$T_{amb}$	Operating free-air temperature range	0		+70	°C

## LIVE INSERTION SPECIFICATIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	TYP	MAX	
$V_{BIASV}$	Bias pin voltage	Voltage difference between the Bias voltage and $V_{CC}$ after the PCB is plugged in.		0.5	V
$I_{BIASV}$	Bias pin ( $I_{BIASV}$ ) input DC current	$V_{CC} = 0$ V, Bias V = 3.6V		1.2	mA
		$V_{CC} = 3.3$ V, Bias V = 3.6V		10	$\mu$ A
$\overline{V}_{Bn}$	Bus voltage during prebias	$\overline{B}$ 0 – $\overline{B}$ 8 = 0V, Bias V = 3.3V	1.62	2.1	V
$I_{LM}$	Fall current during prebias	$\overline{B}$ 0 – $\overline{B}$ 8 = 2V, Bias V = 1.3 to 2.5V		1	$\mu$ A
$I_{HM}$	Rise current during prebias	$\overline{B}$ 0 – $\overline{B}$ 8 = 1V, Bias V = 3 to 3.6V	-1		$\mu$ A
$\overline{I}_{Bn}^{PEAK}$	Peak bus current during insertion	$V_{CC} = 0$ to 3.3V, $\overline{B}$ 0 – $\overline{B}$ 8 = 0 to 2.0V, Bias V = 2.7 to 3.6V, OE $\overline{B}$ 0 = 0.8V, $t_r = 2$ ns		10	mA
$I_{OLOFF}$	Power up current	$V_{CC} = 0$ to 3.3V, OE $\overline{B}$ 0 = 0.8V		100	$\mu$ A
		$V_{CC} = 0$ to 1.2V, OE $\overline{B}$ 0 = 0 to 5V		100	
$t_{GR}$	Input glitch rejection	$V_{CC} = 3.3$ V	1.0	1.35	ns

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## DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT
				MIN	TYP <sup>2</sup>	MAX	
$I_{OH}$	High level output current	$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_{IL} = \text{MAX}, V_{OH} = 1.9\text{V}$			100	$\mu\text{A}$
$I_{OFF}$	Power-off output current	$\overline{B0} - \overline{B8}$	$V_{CC} = 0\text{V}, V_{IL} = \text{MAX}, V_{OH} = 1.9\text{V}$			100	$\mu\text{A}$
			$V_{CC} = 0\text{V}, V_{IL} = \text{MAX}, V_{OH} = 1.9\text{V} @ 85^\circ\text{C}$			300	
$V_{OH}$	High-level output voltage	AO0 – AO8 <sup>3</sup>	$V_{CC} = \text{MIN to MAX}$	$V_{CC}-0.2$			V
			$V_{CC} = \text{MIN}; I_{OH} = -8\text{mA}$	2.4			V
			$V_{CC} = \text{MIN}; I_{OH} = -32\text{mA}$	2.0			V
$V_{OL}$	Low-level output voltage	AO0 – AO8 <sup>3</sup>	$V_{CC} = \text{MIN}; I_{OL} = 16\text{mA}$			0.4	V
			$V_{CC} = \text{MIN}; I_{OL} = 32\text{mA}$			0.5	V
		$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MIN}, I_{OL} = 4\text{mA}$	0.5			V
			$V_{CC} = \text{MIN}, I_{OL} = 100\text{mA}$	0.75	1.0	1.20	
$V_{IK}$	Input clamp voltage		$V_{CC} = \text{MIN}, I_I = I_{IK} = -18\text{mA}$		-0.85	-1.2	V
$I_I$	Input leakage current	Control pins	$V_{CC} = 3.6\text{V}; V_I = V_{CC} \text{ or GND}$			$\pm 1.0$	$\mu\text{A}$
		Control/AI0 – AI8	$V_{CC} = 0\text{V or } 3.6\text{V}; V_I = 5.5\text{V}$			10	
		AI0 – AI8	$V_{CC} = 3.6\text{V}; V_I = V_{CC}$			1	
		Note 4	$V_{CC} = 3.6\text{V}; V_I = 0\text{V}$			-5	
$I_{IH}$	High-level input current	$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_I = 1.9\text{V}$			100	$\mu\text{A}$
			$V_{CC} = \text{MAX}, V_I = 3.5\text{V}, \text{note } 5$	100			mA
			$V_{CC} = \text{MAX}, V_I = 3.75\text{V} @ -40^\circ\text{C}$	100			
$I_{IL}$	Low-level input current	$\overline{B0} - \overline{B8}$	$V_{CC} = \text{MAX}, V_I = 0.75\text{V}$			-100	$\mu\text{A}$
$I_{OZH}$	Off-state output current	AO0 – AO8	$V_{CC} = \text{MAX}, V_O = 3\text{V}$			5	$\mu\text{A}$
$I_{OZL}$	Off-state output current	AO0 – AO8	$V_{CC} = \text{MAX}, V_O = 0.5\text{V}$			-5	$\mu\text{A}$
$I_{CC}$	Supply current (total)	$I_{CCH}$ B to A	$V_{CC} = \text{MAX}, \text{outputs High}$		18	32	mA
		$I_{CCL}$ B to A	$V_{CC} = \text{MAX}, \text{outputs Low}$		22	37	mA
		$I_{CCH}$ A to B	$V_{CC} = \text{MAX}, \text{outputs High}$		11	16	mA
		$I_{CCL}$ A to B	$V_{CC} = \text{MAX}, \text{outputs Low}$		11	16	mA
		$I_{CCZ}$	$V_{CC} = \text{MAX}$		18	32	mA

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operation conditions for the applicable type.
- All typical values are at  $V_{CC} = 3.3\text{V}, T_A = 25^\circ\text{C}$ .
- Due to test equipment limitations, actual test conditions are  $V_{IH} = 1.8\text{V}$  and  $V_{IL} = 1.3\text{V}$  for the B side.
- Unused pins are at  $V_{CC}$  or GND.
- For B port input voltage between 3 and 5 volt;  $I_{IH}$  will be greater than 100mA but the part will continue to function normally (clamping circuit is active). This is not a tested condition.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	B TO A SPECIFICATIONS					UNIT
			T <sub>amb</sub> = +25°C, V <sub>CC</sub> = 3.3V,			T <sub>amb</sub> = -40 to +85°C, V <sub>CC</sub> = 3.3V±10%,		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 4	120	150				MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (thru mode) Bn to An	Waveform 1, 2	2.8 3.0	4.3 4.5	5.9 6.0	2.2 2.6	6.8 7.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (transparent latch) Bn to An	Waveform 1, 2	2.8 3.4	4.9 5.0	7.0 6.6	1.8 2.8	8.4 7.8	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LCBA to An (latch)	Waveform 1, 2	7.7 7.5	10.2 10.1	13.0 12.9	6.1 6.1	15.6 15.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LCBA to An (register)	Waveform 1, 2	2.7 3.0	4.2 4.5	5.7 6.1	2.1 2.4	6.7 6.9	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SEL0 or SEL1 to An (inverting)	Waveform 1, 2	2.9 1.9	5.8 5.8	9.1 10.4	2.2 1.2	10.5 11.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SEL0 or SEL1 to An (non-inverting)	Waveform 1, 2	2.0 2.8	5.9 5.6	10.3 8.8	1.4 2.2	12.3 10.0	ns
t <sub>PZH</sub> t <sub>PHZ</sub>	Output enable time from High or Low OEA to An	Waveform 5, 6	3.0 4.0	4.4 5.6	5.7 7.3	2.6 3.2	6.6 8.3	ns
t <sub>PZL</sub> t <sub>PLZ</sub>	Output disable time to High or Low OEA to An	Waveform 5, 6	2.6 1.4	4.0 2.6	5.4 3.7	2.1 1.0	6.0 4.4	ns
t <sub>TLH</sub> t <sub>THL</sub>	Output transition time, An Port 10% to 90%, 90% to 10%	Test Circuit and Waveforms				0.2 0.1	2.0 1.2	ns
t <sub>SK(o)</sub>	Output to output skew for multiple channels <sup>1</sup>	Waveform 3		0.5	1.0		1.5	ns
t <sub>SK(p)</sub>	Pulse skew <sup>2</sup>  t <sub>PHL</sub> - t <sub>PLH</sub>   <sub>MAX</sub>	Waveform 2		0.5	1.0		1.5	ns

NOTES:

1. |t<sub>P<sub>N</sub>actual</sub> - t<sub>P<sub>M</sub>actual</sub>| for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V<sub>CC</sub>, loading, etc.). t<sub>SK</sub>(0) compares t<sub>PLH</sub> on a given path to t<sub>PLH</sub> on any other path or compares t<sub>PHL</sub> on a given path to t<sub>PHL</sub> on any other path.
2. t<sub>SK</sub>(p) is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A TO B 9 Ω LOAD SPECIFICATIONS					UNIT
			T <sub>amb</sub> = +25°C, V <sub>CC</sub> = 3.3V,			T <sub>amb</sub> = -40 to +85°C, V <sub>CC</sub> = 3.3V±10%,		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (thru latch) An to Bn	Waveform 1, 2	1.4 1.3	2.6 2.5	3.8 3.8	1.0 1.0	4.9 4.2	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (transparent latch) An to Bn	Waveform 1, 2	1.7 2.0	2.9 3.5	4.2 5.0	1.0 1.5	5.4 5.7	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LCAB to Bn (latch)	Waveform 1, 2	8.8 8.4	11.6 11.0	14.5 13.7	6.7 6.7	17.9 16.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LCAB to Bn (register)	Waveform 1, 2	2.3 2.5	3.6 4.0	5.0 5.4	1.4 1.9	6.2 6.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SEL0 or SEL1 to Bn (inverting)	Waveform 1, 2	2.3 1.3	3.8 4.8	5.5 8.8	1.2 1.0	7.0 9.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SEL0 or SEL1 to Bn (non-inverting)	Waveform 1, 2	2.0 2.6	4.4 4.3	7.2 6.1	1.1 1.7	8.5 7.6	ns
t <sub>PLH</sub> t <sub>PHL</sub>	OEBn to Bn	Waveform 1, 2	1.2 1.9	2.9 3.3	4.8 4.7	1.0 1.2	5.8 6.4	ns
t <sub>TLH</sub> t <sub>THL</sub>	Output transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms				1.2 0.4	3.0 1.5	ns
t <sub>SK(o)</sub>	Output to output skew for multiple channels <sup>1</sup>	Waveform 3		0.4	1.0		2.0	ns
t <sub>SK(p)</sub>	Pulse skew <sup>2</sup> $ t_{PHL} - t_{PLH} _{MAX}$	Waveform 2		0.3	1.0		1.5	ns

NOTES:

1.  $|t_{PNactual} - t_{PMactual}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V<sub>CC</sub>, loading, etc.). t<sub>SK</sub> (0) compares t<sub>PLH</sub> on a given path to t<sub>PLH</sub> on any other path or compares t<sub>PHL</sub> on a given path to t<sub>PHL</sub> on any other path.
2. t<sub>SK</sub>(p) is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	A TO B 16.5 Ω LOAD SPECIFICATIONS					UNIT
			T <sub>amb</sub> = +25°C, V <sub>CC</sub> = 3.3V,			T <sub>amb</sub> = -40 to +85°C, V <sub>CC</sub> = 3.3V±10%,		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (thru latch) An to Bn	Waveform 1, 2	1.4 1.2	2.7 2.4	3.9 3.6	1.0 1.0	5.0 4.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay (transparent latch) An to Bn	Waveform 1, 2	1.8 2.0	3.0 3.2	4.2 4.7	1.0 1.4	5.6 5.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LCAB to Bn (latch)	Waveform 1, 2	8.6 8.0	11.4 10.6	14.2 13.3	6.5 6.4	17.5 16.1	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay LCAB to Bn (register)	Waveform 1, 2	2.2 2.3	3.5 3.7	4.8 5.1	1.2 1.7	6.1 5.9	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SEL0 or SEL1 to Bn (inverting)	Waveform 1, 2	2.6 1.4	4.5 4.4	6.7 7.7	1.5 1.1	8.1 8.4	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay SEL0 or SEL1 to Bn (non-inverting)	Waveform 1, 2	2.2 2.3	4.5 4.0	6.9 5.8	1.4 1.5	8.2 6.9	ns
t <sub>PLH</sub> t <sub>PHL</sub>	OEB0 to Bn	Waveform 1, 2	1.8 1.7	3.1 2.9	4.4 4.2	1.0 1.0	5.8 6.0	ns
t <sub>TLH</sub> t <sub>THL</sub>	Output transition time, $\overline{Bn}$ Port (1.3V to 1.8V)	Test Circuit and Waveforms				1.2 0.4	3.0 1.5	ns
t <sub>SK(o)</sub>	Output to output skew for multiple channels <sup>1</sup>	Waveform 3		0.5	1.0		2.0	ns
t <sub>SK(p)</sub>	Pulse skew <sup>2</sup> $ t_{PHL} - t_{PLH} _{MAX}$	Waveform 2		0.5	1.0		1.5	ns

NOTES:

1.  $|t_{PNactual} - t_{PMactual}|$  for any data input to output path compared to any other data input to output path where N and M are either LH or HL. Skew times are valid only under same test conditions (temperature, V<sub>CC</sub>, loading, etc.). t<sub>SK</sub> (0) compares t<sub>PLH</sub> on a given path to t<sub>PLH</sub> on any other path or compares t<sub>PHL</sub> on a given path to t<sub>PHL</sub> on any other path.
2. t<sub>SK</sub>(p) is used to quantify duty cycle characteristics. In essence it compares the input signal duty cycle to the corresponding output signal duty cycle (50MHz input frequency and 50% duty cycle, tested on data paths only).

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## AC SETUP REQUIREMENTS (Commercial)

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			$T_{amb} = +25^{\circ}\text{C}, V_{CC} = 3.3\text{V},$		$T_{amb} = -40 \text{ to } +85^{\circ}\text{C},$	
			$V_{CC} = 3.3\text{V} \pm 10\%,$			
			$C_L = 50\text{pF (A side)} / C_D = 30\text{pF (B side)}$ $R_L = 500\Omega \text{ (A side)} / R_U = 16.5\Omega \text{ (B side)}$			
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time An to LCAB	Waveform 4	1.3 1.3		1.5 1.5	ns
$t_h(H)$ $t_h(L)$	Hold time An to LCAB	Waveform 4	1.0 1.0		1.0 1.0	ns
$t_s(H)$ $t_s(L)$	Setup time $\overline{Bn}$ to LCBA	Waveform 4	5.0 4.0		6.0 4.5	ns
$t_h(H)$ $t_h(L)$	Hold time $\overline{Bn}$ to LCBA	Waveform 4	0.0 0.0		0.0 0.0	ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low LCAB or LCBA	Waveform 4	3.0 3.0		3.0 3.0	ns

## AC WAVEFORMS

**Waveform 1. Propagation Delay for Data or Output Enable to Output**

**Waveform 2. Propagation Delay for Data or Output Enable to Output**

**Waveform 3. Output to Output Skew**

**Waveform 4. Setup and Hold Times, Pulse Widths and Maximum Frequency**

**Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level**

**Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

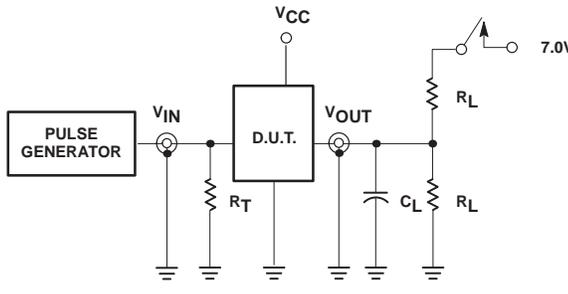
**NOTE:**  $V_M = 1.55\text{V}$  for  $\overline{Bn}$ ,  $V_M = 1.5\text{V}$  for all others.  
The shaded areas indicate when the input is permitted to change for predictable output performance.

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# 9-bit BTL 3.3V latched/registered/pass-thru Futurebus+ transceiver

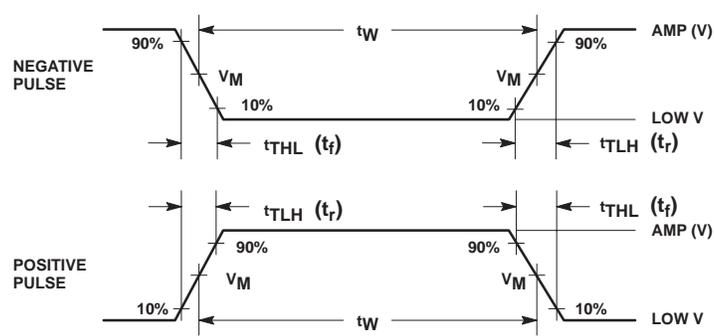
FBL2031

## TEST CIRCUIT AND WAVEFORMS



**Test Circuit for 3-State Outputs on A Port**

The circuit shows a Pulse Generator connected to the input  $V_{IN}$  of a D.U.T. through a termination resistor  $R_T$ . The output  $V_{OUT}$  is connected to a load resistor  $R_L$  and a load capacitor  $C_L$ . A switch is connected to  $V_{OUT}$  and can be set to 7.0V or ground. The supply voltage is  $V_{CC}$ .



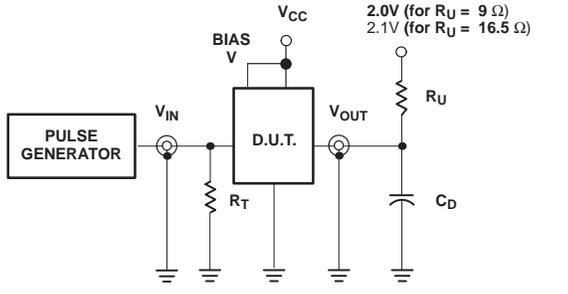
**Input Pulse Definitions**

The diagrams show waveforms for Negative and Positive pulses. Key parameters include pulse width  $t_W$ , high/low levels  $V_M$ , and transition times  $t_{THL}$  and  $t_{TLH}$  measured between 10% and 90% levels. The pulse levels are labeled as AMP (V) and LOW V.

$V_M = 1.55V$  for  $\overline{Bn}$ ,  $V_M = 1.5V$  for all others.

**SWITCH POSITION**

TEST	SWITCH
$t_{PLZ}$ , $t_{PZL}$	closed
All other	open



**Test Circuit for Outputs on B Port**

The circuit shows a Pulse Generator connected to the input  $V_{IN}$  of a D.U.T. through a termination resistor  $R_T$ . The output  $V_{OUT}$  is connected to a pull-up resistor  $R_U$  and a load capacitor  $C_D$ . A BIAS V input is also shown. The supply voltage is  $V_{CC}$ . Values for  $R_U$  are specified as 2.0V for  $R_U = 9\Omega$  and 2.1V for  $R_U = 16.5\Omega$ .

Family FB+	INPUT PULSE REQUIREMENTS					
	Amplitude	Low V	Rep. Rate	$t_W$	$t_{TLH}$	$t_{THL}$
A Port	3.0V	0.0V	1MHz	500ns	2.5ns	2.5ns
B Port	2.0V	1.0V	1MHz	500ns	2.0ns	2.0ns

**DEFINITIONS:**  
 $R_L$  = Load Resistor; see AC CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.  
 $C_D$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.  
 $R_U$  = Pull up resistor; see AC CHARACTERISTICS for value.

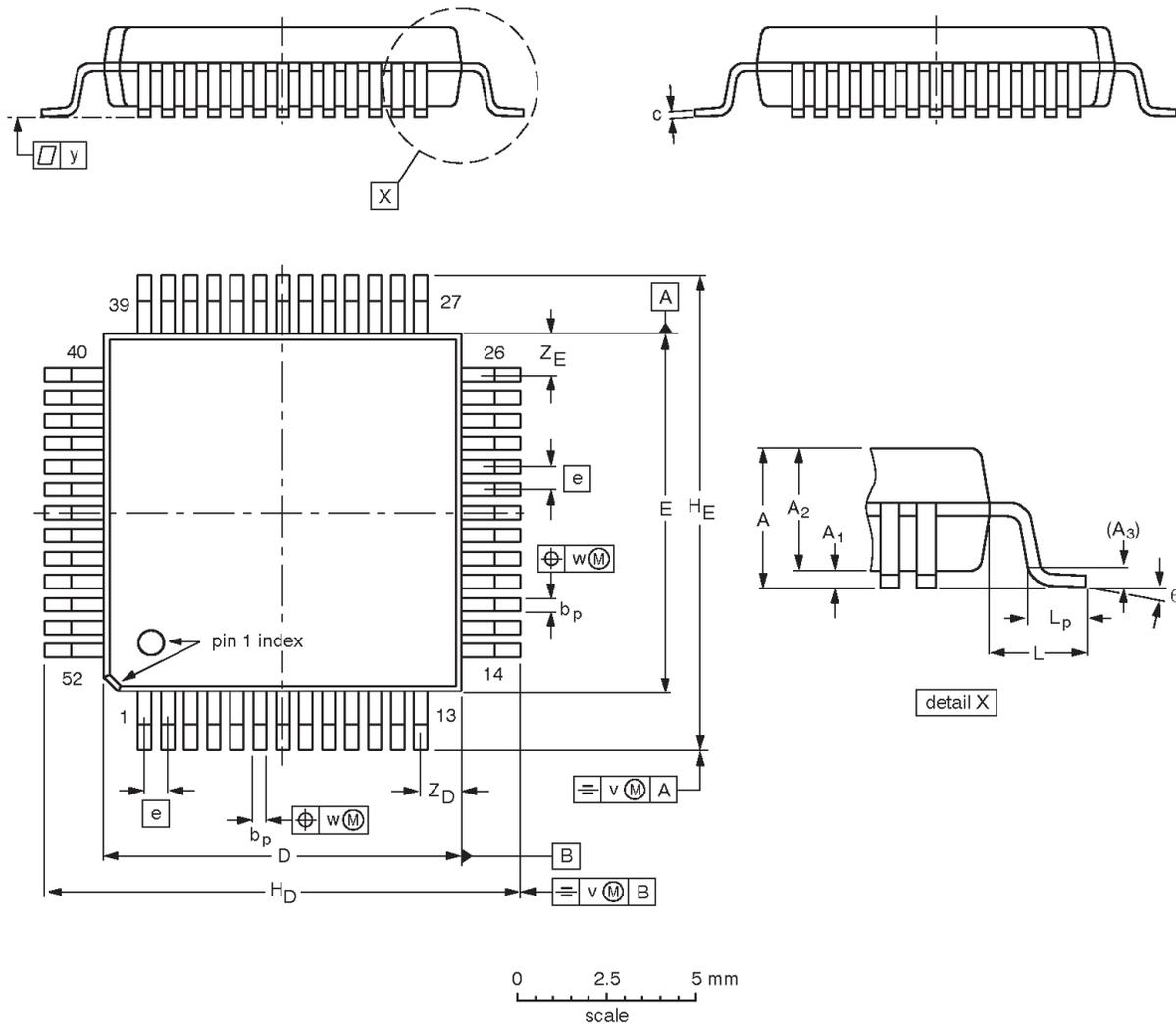
SG00063

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QFP52: plastic quad flat package; 52 leads (lead length 1.6 mm); body 10 x 10 x 2.0 mm

SOT379-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	2.45	0.45 0.25	2.10 1.95	0.25	0.38 0.22	0.23 0.13	10.1 9.9	10.1 9.9	0.65	13.45 12.95	13.45 12.95	1.60	0.95 0.65	0.20	0.12	0.10	1.24 0.95	1.24 0.95	7° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT379-1	135E04	MS-022				-99-12-27- 00-01-19

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**NOTES**

# 9-bit BTL 3.3V latched/registered/pass-thru Futurebus+ transceiver

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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