APPLICATION NOTE

AN92001
Low RF-emission applications with a P83CE654 microcontroller

April 1992

Philips
Semiconductors

PHILIPS

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EIE/AN92001

1.0 INTRODUCTION

Quite recently customers asked for dedicated 8-bit microcontrollers at high clockrates which would not cause Radio Frequency (RF-) disturbances in consumer and communication applications, e.g., keyboard control, tuning, etc. . .

Up to now either a slower 4-bit microcontroller was used or a more modern 8-bit microcontroller is in use with additional RF-shielding and filtering measures.

With a car radio manufacturer, a bargain was set for new (EMC friendly) 8-bit microcontroller such that the product would maintain equal receiving performance with more control features. The new receiver would then only be modified for the microcontroller part.

To set the emission requirements, for a microcontroller in this application, the measurement technique described int eh application note, EIE/AN91001 *"Workbench EMC evaluation method"* was used and applied to the existing receiver in which the new microcontroller has to fit in.

Later on, the same technique was used to verify the basic and modified samples which contained one or more measures to reduce RF-emission.

Each (mask) shrinking event will cause circuits to become faster and produce more RF-disturbances for these kind of appliances. As such, more EMC measures need to be taken after each shrinking event to maintain the above set emission requirements.

2.0 MEASURES TO REDUCE RF-EMISSION

Up to now, evident measures are known to reduce RF-emission. Within a few years time, new techniques will mature to keep pace with shrinking actions.

So far, it is only interesting to take emission reducing measures on-chip for a microcontroller when there are no external ROM, RAM or (E)EPROM buses. The externally required data- and address-buses will cause much more RF-radiation, when used in a non-shielded way.

We've restricted ourselves to stand-alone controllers, which can control most functions locally with, when required low speed serial buses, e.g., I^2C (100 kbit/s or 400 kbit/s with output-edge-control), or parallel communication to another controller.

To compare our results, reference is made to an existing standard microcontroller based on the INTEL 80C51-core mounted in a 40-pin DIL package.

Dedicated software has been used to allow true comparison between all microcontrollers in a defined application.

2.1 IC package

Density problems demand smaller packages to allow further integration of functions within a certain product size. It was decided to take the Quad Flat Pack (QFP) 44, because it was the lowest pin number package available above 40 pins required to apply the circuit as stated above.

The advantage of this package is the smaller loop area enclosed by the currents running through the circuit. As a result, direct radiation will e reduced. The worst-case area difference between the package sizes is:

DIL 40: $48.46 \times 15.24 \times 4.3$ mm ($l \times w \times h$, h = PCB + die-path height)
diagonal: 50.8 mm
looparea: 218.5 mm^2

QFP 44: $11.4 \times 8.8 \times 1.2$ mm ($l \times w \times h$, h = die-path height)
diagonal: 14.4 mm
looparea: 17.3 mm^2

When package radiation is considered only, the magnetic dipole moment produced by the package will be reduced by a factor of 12.6, which can give a decrease in electromagnetic emission of about 22dB.

External supply decoupling capacitors can be places more closely to the pins where needed. The latter will shorten the length of the current path between V_{DD} and V_{SS}, thus resulting in a lower voltage drop appearing in-between reference point taken on the PCB. Considering this, the current path reduction will be a factor of 4.5 which would result in an RF-emission reduction of about 12dB. One should consider that also I/O-pins will contribute to the RF-emission.

Practical radiation figures have shown a decrease of about 12dB.

2.2 IC pinning

As already given above, supply and I/O pinning will determine emission performance, due to the fact that radiation is determined by the way currents flow through a device. For some years it is known that each output pin should be embedded in-between a V_{DD} and a V_{SS} pin. As such, the 3 one-byte wide buses would need $3 \times (2 \times 8 + 1)$ pins (O, V_{DD}, V_{SS}), equals at least 51 pins. For such a device this seems unpractical.

The advantage of such a pinning will be that currents will always flow through adjacent leadframe fingers, and as such, emission will be absolutely minimal. For this application, I/O will commonly occur at low frequencies, and as such, their contribution to RF-emission will be low. In CMOS applications these currents will mainly occur during transitions by charging and discharging the output load.

A more serious contribution will arise from the ground-bounce or supply-bounce which will occur between the PCB-reference and the IC's substrate. This disturbance voltage will be superimposed to all I/Os which are either coupled to V_{SS} or V_{DD}. When these lines are long, longer than the path involved for supply decoupling, their contribution to radiation can be high. The disturbance source, being the supply- or ground-bounce voltage, has a negligible impedance (ω.L, L = leadfinger + bonding wire inductance) and will be difficult to filter by using simple and cheap components such as capacitors. More often, radiation will increase by such measures due to the increases current through these I/Os.

The most effective action will be the use of several ground and supply pins. The ground pins must be spread around the circumference of the package while the supply pins need to be the adjacent to these grounds to benefit the mutual coupling in-between. This mutual coupling reduces the 'effective' series inductance with the external decoupling capacitor.

With the DIL-40, pin 20 is the V_{SS} pin, and pin 40 is the supply pin, V_{DD}. The I/O pins are randomly located. With the QFP-44, for the V_{SS} the following pins are selected: 6, 16, 28, 39; the supply pins are: 17, (for I/O) and 38 (for the core).

Another cause for ground-bounce can be the X-tal oscillator's output with its external capacitance. Normally, this contribution can be reduced by adding some series impedance with the output and changing the capacitor's values such that the X-tal circuit operation remains within its linear range with sufficient amplitude.

All together, the ground-bounce, which will be emitted by the I/O, can be reduced by a factor of 4 (4 gnd pins QFP versus 1 gnd pin DIL), assuming random I/O current distributions. Individual decoupling of the I/O and core supply will dampen the supply bounce even further.

As such, these measures will reduce emissions further by some 12dB. The expectation of even more drastic effects can be accounted for by the shorter leadframe finger lengths comparing DIL-40 to QFP-44.

2.3 On-chip decoupling measures

From the above, it will be clear that RF-emission will primarily come from the core and that the lower frequencies will be mainly caused by the I/O. For the latter output-edge-rate control can be considered, when the number of outputs are high compared to the number of V_{SS} and V_{DD} pins.

When core decoupling is integrated, the high frequency low energy currents can close their loop on silicon. As a result, these RF-currents will not flow through the leadframe any longer and will not add to any additional ground-bounce.

If the latter is implemented without further considerations, the effect can be quite negative. The original circuit design assumed that all charge (current) comes from the external decoupling capacitor. This charge (current) then, flows from the capacitor, through its leadwires, PCB traces, IC leadframe, interconnect to the circuit (that needed it) and then back. When on-chip decoupling is used, charge is there and switching will occur instantaneously.

In our case, most bus-driving circuits were re-designed such that waveforms maintain within their specifications under worst-case conditions (temperature, supply voltage, etc.).

The overall result is that on-chip decoupling will require little space due to the fact that all empty areas can be used, even within the circuit-blocks, and that bus-driving circuits can be made much smaller with respect to the present dimensions.

2.4 PCB design measures

The QFP-package and the pinning of the controller will only reduce the RF-emission when the PCB is laid out following some constraints.

An example of a good supply and ground plane layout is given in Figure 1. The microcontroller is mounted on the component side of a double layer PCB. The supply pairs V_{SS1}/V_{DD1} for the I/O supply and V_{SS3}/V_{DD2} for the core supply are connected directly to the ceramic chip capacitors C1 and C2, which are surface-mounted on the solder side. A short connection of V_{SS3}/V_{DD2} to the capacitor C2 minimizes loop inductance. Thus, the external supply current drawn by the core will flow in this loop mainly. This current path can be ensured by the insertion of an inductor (L2) in series to the +5V general supply. An equal action is taken for the I/O supply.

The implemented on-chip decoupling allows a separation between core and I/O-ports. The PCB layout shall use these V_{DD}/V_{SS} connections to minimize the loop areas in-between signal lines from each port pin to any load via the ground plane back to these V_{SS}/V_{DD} pins.

By applying these hints, V_{SS2} may be used as the return pin for ALE, PSEN, port0 and port2, because V_{SS2} is connected very near to them. V_{SS3} shall be used for the core supply mainly. V_{SS1} is nearest to lower part of port2, upper part of port3 and the crystal oscillator. Even though V_{SS1} may be the best return for port2 and port3, this pin shall in any case be used as return for the external crystal oscillator capacitors (not shown here). V_{SS4} is located nearest to the lower part of port3 and the whole port1, being the best return for these ports.

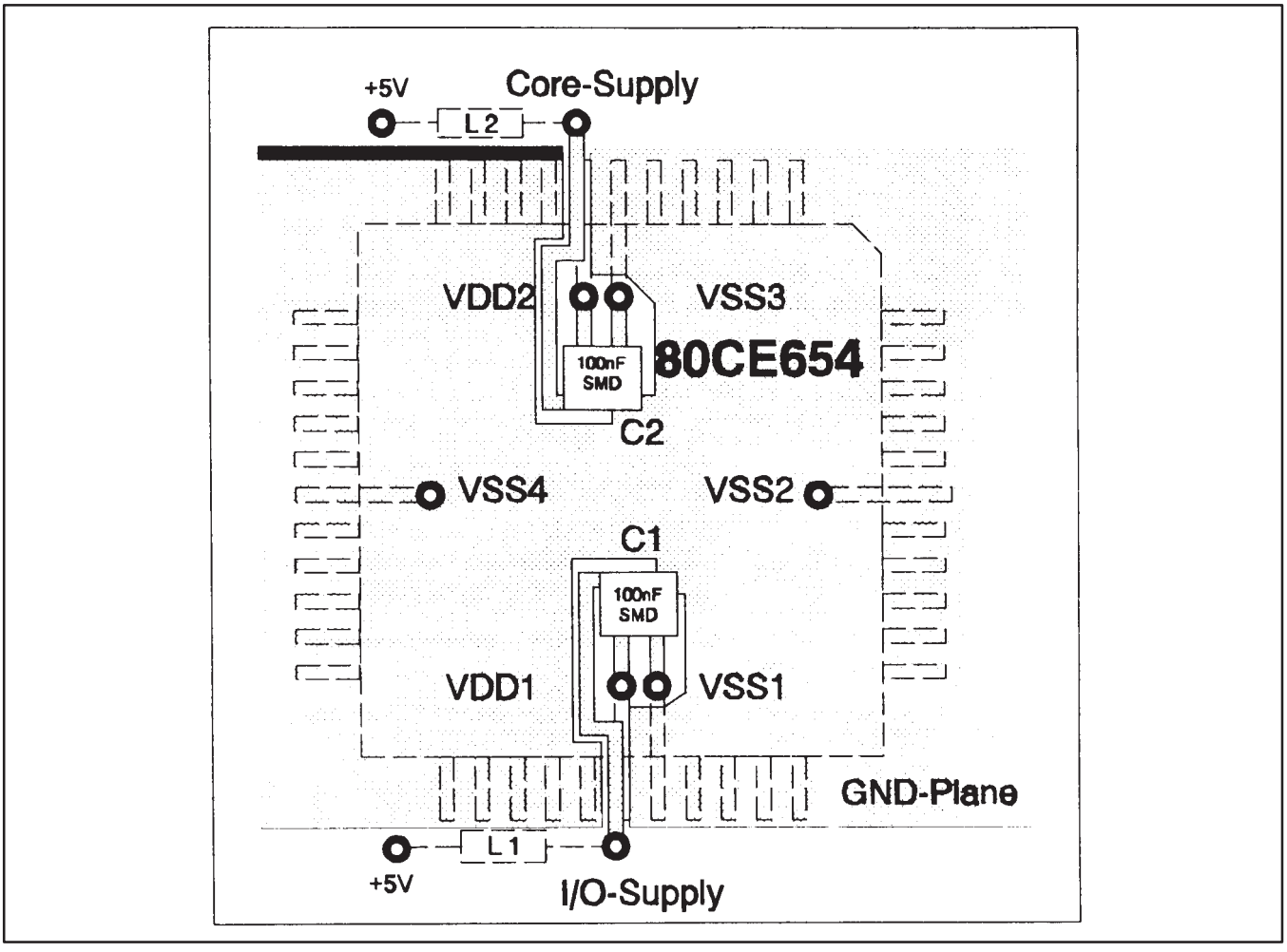


Figure 1.

3.0 FUTURE DEVELOPMENTS

Existing products are shrunk, to cut costs and increase complexity. Recent developments (SAC3 → SAC2 → SAC1, C300 → C250 → C200 and others) have demonstrated an upwards tendency in the RF-emission following shrinking when EMC is not considered. This means that the end in taking measures to reduce RF-emission has not been reached. further improvements are still possible and already considered for new products, such as:

- A PLL circuit, to replace the high-frequency Xtal oscillator
- Output-edge-control (application-dependent)
- Further circuit improvements on-chip, e.g., coplanar supply, decoupling measures within cell-blocks, multi-phase clock systems to prevent simultaneous switching

4.0 RESULTS

All measurements were carried out under the same conditions, using the same kind of PCB, with the same software and the same bus loadings, Figure 2.

The following applications were tested:

• 1	87C51	DIL40	12MHz Xtal	→ 0 dB(rel)
• 2	80C31	QFP44	but with 2 V_{SS} and only one V_{DD} connection, 12 MHz Xtal	→ 13 dB
• 3	83CE654	QFP44	with Address Latch Enable (ALE) active, 12 MHz Xtal	→ 32 dB
• 4	83CE654	QFP44	ALE off, 12 MHz Xtal	→ 50 dB
• 5	83CE654	QFP44	ALE off, externally 12 MHz, 500 mV sinewave	→ 54 dB

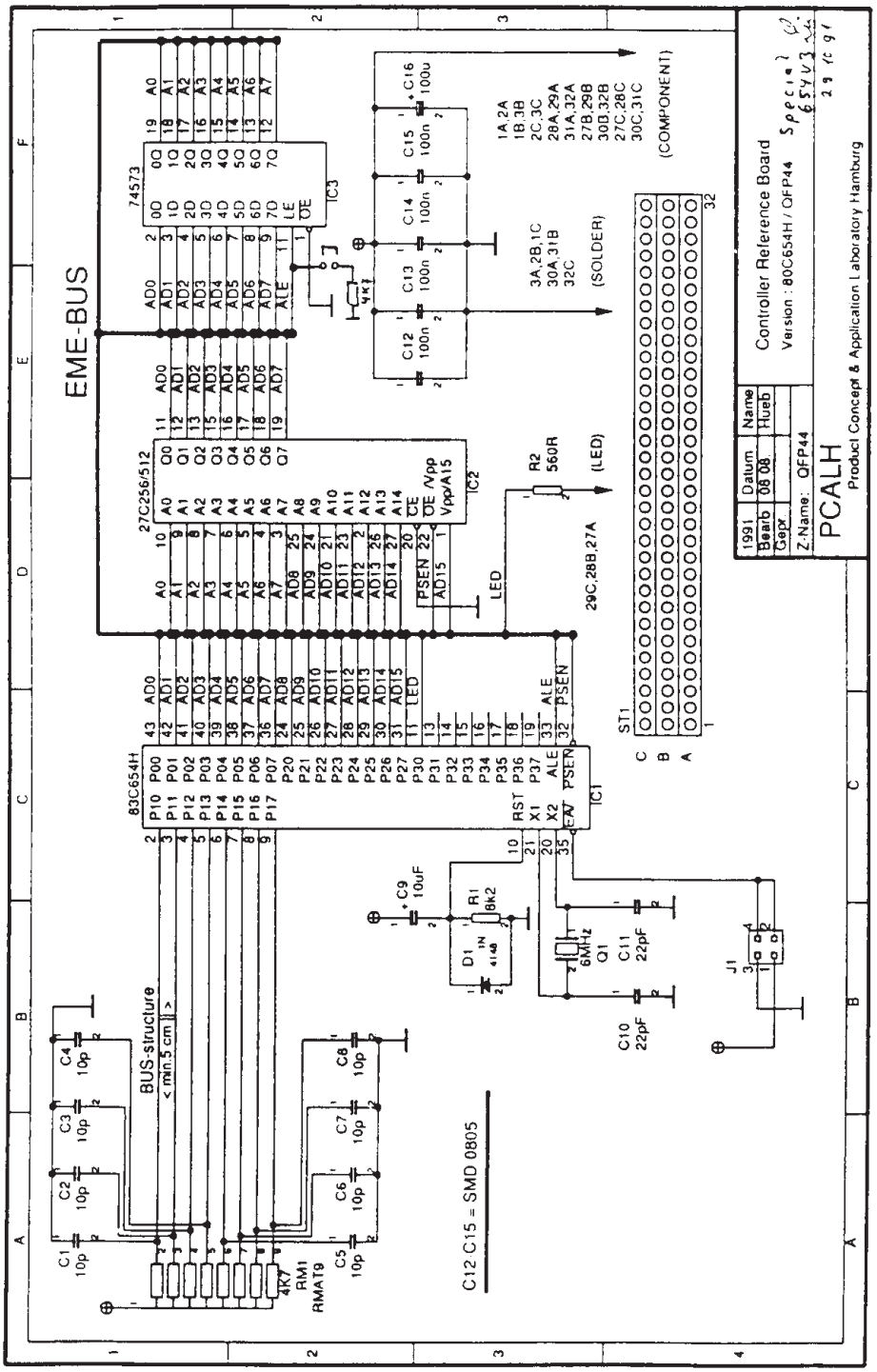

EME-BUS
83C654H
27C256/512
74573
IC1
IC2
IC3
ST1
R1 8k2
R2 560R
(LED)
(SOLDER)
(COMPONENT)
C9 10uF
C10 22pF
C11 22pF
Q1 6MHz
C12 100n
C13 100n
C14 100n
C15 100n
C16 100u
C1 10p
C2 10p
C3 10p
C4 10p
C5 10p
C6 10p
C7 10p
C8 10p
RM1 4K7
BUS-structure
< min.5 cm >
C12 C15 = SMD 0805
Controller Reference Board
Version : 80C654H / QFP44
PCALH
Product Concept & Application Laboratory Hamburg

Figure 2.

5.0 CONCLUSIONS

With the measures indicated in chapter 2, RF-emission can be reduced substantially, especially for stand-alone microcontroller applications. Up to now, a number of measures have been implemented which indicate an improvement of about 40dB in the FM region when changing from a DIL-40, annex 1 to a QFP-44 application, annex 4, taking into account minor additional supply measures. The inclusion of a PLL can make the improvement even further to about 50dB, annex 5.

With these measures, some 12 to 22 dB can be accounted for by the choice of the package, same 12 dB due to the pinning and the rest due to the internal measures.

The advantage of these measures can be easily wasted by insufficient measures on the PCB. Constraints are given in chapter 2.4.

When considering the reducing effects PCB layouts might have to RF emission, the following relative information needs to be considered:

- Single layer board → 0 dB (relative)
- Double layer board → 26 dB (best case)
- Multi-layer board → 44 dB (4-layer, best case)

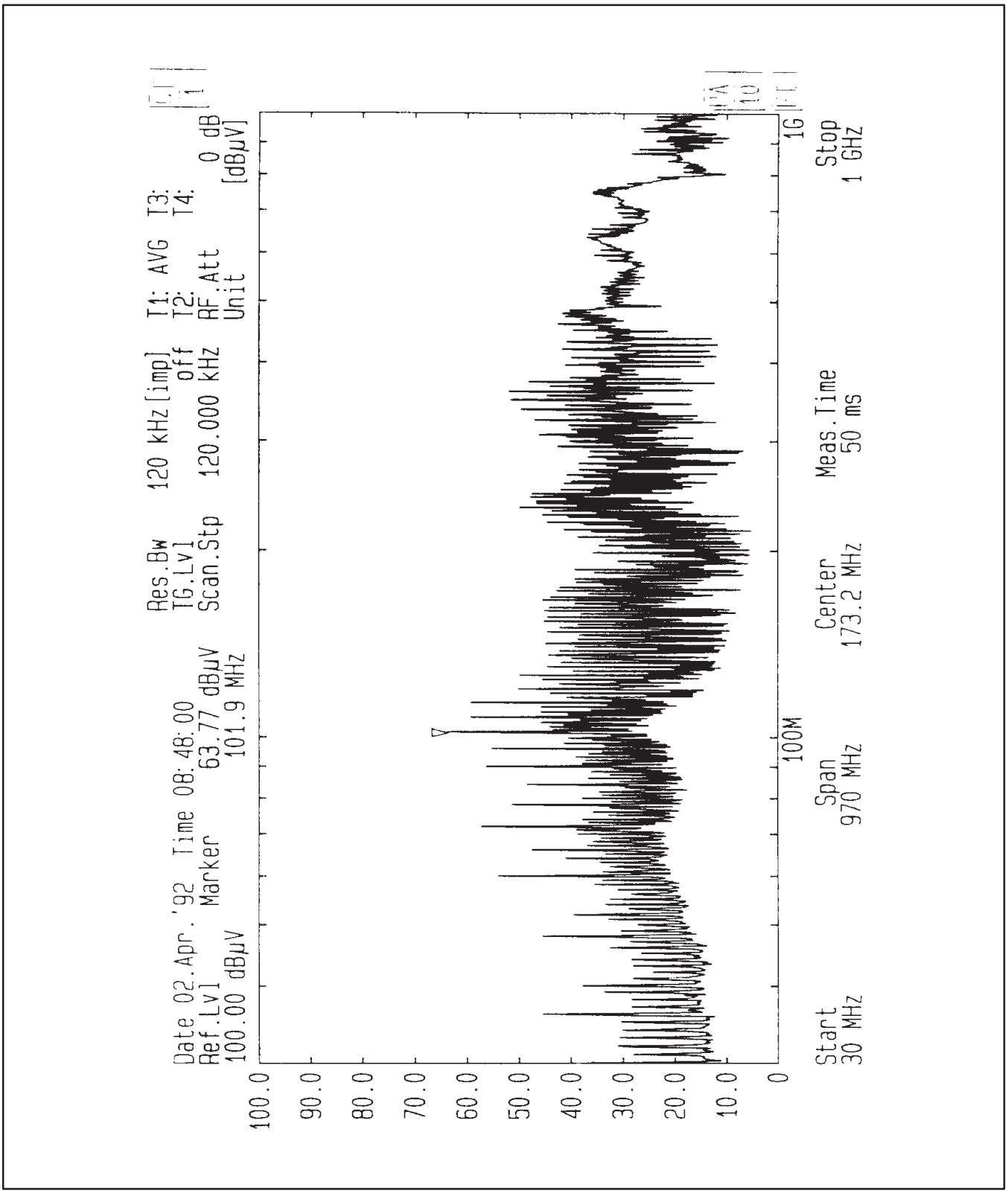
6.0 REFERENCES

[1] Syllabus of the design course *Fast digital and analog circuit design*, Philips CTT, 1991, Eindhoven.

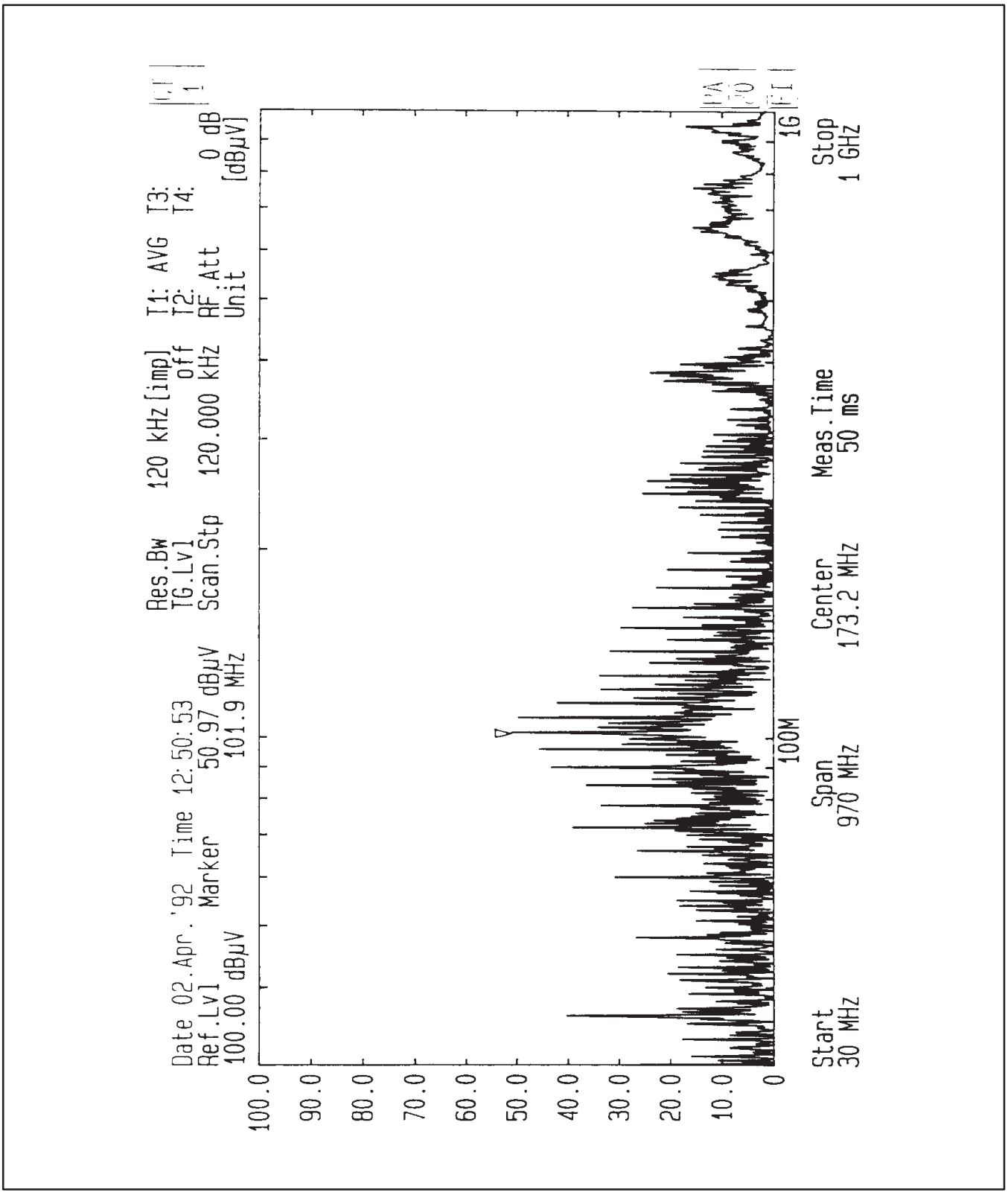
[2] *IC package outlines*, Philips Components, 1990, 12NC: 9398 175 80011.

[3] *Improvements in microcontrollers for a better EMC behaviour*, H. Schutte, EIE/IN90039 version 2, 1991.

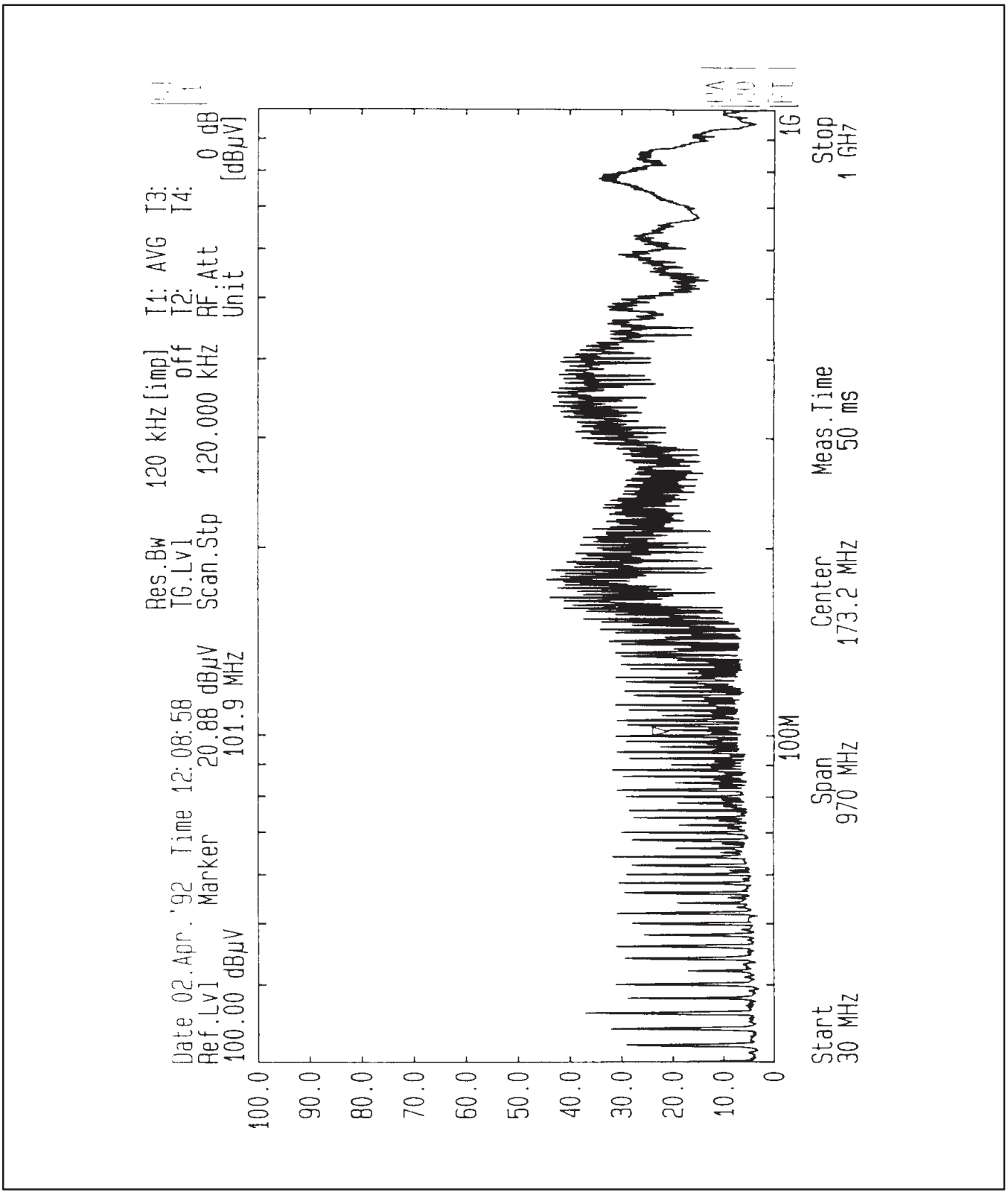
[4] *Investigations on EME improvements for the microcontrollers 8xCE592 and 8xCE598*, H.W. Lütjens, HKI/IR 92001, 1992.



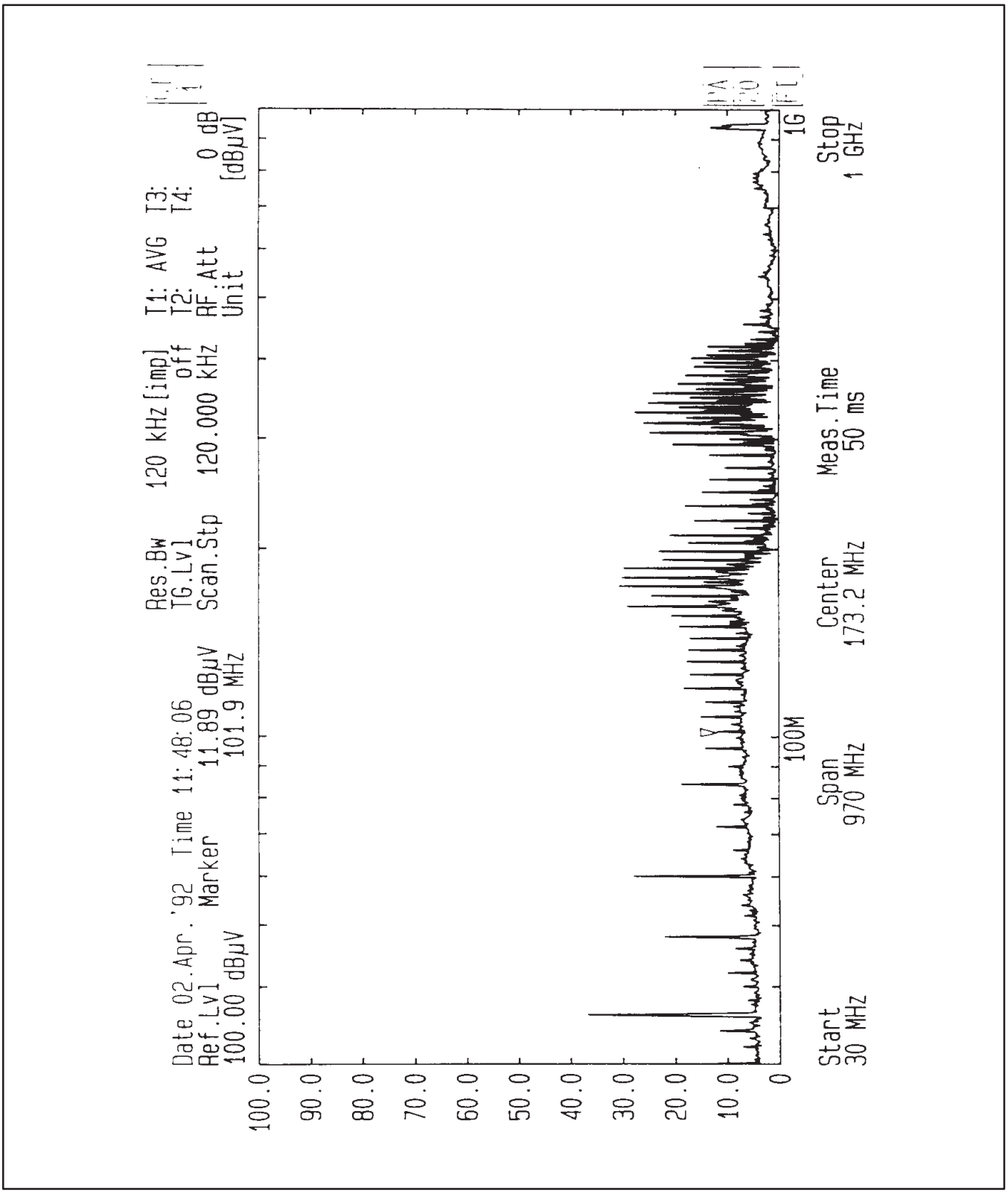
Annex 1. RF-emission from a 87C51, DIL-40, 12MHz Xtal



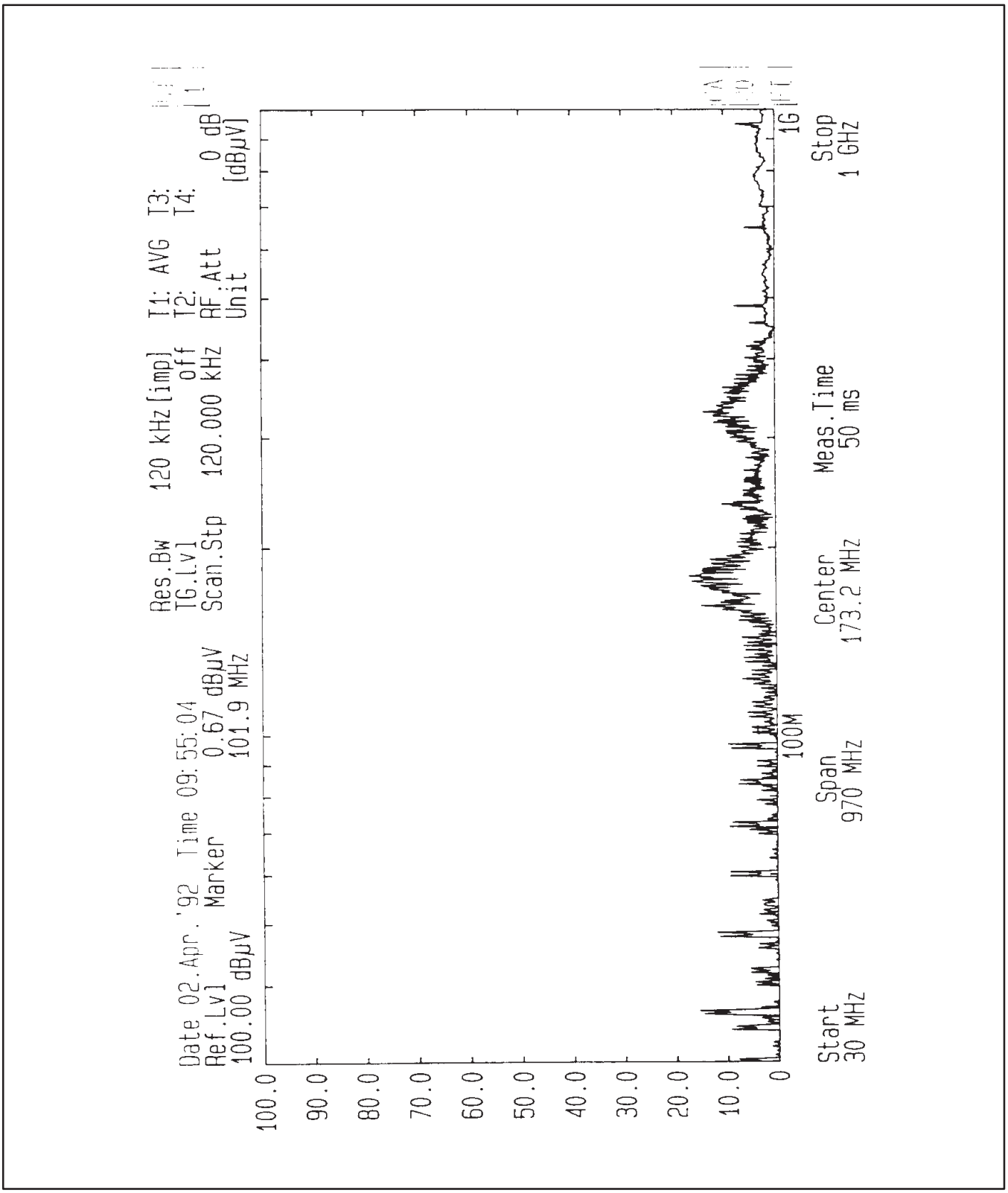
Annex 2. RF-emission from a 80C31, QFP-44, but with two V_{SS} and only one V_{DD} connection, 12MHz Xtal



Annex 3. RF-emission from a 83CE654, QFP-44, with Address Latch Enable (ALE) active, 12MHz Xtal. Four V_{SS} and two V_{DD} pins as given above.



Annex 4. RF-emission from a 83CE654, QFP-44, ALE off, 12MHz Xtal



Annex 5. RF-emission from a 83CE654, QFP-44, ALE off, externally 12MHz, 500mV sinewave

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