DSP96002

32-BIT IEEE FLOATING-POINT DUAL-PORT DSP

The DSP96002 is a single-chip, dual port, HCMOS, low-power, general purpose IEEE floating-point Digital Signal Processor (DSP) that features 1024 words of data RAM (equally divided into X data and Y data memory), 1024 words of full speed on-chip program RAM, two preprogrammed data ROMs, a dual channel DMA controller, special on-chip bootstrap hardware, and On-Chip Emulation (OnCE™) debug circuitry. The Central Processing Unit (CPU) consists of three 32-bit execution units operating in parallel. The DSP96002 has two identical memory expansion ports with control lines that facilitate interfacing to SRAMs, fast-access DRAMs, and Video RAMs (VRAMs). Each port can be transformed into a Host Interface (HI), which facilitates easy interfacing to other processors for multiprocessor applications. Linear arrays of DSP96002s can be implemented without glue logic. The MPU-style programming model and instruction set allow straightforward generation of efficient, compact code. The high speed of the DSP96002 makes it well-suited for high bandwidth and numerically intensive applications such as graphics, image, and numeric processing.

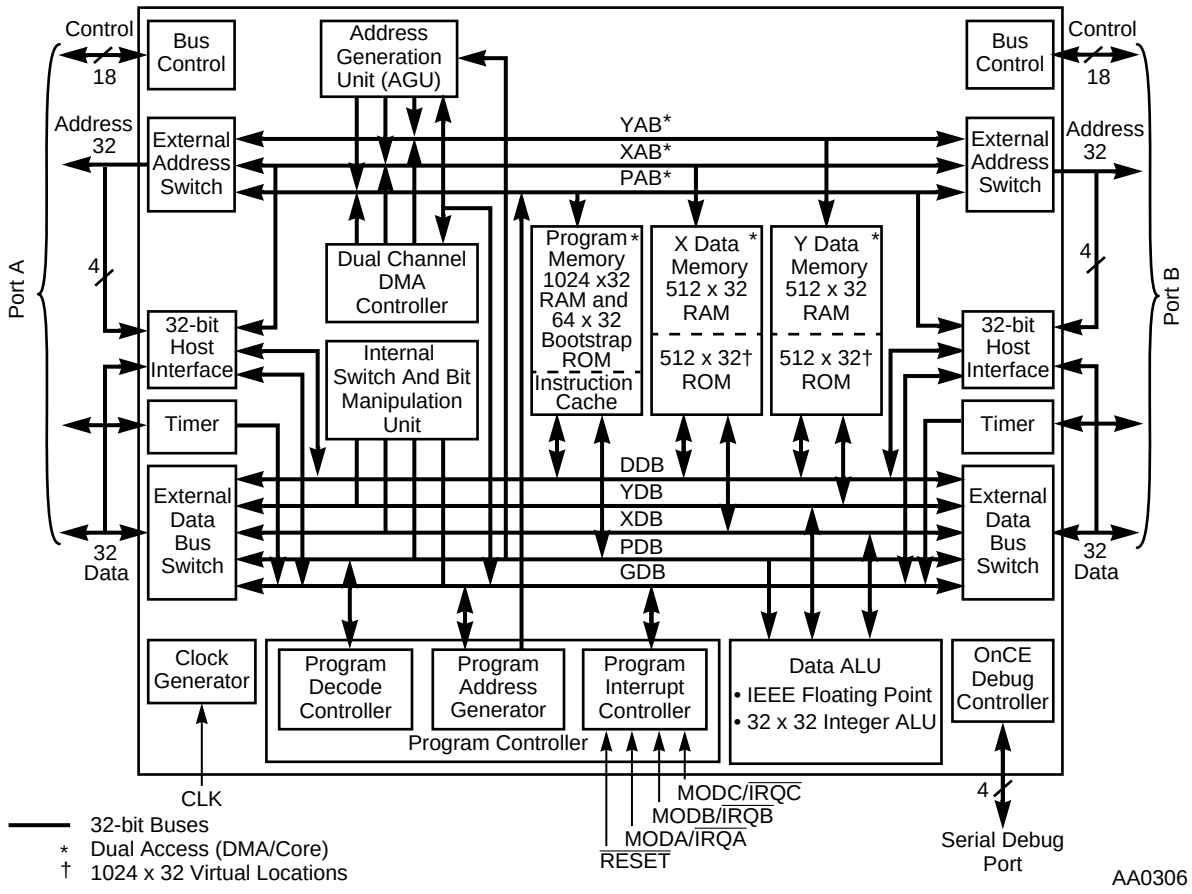

Figure 1 DSP96002 Block Diagram

DSP96002 FEATURES

- Digital signal processing core
  - Efficient 32-bit DSP engine
  - Conforms to IEEE 754-1985 standard for single precision (32-bit) and single extended precision (44-bit) arithmetic
  - Up to 20 million instructions per second (MIPS) at 40 MHz
  - Parallel operation of data ALU, Address Generation Unit (AGU), and program controller within the CPU allow more processing per instruction cycle
  - Single-cycle 32 x 32 bit parallel multiplier
  - Highly parallel instruction set with unique DSP addressing modes
  - Nested hardware DO loops
  - Instruction cache extended to operate as 4K byte (1K word)
  - Fast auto-return interrupts
  - Address buses:
    - One 32-bit unidirectional internal X memory Address Bus (XAB)
    - One 32-bit unidirectional internal Y memory Address Bus (YAB)
    - One 32-bit internal Program Address Bus (PAB)
    - Two 32-bit external address buses
  - Data buses:
    - One 32-bit bidirectional internal X memory Data Bus (XDB)
    - One 32-bit bidirectional internal Y memory Data Bus (YDB)
    - One 32-bit bidirectional internal Global memory Data Bus (GDB)
    - One 32-bit bidirectional internal DMA Data Bus (DDB)
    - One 32-bit bidirectional internal Program Data Bus (PDB)
    - Two 32-bit external data buses
  - MCU-like instruction set mnemonics make programming easier
- Memory
  - On-chip 1024 x 32 bit program RAM
  - Two independent on-chip 512 x 32 bit data RAMs
  - Two independent on-chip 1024 x 32 bit data ROMs (512 x 32 bit virtual memory)
  - On-chip 64 x 32 bit bootstrap ROM

  - Off-chip expansion to 2 x 2^{32} 32-bit words of data memory
  - Off-chip expansion to 2^{32} 32-bit words of program memory
- Miscellaneous features
  - Two expansion ports assignable to X data, Y data, or program memory spaces or a combination thereof, effectively doubling off-chip bus bandwidth.
  - Host interface circuitry on each port provides a flexible slave interface to Direct Memory Access (DMA) controllers and external processors for easy design of multimaster systems
  - Write strobe pins support interface to external SRAMs without additional logic
  - Two programmable timers / counters
  - Three external interrupt / mode control lines
  - One external reset line for hardware reset
  - OnCE 4-pin port for unobtrusive, processor speed-independent debugging
  - HCMOS design for operating frequencies from 40 MHz down to DC
  - 223-pin plastic Pin Grid Array (PGA) package or 240-pin Ceramic Quad Flat Pack (CQFP) package
  - 5.0 V power supply

PRODUCT DOCUMENTATION

The two manuals listed in **Table 1** are required for a complete description of the DSP96002 and are necessary to properly design with the device. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 Additional Documentation

Document Name	Description	Order Number
DSP96002 User's Manual	Detailed description of the DSP96002 core processor and peripherals	DSP96002UM / AD
DSP96002 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP96002 / D, Rev. 1

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