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PRODUCT BRIEF

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DSP56L811P/D Rev. 1

DSP56L811

16-BIT DIGITAL SIGNAL PROCESSOR

The DSP56L811 is a member of the DSP56800 core-based family of digital signal processors (DSPs). This general-purpose DSP combines processing power with configuration flexibility, making it an excellent choice for signal processing and control functions, all at a low cost. The central processing unit, the DSP56800 core, consists of three execution units operating in parallel, allowing up to six operations during each instruction cycle. The MPU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers. The DSP56L811 supports program execution from internal or external memories. Two data operands can be accessed per instruction cycle from the on-chip data RAM. The rich set of programmable peripherals and ports provides support for interfacing multiple external devices such as codecs, microprocessors, or other DSPs. The DSP56L811 also provides 16 to 32 GPIO lines, depending on which optional peripherals are selected (see Figure 1), and two external dedicated interrupt lines. Because of its configuration flexibility, compact program code, and low cost, the DSP56800 family is well-suited for cost-sensitive applications including digital wireless messaging, digital answering machines / feature phones, wireline and wireless modems, servo and AC motor control, and digital cameras.

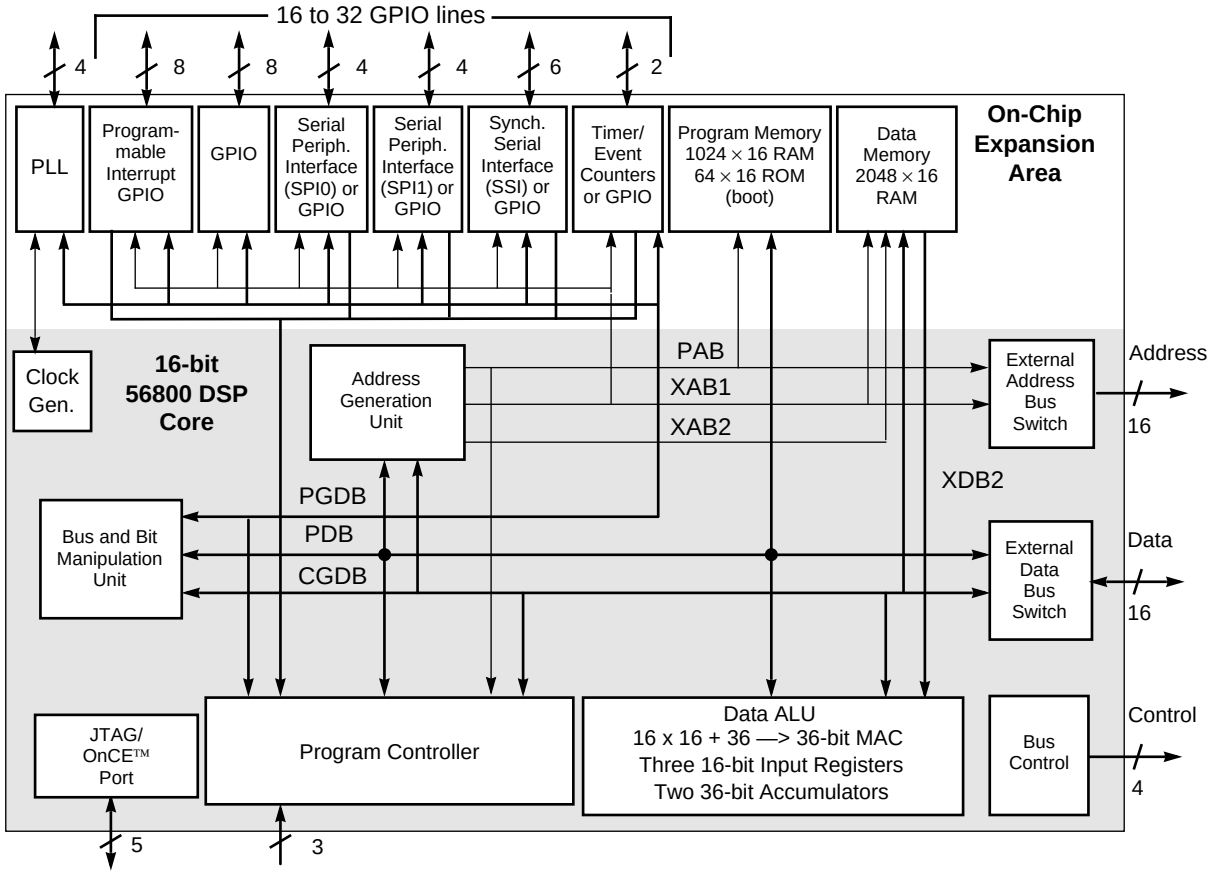

Figure 1 DSP56L811 Block Diagram

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DSP56L811 FEATURES

- Digital Signal Processing Core
  - Efficient 16-bit DSP56800-Family DSP engine
  - Up to 20 million instructions per second (MIPS) at 40 MHz
  - Single-cycle 16 x 16-bit parallel multiply-accumulator
  - Two 36-bit accumulators including extension bits
  - Parallel instruction set with unique DSP addressing modes
  - Hardware DO and REP loops
  - DO loops nestable in software
  - Address buses:
    - One 16-bit internal memory address bus (XAB1)
    - One 16-bit internal memory address bus (XAB2)
    - One 19-bit internal program address bus (PAB)
    - One 16-bit external address bus (EAB)
  - Data buses:
    - One 16-bit bidirectional internal memory data bus (CGDB)
    - One 16-bit unidirectional internal memory data bus (XDB2)
    - One 16-bit bidirectional dedicated peripheral data bus (PGDB)
    - One 16-bit bidirectional internal program data bus (PDB)
    - One 16-bit bidirectional external data bus (EDB)
  - Instruction set supports both DSP and controller functions
  - Controller style addressing modes and instructions for compact code
  - Efficient C compiler and local variable support
  - Software subroutine and interrupt stack with unlimited depth
- Memory
  - On-chip Harvard architecture permits up to three simultaneous accesses to program and data memory
  - 1K x 16 program RAM
  - 64 x16 bootstrap ROM
  - 2K x 16 X-data RAM
  - Programs can run out of X-data RAM

- Peripheral and Support Circuits
  - External memory interface (EMI)
  - Sixteen dedicated general purpose input/output (GPIO) pins (eight pins programmable as interrupts)
  - Serial peripheral interface (SPI) support: Two configurable 4-pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
    - Supports LCD drivers, A/D subsystems, and MCU systems
    - Supports inter-processor communications in a multiple master system
    - Demand-driven master or slave devices with high data rates
  - Synchronous serial interface (SSI) support: One 6-pin port (or six additional GPIO lines)
    - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola-SPI-compliant peripherals
    - Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
    - Network mode using frame sync and up to 32 time slots
    - 8-bit, 10-bit, 12-bit, and 16-bit data word lengths
  - Three programmable timers (accessed using two I/O pins that can also be programmed as two additional GPIO lines)
  - Two external interrupt/mode control lines
  - One external reset for hardware reset
  - JTAG/On-Chip Emulation (OnCE) 5-pin port for unobtrusive, processor speed-independent debugging
  - Software-programmable, phase-locked-loop-based (PLL) frequency synthesizer for the DSP core clock
  - Computer-operating properly (COP) and real-time interrupt (RTI) timers
- Energy Efficient Design
  - Power-saving wait and multiple stop modes available
  - Fully static, HCMOS design for operating frequencies from 40 MHz down to DC
  - 100-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package
  - 2.7 V-3.6 V power supply

PRODUCT DOCUMENTATION

The three manuals listed in Table 1 are required for a complete description of the DSP56L811 and are necessary to properly design with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 Additional Documentation

Document Name	Description	Order Number
DSP56800 Family Manual	Detailed description of the 56800-family architecture, and 16-bit DSP core processor and the instruction set	DSP56800 FAM/AD
DSP56L811 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56L811UM/AD
DSP56L811 Data Sheet	Electrical and timing specifications, and pin and package descriptions	DSP56L811/D

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