MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document by:
DSP56L811/D Rev. 2

DSP56L811

Advance Information
16-BIT DIGITAL SIGNAL PROCESSOR

The DSP56L811 is a member of the DSP56800 core-based family of Digital Signal Processors (DSPs). This general-purpose DSP combines processing power with configuration flexibility, making it an excellent choice for signal processing and control functions, all at a low cost. The Central Processing Unit, the DSP56800 core, consists of three execution units operating in parallel, allowing up to six operations during each instruction cycle. The MPU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers. The DSP56L811 supports program execution from internal or external memories. Two data operands can be accessed per instruction cycle from the on-chip data RAM. The rich set of programmable peripherals and ports provides support for interfacing multiple external devices, such as codecs, microprocessors, or other DSPs. The DSP56L811 also provides sixteen to thirty-two GPIO lines, depending on which optional peripherals are selected (see **Figure 1**), and two external dedicated interrupt lines. Because of its configuration flexibility, compact program code, and low cost, the DSP56800 family is well-suited for cost-sensitive applications including digital wireless messaging, digital answering machines/feature phones, wireline and wireless modems, servo and AC motor control, and digital cameras.

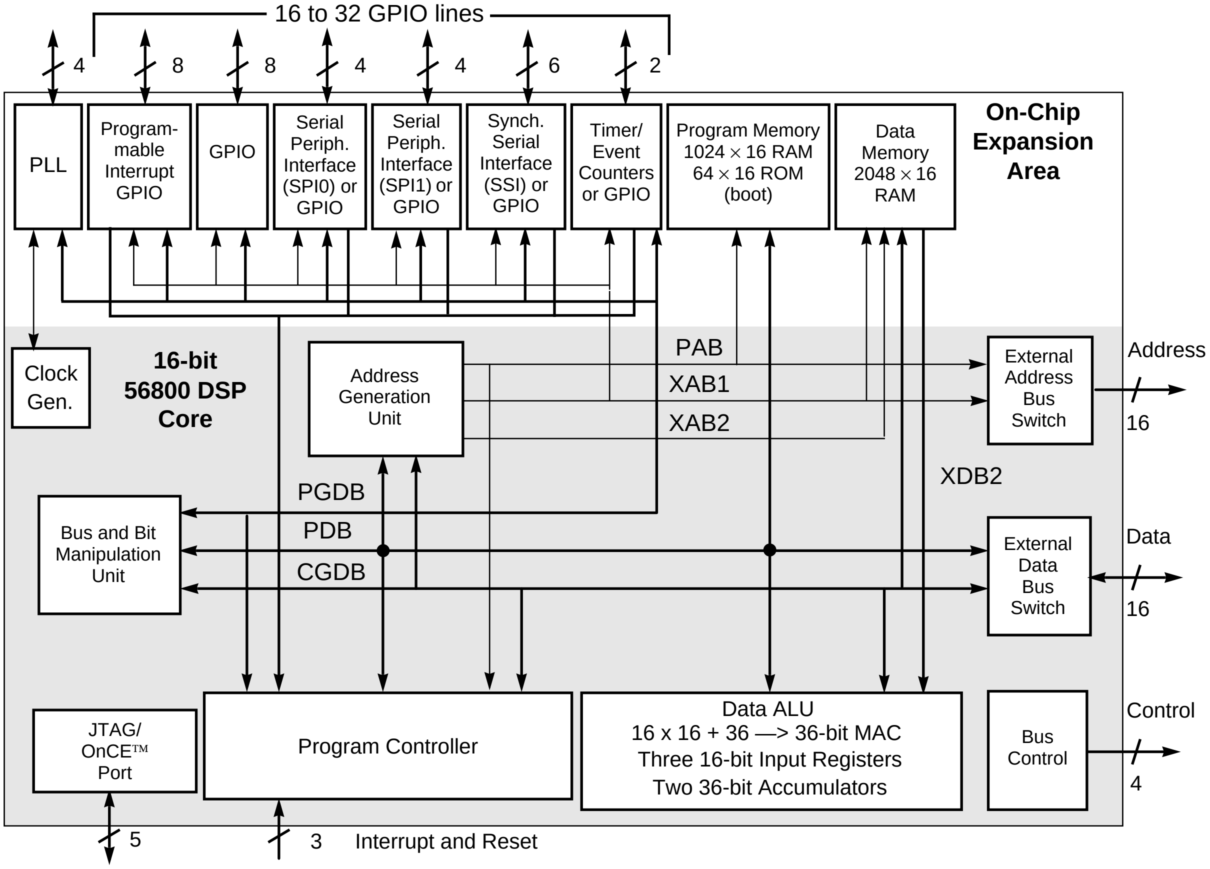


Figure 1 DSP56L811 Block Diagram

DSP56L811 FEATURES

- Digital Signal Processing Core
  - Efficient 16-bit DSP56800 family DSP engine
  - Up to 20 Million Instructions Per Second (MIPS) at 40 MHz
  - Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
  - Two 36-bit accumulators including extension bits
  - 16-bit bidirectional barrel shifter
  - Parallel instruction set with unique DSP addressing modes
  - Hardware DO and REP loops
  - DO loops nestable in software
  - Address buses:
    - Two 16-bit internal memory address bus (XAB1 and XAB2)
    - One 19-bit internal program address bus
    - One 16-bit external address bus
  - Data buses:
    - One 16-bit bidirectional internal memory data bus (CGDB)
    - One 16-bit unidirectional internal memory data bus (XDB2)
    - One 16-bit bidirectional dedicated peripheral data bus (PGDB)
    - One 16-bit bidirectional internal Program Data Bus (PDB)
    - One 16-bit bidirectional External Data Bus (EDB)
  - Instruction set supports both DSP and controller functions
  - Controller style addressing modes and instructions for compact code
  - Efficient C compiler and local variable support
  - Software subroutine and interrupt stack with unlimited depth
- Memory
  - On-chip Harvard architecture permits up to three simultaneous accesses to program and data memory
  - 1 K x 16 Program RAM
  - 64 x 16 bootstrap ROM
  - 2 K x 16 X data RAM
  - Programs can run out of X data RAM

- Peripheral and Support Circuits
  - External Memory Interface (EMI)
  - Sixteen dedicated General Purpose Input/Output (GPIO) pins (eight pins programmable as interrupts)
  - Serial Peripheral Interface (SPI) support: Two configurable 4-pin ports (SPI0 and SPI1) (or eight additional GPIO lines)
    - Supports LCD drivers, A/D subsystems, and MCU systems
    - Supports inter-processor communications in a multiple master system
    - Demand-driven master or slave devices with high data rates
  - Synchronous Serial Interface (SSI) support: One 6-pin port (or six additional GPIO lines)
    - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
    - Asynchronous or synchronous transmit and receive sections with separate or shared internal/external clocks and frame syncs
    - Network mode using frame sync and up to 32 time slots
    - 8-bit, 10-bit, 12-bit, and 16-bit data word lengths
  - Three programmable 16-bit timers (accessed using two I/O pins that can also be programmed as two additional GPIO lines)
  - Computer-Operating Properly (COP) and Real-Time Interrupt (RTI) timers
  - Two external interrupt/mode control pins
  - One external reset pin for hardware reset
  - JTAG/On-Chip Emulation (OnCE) 5-pin port for unobtrusive, processor speed-independent debugging
  - Software-programmable, Phase Lock Loop-based (PLL) frequency synthesizer for the DSP core clock
- Energy Efficient Design
  - Power-saving wait And multiple Stop modes available
  - Fully static, HCMOS design for 40 MHz to DC operating frequencies
  - 100-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package
  - 2.7–3.6 V power supply

PRODUCT DOCUMENTATION

The three manuals listed in **Table 1** are required for a complete description of the DSP56L811 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 DSP56L811 Documentation

Document Name	Description	Order Number
DSP56800 Family Manual	Detailed description of the 56800-family architecture, 16-bit core processor, and the instruction set	DSP56800FM/AD
DSP56L811 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56L811UM/AD
DSP56L811 Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56L811/D

FOR THE LATEST INFORMATION

Refer to the back cover of this document for:

- Motorola contact addresses
- Motorola Mfax™ service
- Motorola DSP Internet address

The Mfax service and the DSP internet connection maintain the most current specifications, documents, and drawings. These two services are available on demand 24 hours a day.

SECTION 1

PIN DESCRIPTIONS

INTRODUCTION

The DSP56L811 is available in a 100-pin Thin Quad Flat Pack (TQFP) package. The pins are organized into thirteen functional groups as summarized in **Table 1-1**.

Table 1-1 Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDPLL})	10	Table 1-2
Ground (V_{SS} or V_{SSPLL})	10	Table 1-3
PLL and Clock	4	Table 1-4
Address Bus	16	Table 1-5
Data Bus	16	Table 1-6
Bus Control	4	Table 1-7
Interrupt and Mode Control	3	Table 1-8
Programmable Interrupt General Purpose Input/Output	8	Table 1-9
Dedicated General Purpose Input/Output	8	Table 1-10
Serial Peripheral Interface (SPI) Ports[1]	8	Table 1-11
Synchronous Serial Interface (SSI) Port[1]	6	Table 1-12
Timer Module[1]	2	Table 1-13
JTAG/On-Chip Emulation (OnCE)	5	Table 1-14
Note: 1. Alternately, GPIO pins		

Figure 1-1 is a diagram of DSP56L811 pins by functional group.

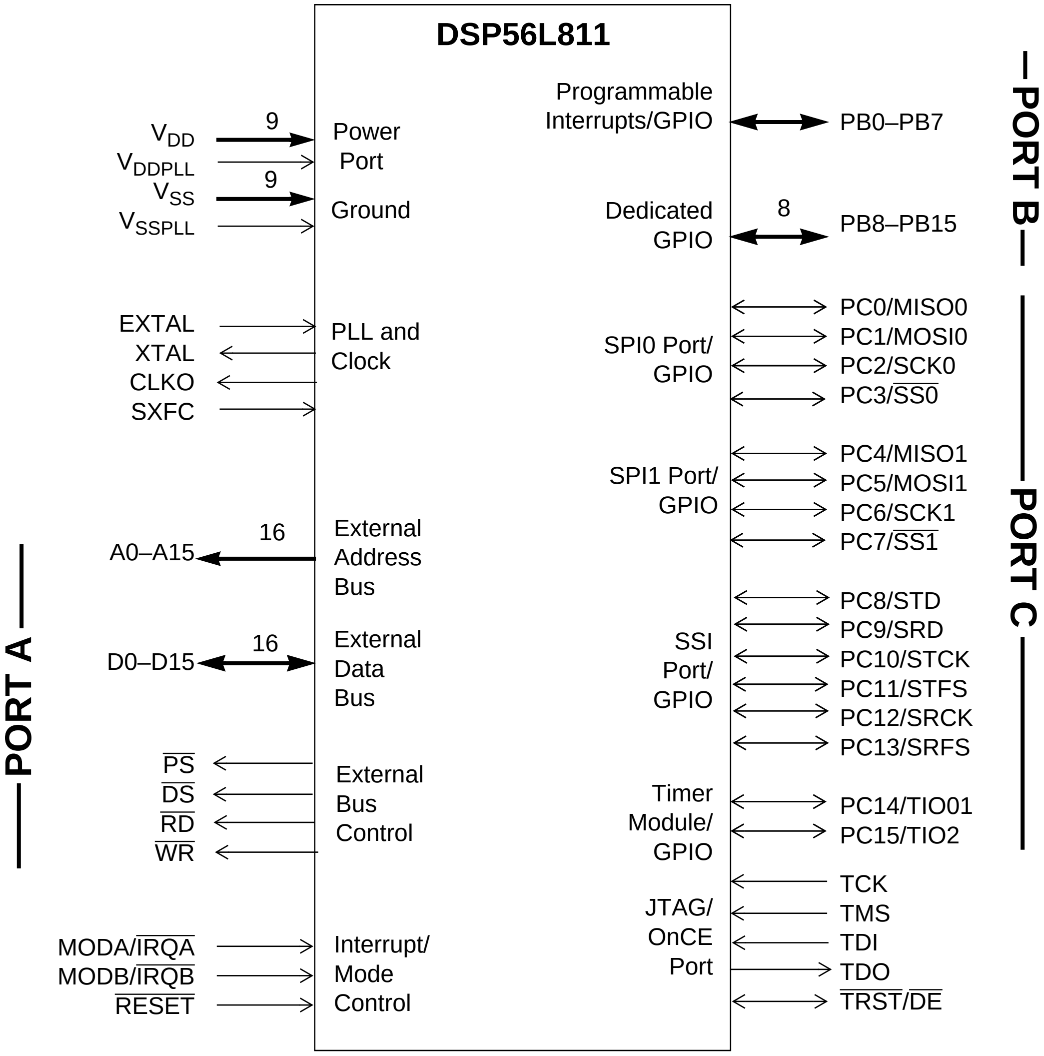


Figure 1-1 Functional Group Pin Allocations

POWER AND GROUND PINS

Table 1-2 Power Pins

Pin Name	Pin Description
V_{DD} (9)	**Power—**power pins
V_{DDPLL}	**PLL Power—**This pin supplies a quiet power source to the VCO to provide greater frequency stability.

Table 1-3 Ground Pins

Pin Name	Pin Description
V_{SS} (9)	**GND—**ground pins
V_{SSPLL}	**PLL Ground—**This pin supplies a quiet ground to the VCO to provide greater frequency stability.

PLL AND CLOCK PINS

Table 1-4 PLL and Clock Pins

Pin Name	Signal Type	State during Reset	Pin Description
EXTAL	Input	Input	**External Clock/Crystal Input—**This input should be connected to an external clock or to an external oscillator. After being squared, the input clock can be selected to provide the clock directly to the DSP core. The minimum instruction time is two input clock periods, broken up into four phases named T0, T1, T2, and T3. This input clock can also be selected as input clock for the on-chip PLL.
XTAL	Output	Chip-driven	**Crystal Output—**This output connects the internal crystal oscillator output to an external crystal. If an external clock is used, XTAL should not be connected.
CLKO	Output	Chip-driven	**Clock Output—**This pin outputs a buffered clock signal. By programming two bits (CS1, CS0) inside the PLL Control Register PCR1, the user can select between outputting a squared version of the signal applied to EXTAL and a version of the DSP master clock at the output of the PLL. The clock frequency on this pin can also be disabled by programming the CS1, CS0 bits in the PLL Control Register, PCR1.

Table 1-4 PLL and Clock Pins (Continued)

Pin Name	Signal Type	State during Reset	Pin Description
SXFC	Input	Input	**External Filter Capacitor**—This pin is used to add an external filter circuit to the Phase Lock Loop (PLL). Refer to **Figure 2-6**.

ADDRESS, DATA, AND BUS CONTROL PINS

Table 1-5 Address Bus Pins

Pin Names	Signal Type	State during Reset	Pin Description
A0–A15	Output	Tri-stated	**Address Bus**—A0–A15 change in T0, and specify the address for external program or data memory accesses.

Table 1-6 Data Bus Pins

Pin Names	Signal Type	State during Reset	Pin Description
D0–D15	Input/Output	Tri-stated	**Data Bus**—Read data is sampled in by the trailing edge of T2, while write data output is enabled by the leading edge of T2 and tri-stated by the leading edge of T0. If there is no external bus activity, D0–D15 are tri-stated.

Table 1-7 Bus Control Pins

Pin Name	Signal Type	State during Reset	Pin Description
$\overline{\text{PS}}$	Output	Tri-stated	**Program Memory Select**—$\overline{\text{PS}}$ is asserted low for external program memory access. If the external bus is not used during an instruction cycle (T0, T1, T2, T3), $\overline{\text{PS}}$ goes high in T0.
$\overline{\text{DS}}$	Output	Tri-stated	**Data Memory Select**—$\overline{\text{DS}}$ is asserted low for external data memory access. If the external bus is not used during an instruction cycle (T0, T1, T2, T3), $\overline{\text{DS}}$ goes high in T0.

Table 1-7 Bus Control Pins (Continued)

Pin Name	Signal Type	State during Reset	Pin Description
$\overline{\text{WR}}$	Output	Tri-stated	**Write Enable—**This output is asserted during external memory write cycles. When $\overline{\text{WR}}$ is asserted low in T1, the data bus pins D0–D15 become outputs and the DSP puts data on the bus during the leading edge of T2. When $\overline{\text{WR}}$ is deasserted high in T3, the external data is latched inside the external device. When $\overline{\text{WR}}$ is asserted, it qualifies the A0–A15, $\overline{\text{PS}}$ and $\overline{\text{DS}}$ pins. $\overline{\text{WR}}$ can be connected directly to the $\overline{\text{WE}}$ pin of a Static RAM.
$\overline{\text{RD}}$	Output	Tri-stated	**Read Enable—**This output is asserted during external memory read cycles. When $\overline{\text{RD}}$ is asserted low late T0/early T1, the data bus pins D0–D15 become inputs and an external device is enabled onto the DSP data bus. When $\overline{\text{RD}}$ is deasserted high in T3, the external data is latched inside the DSP. When $\overline{\text{RD}}$ is asserted, it qualifies the A0–A15 and $\overline{\text{PS}}$ and $\overline{\text{DS}}$ pins. $\overline{\text{RD}}$ can be connected directly to the $\overline{\text{OE}}$ pin of a Static RAM or ROM.

INTERRUPT AND MODE CONTROL PINS

Table 1-8 Interrupt and Mode Control Pins

Pin Name	Signal Type	State during Reset	Pin Description
MODA/ $\overline{\text{IRQA}}$	Input	Input	**Mode Select A/External Interrupt Request A—**This input has two functions: (1) to select the initial chip operating mode and (2), after synchronization, to allow an external device to request a DSP interrupt. MODA is read and internally latched in the DSP when the processor exits the Reset state. MODA and MODB select the initial chip operating mode. Several clock cycles (depending on PLL setup time) after leaving the Reset state, the MODA pin changes to external interrupt request $\overline{\text{IRQA}}$. The chip operating mode can be changed by software after reset. The $\overline{\text{IRQA}}$ input is a synchronized external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-sensitive. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation. If the processor is in the Stop state and $\overline{\text{IRQA}}$ is asserted, the processor will exit the Stop state.

Table 1-8 Interrupt and Mode Control Pins

Pin Name	Signal Type	State during Reset	Pin Description
MODB/ $\overline{\text{IRQB}}$	Input	Input	**Mode Select B/External Interrupt Request B—**This input has two functions: (1) to select the initial chip operating mode and (2), after internal synchronization, to allow an external device to request a DSP interrupt. MODB is read and internally latched in the DSP when the processor exits the Reset state. MODA and MODB select the initial chip operating mode. Several clock cycles (depending on PLL setup time) after leaving the Reset state, the MODB pin changes to external interrupt request $\overline{\text{IRQB}}$. After reset, the chip operating mode can be changed by software. The $\overline{\text{IRQB}}$ input is an external interrupt request that indicates that an external device is requesting service. It may be programmed to be level-sensitive or negative-edge-triggered. If level-sensitive triggering is selected, an external pull up resistor is required for wired-OR operation.
$\overline{\text{RESET}}$	Input	Input	**Reset—**This input is a direct hardware reset on the processor. When $\overline{\text{RESET}}$ is asserted low, the DSP is initialized and placed in the Reset state. A Schmitt trigger input is used for noise immunity. When the $\overline{\text{RESET}}$ pin is deasserted, the initial chip operating mode is latched from the MODA and MODB pins. The internal reset signal should be deasserted synchronous with the internal clocks. To ensure complete hardware reset, $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$/$\overline{\text{DE}}$ should be asserted together. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$/$\overline{\text{DE}}$.

GPIO PINS

Table 1-9 Programmable Interrupt GPIO Pins

Pin Name	Signal Type	State during Reset	Pin Description
PB0–PB7	Input or Output	Input	**Port B GPIO—**These eight pins can be programmed to generate an interrupt for any pin programmed as an input when there is a transition on that pin. Each pin can individually be configured to recognize a low-to-high or a high-to-low transition. In addition, these pins are dedicated General Purpose I/O (GPIO) pins that can individually be programmed as input or output pins. After reset, the default state is GPIO input.

Table 1-10 Dedicated General Purpose Input/Output (GPIO) Pins

Pin Name	Signal Type	State during Reset	Pin Description
PB8–PB14	Input or Output	Input	**Port B GPIO—**These seven pins are dedicated General Purpose I/O (GPIO) pins that can individually be programmed as input or output pins. After reset, the default state is GPIO input
PB15/ $\overline{\text{XCOLF}}$	Input or Output	Input, pulled high internally	**Port B GPIO—**This pin is a dedicated GPIO pin that can individually be programmed as an input or output pin. During reset, the External Crystal Oscillator Low Frequency ($\overline{\text{XCOLF}}$) function of this pin is active. PB15/$\overline{\text{XCOLF}}$ is tied to an on-chip pull-up transistor that is active during reset. When $\overline{\text{XCOLF}}$ is driven low during reset (or tied to a 10 kΩ pull-down resistor), the crystal oscillator amplifier is set to a low frequency mode. In this low-frequency mode, only oscillator frequencies of 32 kHz and 38.4 kHz are supported. If $\overline{\text{XCOLF}}$ is not driven low during reset (or if a pull-down resistor is not used), the crystal oscillator amplifier operates in the Default mode, and oscillator frequencies from 2 MHz to 10 MHz are supported. If an external clock is provided to the EXTAL pin, 40 MHz is the maximum frequency allowed. (In this case, do not connect a pull-down resistor or drive this pin low during reset.) After reset, the default state is GPIO input.

SERIAL PERIPHERAL INTERFACE PINS

Table 1-11 Serial Peripheral Interface (SPI0 and SPI1) Pins

Pin Name	Signal Type	State during Reset	Pin Description
PC0/MISO0	Input/ Output	Input	**SPI0 Master In/Slave Out (MISO0)—**This serial data pin is an input to a master device and an output from a slave device. The MISO0 line of a slave device is placed in the high-impedance state if the slave device is not selected. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device. **Port C GPIO 0 (PC0)—**This pin is a GPIO pin called PC0 when the SPI MISO0 function is not being used. After reset, the default state is GPIO input.
PC1/MOSI0	Input/ Output	Input	**SPI0 Master Out/Slave In (MOSI0)—**This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI0 line a half-cycle before the clock edge that the slave device uses to latch the data. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device. **Port C GPIO 1 (PC1)—**This pin is a GPIO pin called PC1 when the SPI MOSI0 function is not being used. After reset, the default state is GPIO input.
PC2/SCK0	Input/ Output	Input	**SPI0 Serial Clock—**This bidirectional pin provides a serial bit rate clock for the SPI. This gated clock signal is an input to a slave device and is generated as an output by a master device. Slave devices ignore the SCK signal unless the slave select pin is active low. In both master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device. **Port C GPIO 2 (PC2)—**This pin is a GPIO pin called PC2 when the SPI SCK0 function is not being used. After reset, the default state is GPIO input.

Table 1-11 Serial Peripheral Interface (SPI0 and SPI1) Pins (Continued)

Pin Name	Signal Type	State during Reset	Pin Description
PC3/$\overline{SS0}$	Input or Input/ Output	Input	**SPI0 Slave Select—**This input pin is used to select a slave device before a master device can exchange data with the slave device. $\overline{SS}$ must be low before data transactions and must stay low for the duration of the transaction. The $\overline{SS}$ line of the master must be held high. **Port C GPIO 3 (PC3)—**This pin is a GPIO pin called PC3 when the SPI $\overline{SS0}$ function is not being used. After reset, the default state is GPIO input.
PC4/MISO1	Input/ Output	Input	**SPI1 Master In/Slave Out—**This serial data pin is an input to a master device and an output from a slave device. The MISO1 line of a slave device is placed in the high-impedance state if the slave device is not selected. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device. **Port C GPIO 4 (PC4)—**This pin is a GPIO pin called PC4 when the SPI MISO1 function is not being used. After reset, the default state is GPIO input.
PC5/MOSI1	Input/ Output	Input	**SPI1 Master Out/Slave In (MOSI1)—**This serial data pin is an output from a master device and an input to a slave device. The master device places data on the MOSI0 line a half-cycle before the clock edge that the slave device uses to latch the data. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device. **Port C GPIO5 (PC5)—**This pin is a GPIO pin called PC5 when the SPI MOSI1 function is not being used. After reset, the default state is GPIO input.

Table 1-11 Serial Peripheral Interface (SPI0 and SPI1) Pins (Continued)

Pin Name	Signal Type	State during Reset	Pin Description
PC6/SCK1	Input/ Output	Input	**SPI1 Serial Clock—**This bidirectional pin provides a serial bit rate clock for the SPI. This gated clock signal is an input to a slave device and is generated as an output by a master device. Slave devices ignore the SCK signal unless the slave select pin is active low. In both master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. The driver on this pin can be configured as an open-drain driver by the SPI's WOM bit when this pin is configured for SPI operation. When using Wired-OR mode, the user must provide an external pull-up device. **Port C GPIO 6 (PC6)—**This pin is a GPIO pin called PC6 when the SPI SCK1 function is not being used. After reset, the default state is GPIO input.
PC7/$\overline{\text{SS1}}$	Input or Input/ Output	Input	**SPI1 Slave Select—**This input pin is used to select a slave device before a master device can exchange data with the slave device. $\overline{\text{SS}}$ must be low before data transactions and must stay low for the duration of the transaction. The $\overline{\text{SS}}$ line of the master must be held high. **Port C GPIO 7 (PC7)—**This pin is a GPIO pin called PC7 when the SPI $\overline{\text{SS1}}$ function is not being used. After reset, the default state is GPIO input.

SYNCHRONOUS SERIAL INTERFACE PINS

Table 1-12 Synchronous Serial Interface (SSI) Pins

Pin Name	Signal Type	State during Reset	Pin Description
PC8/STD	Output or Input/ Output	Input	**SSI Transmit Data (STD)—**This output pin transmits serial data from the SSI Transmitter Shift Register. **Port C GPIO 8 (PC8)—**This pin is a GPIO pin called PC8 when the SSI STD function is not being used. After reset, the default state is GPIO input.

Table 1-12 Synchronous Serial Interface (SSI) Pins (Continued)

Pin Name	Signal Type	State during Reset	Pin Description
PC9/SRD	Input or Input/ Output	Input	**SSI Receive Data—**This input pin receives serial data and transfers the data to the SSI Receive Shift Register. **Port C GPIO 9 (PC9)—**This pin is a GPIO pin called PC9 when the SSI SRD function is not being used. After reset, the default state is GPIO input.
PC10/STCK	Input/ Output	Input	**SSI Serial Transmit Clock—**This bidirectional pin provides the serial bit rate clock for the Transmit section of the SSI. The clock signal can be continuous or gated and can be used by both the transmitter and receiver in Synchronous mode. **Port C GPIO 10 (PC10)—**This pin is a GPIO pin called PC10 when the SSI STCK function is not being used. After reset, the default state is GPIO input.
PC11/STFS	Input/ Output	Input	**Serial Transmit Frame Sync—**This bidirectional pin is used by the Transmit section of the SSI as frame sync I/O or flag I/O. The STFS can be used by both the transmitter and receiver in Synchronous mode. It is used to synchronize data transfer and can be an input or an output. **Port C GPIO 11 (PC11)—**This pin is a GPIO pin called PC11 when the SSI STFS function is not being used. This pin is not required by the SSI in Gated Clock mode. After reset, the default state is input.
PC12/SRCK	Input/ Output	Input	**SSI Serial Receive Clock—**This bidirectional pin provides the serial bit rate clock for the Receive section of the SSI. The clock signal can be continuous or gated and can be used only by the receiver. **Port C GPIO 12 (PC12)—**This pin is a GPIO pin called PC12 when the SSI STD function is not being used. After reset, the default state is GPIO input.

Table 1-12 Synchronous Serial Interface (SSI) Pins (Continued)

Pin Name	Signal Type	State during Reset	Pin Description
PC13/SRFS	Input/ Output	Input	**Serial Receive Frame Sync (SRFS)—**This bidirectional pin is used by the Receive section of the SSI as frame sync I/O or flag I/O. The STFS can be used only by the receiver. It is used to synchronize data transfer and can be an input or an output. **Port C GPIO 13 (PC13)—**This pin is a GPIO pin called PC13 when the SSI SRFS function is not being used. After reset, the default state is GPIO input.

TIMER MODULE PINS

Table 1-13 Timer Module Pins

Pin Name	Signal Type	State during Reset	Pin Description
PC14/TIO01	Input/ Output	Input	**Timer 0 and Timer 1 Input/Output (TIO01)—**This bidirectional pin receives external pulses to be counted by either the on-chip 16-bit Timer 0 or Timer 1 when configured as input and external clocking is selected. The pulses are internally synchronized to the DSP core internal clock. When configured as output, it generates pulses or toggles on a Timer 0 or Timer 1 overflow event. Selection of Timer 0 or Timer 1 is programmable through an internal register. **Port C GPIO 14 (PC14)—**This pin is a GPIO pin called PC14 when the Timer TIO01 function is not being used. After reset, the default state is GPIO input.
PC15/TIO2	Input/ Output	Input	**Timer 2 Input/Output (TIO2)—**This bidirectional pin receives external pulses to be counted by the on-chip 16-bit Timer 2 when configured as input and external clocking is selected. The pulses are internally synchronized to the DSP core internal clock. When configured as output, it generates pulses or toggles on a Timer 2 overflow event. **Port C GPIO 15 (PC15)—**This pin is a GPIO pin called PC15 when the Timer TIO2 function is not being used. After reset, the default state is GPIO input.

JTAG/ONCE PINS

Table 1-14 JTAG/On-Chip Emulation (OnCE) Pins

Pin Name	Signal Type	State during Reset	Pin Description
TCK	Input	Input, pulled low internally	**Test Clock Input—**This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
TMS	Input	Input, pulled high internally	**Test Mode Select Input—**This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDI	Input	Input, pulled high internally	**Test Data Input—**This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output—**This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
$\overline{\text{TRST}}$/$\overline{\text{DE}}$	Input or Output	Input, pulled high internally	**Test Reset/Debug Event—**As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. It can also be programmed within the OnCE port as an output to provide a low pulse on recognized debug events; when configured as an output signal, the $\overline{\text{TRST}}$ input is disabled.This pin is connected internally to a pull-up resistor. To ensure complete hardware reset, $\overline{\text{TRST}}$/$\overline{\text{DE}}$ should be asserted whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware DSP reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$/$\overline{\text{DE}}$.

SECTION 2

SPECIFICATIONS

GENERAL CHARACTERISTICS

The DSP56L811 is fabricated in high density HCMOS with TTL compatible inputs and CMOS compatible outputs.

Table 2-1 Absolute Maximum Ratings (GND = 0 V)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to 4.0	V
All Other Input Voltages	V_{IN}	(GND – 0.3) to (V_{DD} + 0.3)	V
Current Drain per Pin excluding V_{DD} and GND	I	10	mA
Storage Temperature Range	T_{STG}	–55 to 150	˚C

Note: This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Table 2-2 Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	2.7 to 3.6	V
Ambient Temperature	T_A	–40 to 85	˚C

Table 2-3 Package Thermal Characteristics

Thermal Resistance	100-pin TQFP		
	Symbol	Value	Units
Junction-to-ambient (estimated)	$R_{\theta JA}$	65	°C/W
Junction-to-case (estimated)	$R_{\theta JC}$	10	°C/W

Notes:
1. See discussion under **Design Considerations, Heat Dissipation**, page 4-1.
2. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided Printed Circuit Board per SEMI G38-87 in natural convection. SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Road, Mountain View, CA 94043, (415) 964-5111.
3. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88 with the exception that the cold plate temperature is used for the case temperature.

DC ELECTRICAL CHARACTERISTICS

Table 2-4 DC Electrical Characteristics

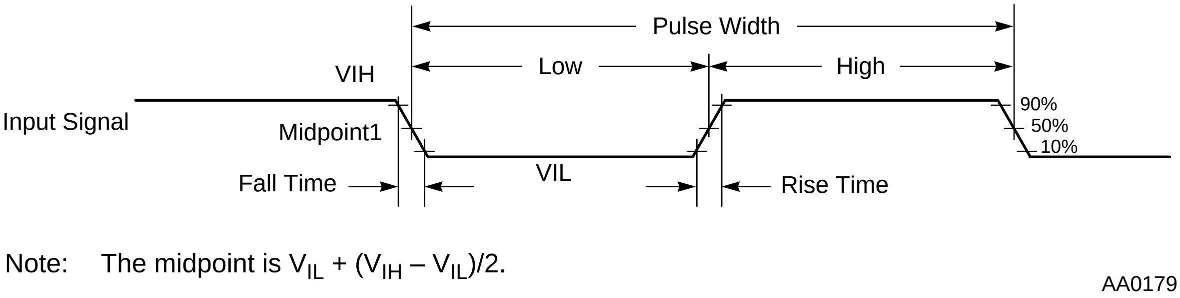
Characteristics	Symbol	Min	Typical	Max	Units
Supply Voltage	V_{DD}	2.7	—	3.6	V
Input High Voltage:					V
EXTAL	V_{IHC}	$0.8 \times V_{DD}$	—	V_{DD}	
all other inputs	V_{IH}	2.0	—		
Input Low Voltage					V
EXTAL	V_{ILC}	–0.3	—	$0.2 \times V_{DD}$	
all other inputs	V_{IL}	–0.3	—	0.8	
Input Leakage Current @ 2.4 V/0.4 V with $V_{DD} = 3.6$ V	I_{IN}	–1	—	1	µA
Input/Output Tri-state (off-state) Leakage Current @ 2.4 V/0.4 V with $V_{DD} = 3.6$ V	I_{TSI}	–10	—	+10	µA
Output High Voltage	V_{OH}				V
$I_{OH} = -0.3$ mA		$V_{DD} - 0.7$	—	—	
$I_{OH} = -50$ µA		$V_{DD} - 0.3$	—	—	
Output Low Voltage	V_{OL}				V
$I_{OL} = 2$ mA		—	—	0.4	
$I_{OL} = 50$ µA)		—	—	0.2	
Core CPU Supply Current[1] ($F_{PLL} = 40$ MHz)	I_{CORE}	—	20	30	mA
Stop Mode Current[1, 2]	I_{STOP}	—	2	5	µA
Input Capacitance (estimated)	C_{IN}	—	10	—	pF

Notes:
1. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float) using CMOS levels.
2. At 25°C, $V_{DD} = 3.0$ V, $V_{IH} = V_{DD}$, $V_{IL} = 0$ V.

AC ELECTRICAL CHARACTERISTICS

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

The timing waveforms in the **AC Electrical Characteristics** are tested with a V_{IL} maximum of 0.8 V and a V_{IH} minimum of 2.0 V for all pins except EXTAL, which is tested using the input levels described in **DC Electrical Characteristics**. AC timing specifications that are referenced to a device input signal are measured in production with respect to the 50% point (midpoint) of the respective input signal transitions, as show in **Figure 2-1**.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 2-1 Signal Measurement Reference

External Clock Operation

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

The DSP56L811 system clock may be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins. The internal oscillator is designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 2-6**. The circuits in **Figure 2-3** shows typical crystal oscillator circuits. Follow the crystal supplier’s recommendations when selecting a crystal, since the crystal parameters determine the component values required to provide maximum stability and reliable start-up. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time.

When using the on-chip oscillator in conjunction with an external crystal to generate the DSP clock, the following specifications apply.

Table 2-5 EXTAL/XTAL Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units
EXTAL Peak-to-Peak Swing (for any value of $\overline{\text{XCOLF}}$) V_{DDPLL} = 2.7 V V_{DDPLL} = 3.0 V V_{DDPLL} = 3.6 V	 — — —	 1.27 1.38 1.58	 — — —	 1.9 2.1 2.75	 V p-p V p-p V p-p
XTAL Transconductance $\overline{\text{XCOLF}}$ = 0 $\overline{\text{XCOLF}}$ = V_{DD}	g_m	 0.206 2.06	 0.465 4.65	 1.02 10.2	mA/V
XTAL Output Resistance $\overline{\text{XCOLF}}$ = 0 $\overline{\text{XCOLF}}$ = V_{DD}	r_o	 28.3 2.83	 80.6 8.06	 209.4 20.94	kΩ

Note: When driving the clock directly into EXTAL (not using a crystal), the input clock should follow normal digital DSP56L811 requirements.

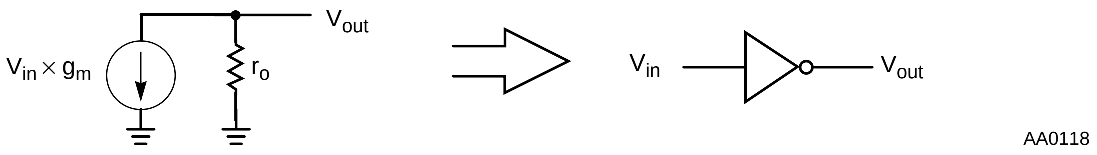
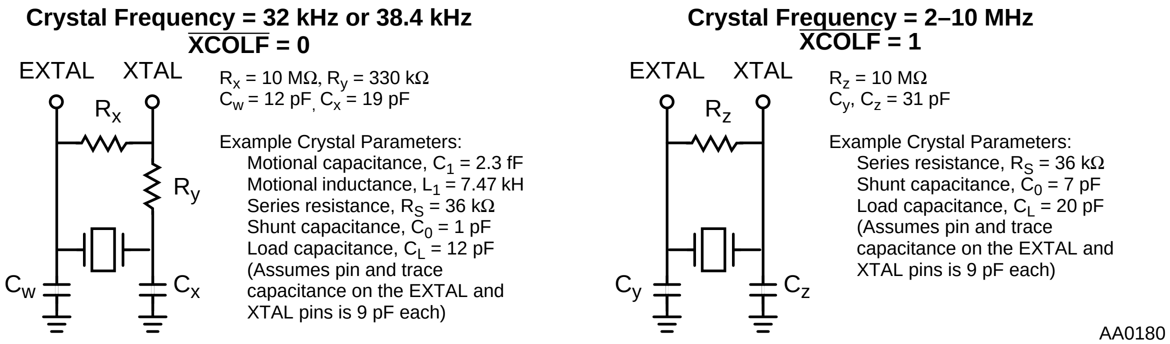


Figure 2-2 XTAL Transconductance Model



R_x = 10 MΩ, R_y = 330 kΩ
C_w = 12 pF, C_x = 19 pF

Example Crystal Parameters:
Motional capacitance, C_1 = 2.3 fF
Motional inductance, L_1 = 7.47 kH
Series resistance, R_S = 36 kΩ
Shunt capacitance, C_0 = 1 pF
Load capacitance, C_L = 12 pF
(Assumes pin and trace capacitance on the EXTAL and XTAL pins is 9 pF each)

R_z = 10 MΩ
C_y, C_z = 31 pF

Example Crystal Parameters:
Series resistance, R_S = 36 kΩ
Shunt capacitance, C_0 = 7 pF
Load capacitance, C_L = 20 pF
(Assumes pin and trace capacitance on the EXTAL and XTAL pins is 9 pF each)

Figure 2-3 Examples of Crystal Oscillator Circuits

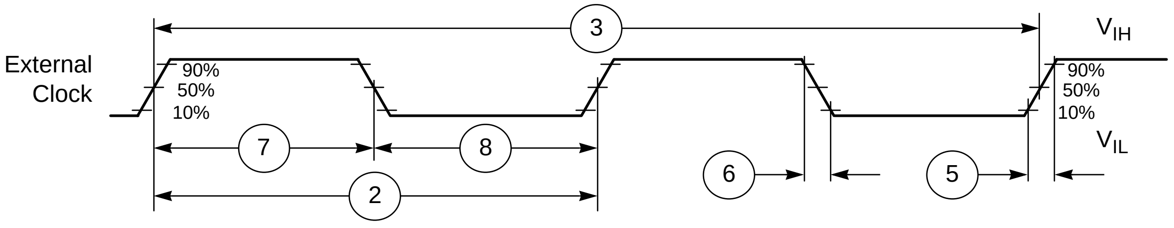
If the design uses an external clock circuit, apply the external clock input to the EXTAL input with the XTAL pin left unconnected, as shown in **Figure 2-4**.

Figure 2-4 Connecting an External Clock Signal

Table 2-6 Clock Operation Timing

No.	**Characteristics**	**40 MHz**		**Unit**
		Min	**Max**	
1	Frequency of Operation (External Clock)	0	40	MHz
2	Clock Cycle Time	25	—	ns
3	Instruction Cycle Time	50	—	ns
4	External Reference Frequency • Crystal option $\overline{\text{XCOLF}}$ = 0[1] $\overline{\text{XCOLF}}$ = 1 • External Clock option $\overline{\text{XCOLF}}$ = 0 $\overline{\text{XCOLF}}$ = 1	 32 2 0 2	 38.4 10 2 40	 kHz MHz MHz MHz
5	External Clock Input Rise Time	—	3	ns
6	External Clock Input Fall Time	—	3	ns
7	External Clock Input High Time	11.25	—	ns
8	External Clock Input Low Time	11.25	—	ns
9	PLL Output Frequency	10	40	MHz
10	PLL stabilization time after crystal oscillator start-up time[2]	—	10	ms

Notes: 1. When the crystal option is used and $\overline{\text{XCOLF}}$ = 0, only frequencies of 32 and 38.4 kHz are supported.
2. This is the minimum time required after the PLL setup is changed to ensure reliable operation.



Note: 1. The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 2-5 External Clock Timing

External Components for the PLL

The on-chip PLL requires an extra circuit connected to the SXFC pin, as shown in **Figure 2-6**. As indicated in **Table 2-7**, the values of R, C_1, and C should be chosen based on the Multiplication Factor used to derive the desired operating frequency from the input frequency selected. This circuit affects the performance of the PLL.

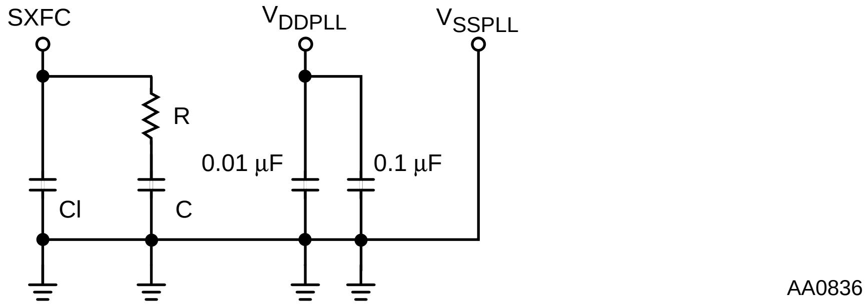


Figure 2-6 Schematic of Required External Components for the PLL

Table 2-7 Recommended Component Values for PLL Multiplication Factors

Multiplication Factor	C_l	R	C
1024	10 nF	15 kΩ	15 nF
512	2.7 nF	15 kΩ	15 nF
256	2.7 nF	15 kΩ	15 nF
128	2.7 nF	15 kΩ	15 nF
100	2.7 nF	15 kΩ	15 nF
80	2.7 nF	15 kΩ	15 nF
40	2.7 nF	15 kΩ	15 nF
10	750 pF	2 kΩ	10 nF
4	750 pF	2 kΩ	10 nF
2	750 pF	2 kΩ	10 nF
Note: 1. Because of the high number of Multiplication Factors available, these are the only Multiplication Factors evaluated.			

Port A External Bus Synchronous Timing

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

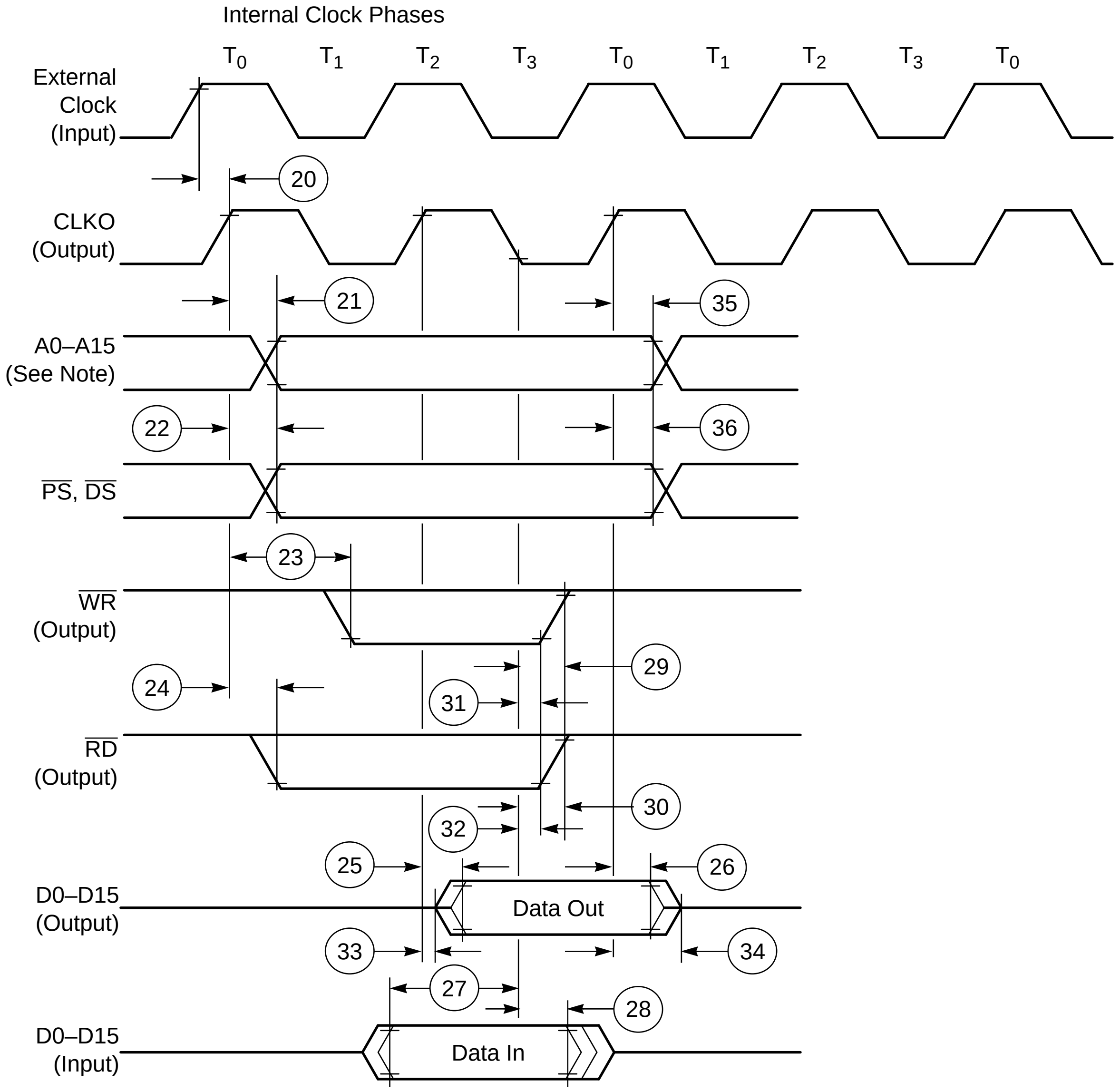
Capacitance Derating

The DSP56L811 external bus synchronous timing specifications are designed and tested at the maximum capacitive load of 50 pF, including stray capacitance. Typically, the drive capability of the pins A0–A15, D0–D15, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, and $\overline{WR}$ derates linearly at 1.7 ns per 20 pF of additional capacitance from 50 pF to 250 pF of loading. When an internal memory access follows an external memory access, the $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, and $\overline{WR}$ strobes remain deasserted and A0–A15 do not change from their previous state.

Note: In **Figure 2-7** and **Figure 2-8**, T_0, T_1, T_2, and T_3 refer to the internal clock phases and T_W refers to wait state.

Table 2-8 External Bus Synchronous Timing

No.	Characteristic	40 MHz		Unit
		Min	Max	
20	External Input Clock High to CLKO High	4	16.6	ns
21	CLKO High to A0–A15 Valid	5.2	12.4	ns
22	CLKO High to $\overline{PS}$, $\overline{DS}$, Asserted	5.6	12.8	ns
23	CLKO High to $\overline{WR}$ Asserted Low	18.5	25.5	ns
24	CLKO High to $\overline{RD}$ Asserted Low	5.6	12.8	ns
25	CLKO High to D0–D15 Out Valid	5.2	15.5	ns
26	CLKO High to D0–D15 Out Invalid	4.2	7.9	ns
27	D0–D15 In Valid to CLKO Low (Setup)	6	—	ns
28	CLKO Low to D0–D15 In Invalid (Hold)	3	—	ns
29	CLKO Low to $\overline{WR}$ Deasserted	2.1	—	ns
30	CLKO Low to $\overline{RD}$ Deasserted	2.1	—	ns
31	$\overline{WR}$ Hold Time from CLKO Low	–2	—	ns
32	$\overline{RD}$ Hold Time from CLKO Low	–2	—	ns
33	CLKO High to D0–D15 Out Active	3	7	ns
34	CLKO High to D0–D15 Out Tri-state	—	15	ns
35	CLKO High to A0–A15 Invalid	2.5	3.5	ns
36	CLKO High to $\overline{PS}$, $\overline{DS}$ Invalid	2.5	3.5	ns



Note: 1. During Read-Modify-Write instructions and internal instructions, the address lines do not change state.

AA0183

Figure 2-7 Synchronous Timing—No Wait State

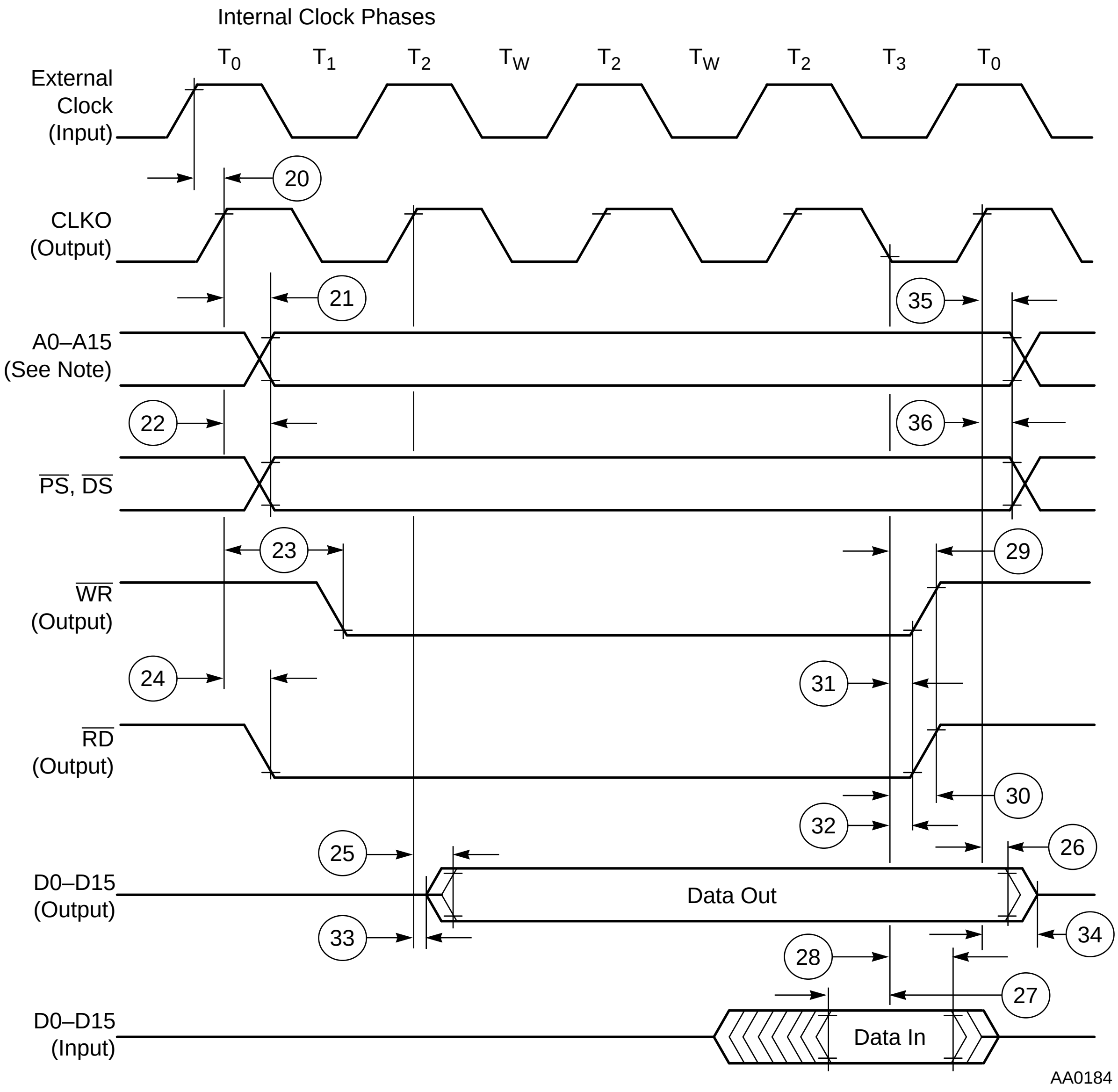


Figure 2-8 Synchronous Timing—Two Wait States

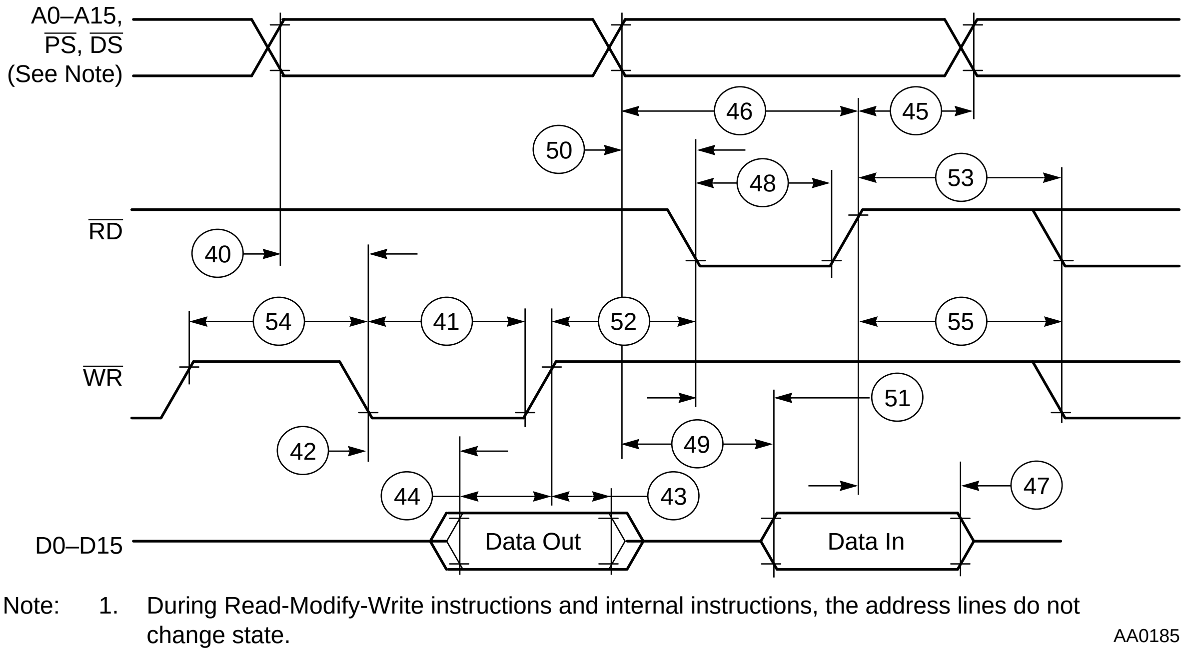
Port A External Bus Asynchronous Timing

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

Table 2-9 External Bus Asynchronous Timing

No.	Characteristic	40 MHz		Unit
		Min[1]	Max[1]	
40	Address Valid to $\overline{\text{WR}}$ Asserted	T – 2	—	ns
41	$\overline{\text{WR}}$ Width Asserted wait states = 0 wait states > 0	 2T – 4 2T(WS + 1) – 4	—	 ns ns
42	$\overline{\text{WR}}$ Asserted to D0–D15 Out Valid	—	T + 2	ns
43	Data Out Hold Time from $\overline{\text{WR}}$ Deasserted	T – 5	—	ns
44	Data Out Set Up Time to $\overline{\text{WR}}$ Deasserted wait states = 0 wait states > 0	 T + 2 T(2WS + 1) + 2	—	 ns ns
45	$\overline{\text{RD}}$ Deasserted to Address Not Valid	T – 4	—	ns
46	Address Valid to $\overline{\text{RD}}$ Deasserted	3T	—	ns
47	Input Data Hold to $\overline{\text{RD}}$ Deasserted	0.0	—	ns
48	$\overline{\text{RD}}$ Assertion Width wait states = 0 wait states > 0	 3T + 3.4 2T(WS) + 3T + 3.4		 ns ns
49	Address Valid to Input Data Valid wait states = 0 wait states > 0	 — —	 3T – 3 2T(WS) + 3T– 3	 ns ns
50	Address Valid to $\overline{\text{RD}}$ Asserted	0.0		ns
51	$\overline{\text{RD}}$ Asserted to Input Data Valid wait states = 0 wait states > 0	 — —	 T + 5 2T(WS) + T + 5	 ns ns
52	$\overline{\text{WR}}$ Deasserted to $\overline{\text{RD}}$ Asserted	T – 2	—	ns
53	$\overline{\text{RD}}$ Deasserted to $\overline{\text{RD}}$ Asserted	T + 1	—	ns
54	$\overline{\text{WR}}$ Deasserted to $\overline{\text{WR}}$ Asserted	2T – 4	—	ns
55	$\overline{\text{RD}}$ Deasserted to $\overline{\text{WR}}$ Asserted	2T – 1	—	ns

Note: 1. Timing is both wait state and frequency dependent. In the formulas listed, WS = the number of wait states and T = 1/2 the clock cycle. For 40 MHz operation, T = 12.5 ns.



Note: 1. During Read-Modify-Write instructions and internal instructions, the address lines do not change state.

Figure 2-9 External Bus Asynchronous Timing

Reset, Stop, Wait, Mode Select, and Interrupt Timing

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

Table 2-10 Reset, Stop, Wait, Mode Select, and Interrupt Timing

No.	Characteristics	40 MHz		Unit
		Min[1]	Max[1]	
60	$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	—	30	ns
61	Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	 600KT 60T	 — —	 ns ns
62	Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output [3]	65T	67T + 20	ns
63	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to CLKO Low	7.5	T + 7.5	ns
64	Synchronous Reset Delay Time from CLKO High to the First External Access[3]	66T + 5	66T + 13	ns
65	Mode and $\overline{\text{XCOLF}}$ Select Setup Time	5	—	ns
66	Mode and $\overline{\text{XCOLF}}$ Select Hold Time	6	—	ns
67	Edge-sensitive Interrupt Request Width	15	—	ns
68	$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	27T +6	—	ns
69	$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	31T + 27	—	ns
70	Synchronous setup time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ assertion to Synchronous CLKO High[4,5]	14	2T – 3	ns
71	CLKO Low to First Interrupt Vector Address Out Valid after Synchronous recovery from Wait State[6]	23T + 5	—	ns
72	$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[7]	15	—	ns
73	Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) [2] OMR Bit 6 = 0 OMR Bit 6 = 1	 524337T 47T	 — —	 ns ns

Table 2-10 Reset, Stop, Wait, Mode Select, and Interrupt Timing (Continued)

No.	Characteristics	40 MHz		Unit
		Min[1]	Max[1]	
74	Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop)[2]			
	OMR Bit 6 = 0	524337T	—	ns
	OMR Bit 6 = 1	47T	—	ns
75	Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop)[2]			
	OMR Bit 6 = 0			
	OMR Bit 6 = 1	524341T + 6	—	ns
		47T + 6	—	ns

Notes:
1. In the formulas, T = the internal clock width (1/4 instruction cycle) and WS = the number of wait states.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   - after power-on reset. and
   - when recovering from Stop mode.
3. The instruction fetch is visible on the pins only in Mode 2 and Mode 3.
4. Timing No. 72 is for all IRQx interrupts, while timing No. 73 is only when exiting the Wait state.
5. Timing No. 72 triggers off T0 in the Normal state and off phi0 when exiting the Wait state.
6. The minimum is specified for the duration of an edge-sensitive $\overline{\text{IRQA}}$ interrupt required to recover from the Stop state. This is not the minimum required so that the $\overline{\text{IRQA}}$ interrupt is accepted.
7. The interrupt instruction fetch is visible on the pins only in Mode 3.

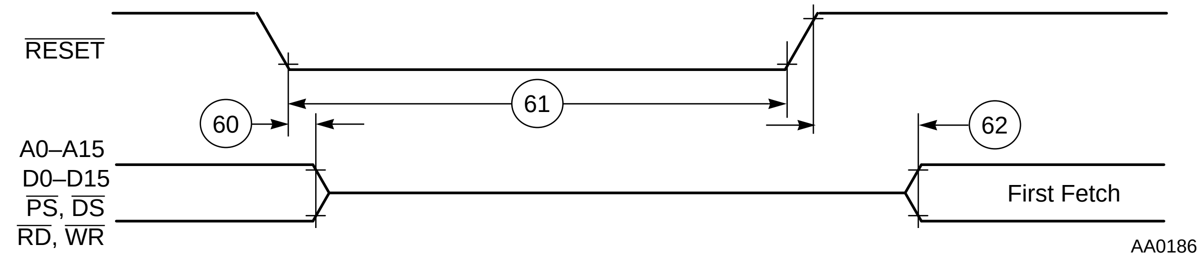


Figure 2-10 Asynchronous Reset Timing

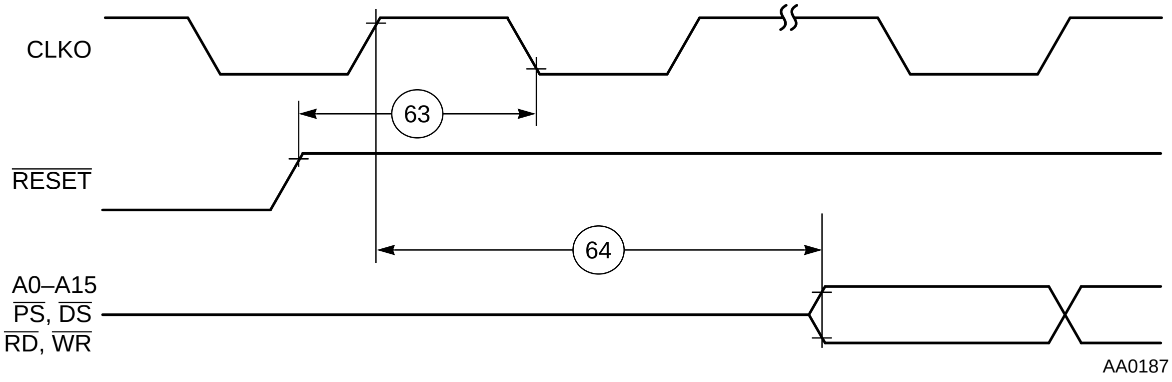


Figure 2-11 Synchronous Reset Timing

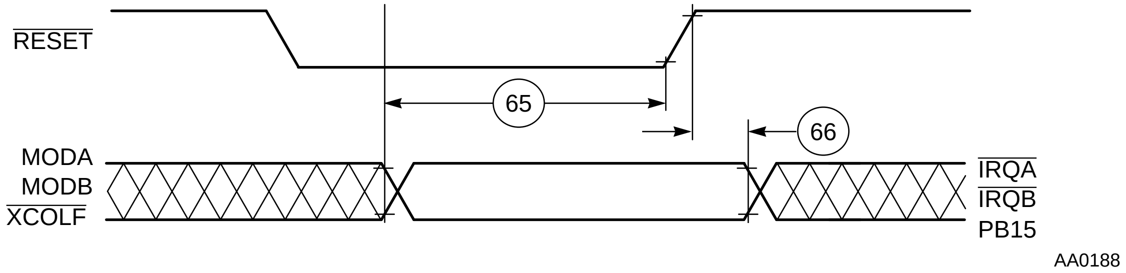


Figure 2-12 Operating Mode Select Timing

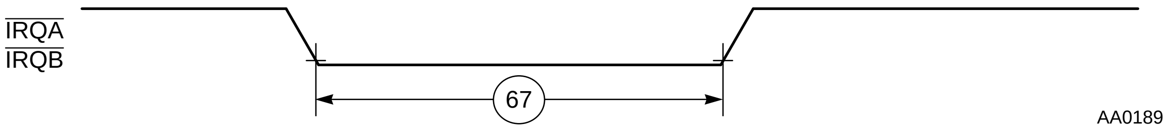


Figure 2-13 External Interrupt Timing (Negative Edge-Sensitive)

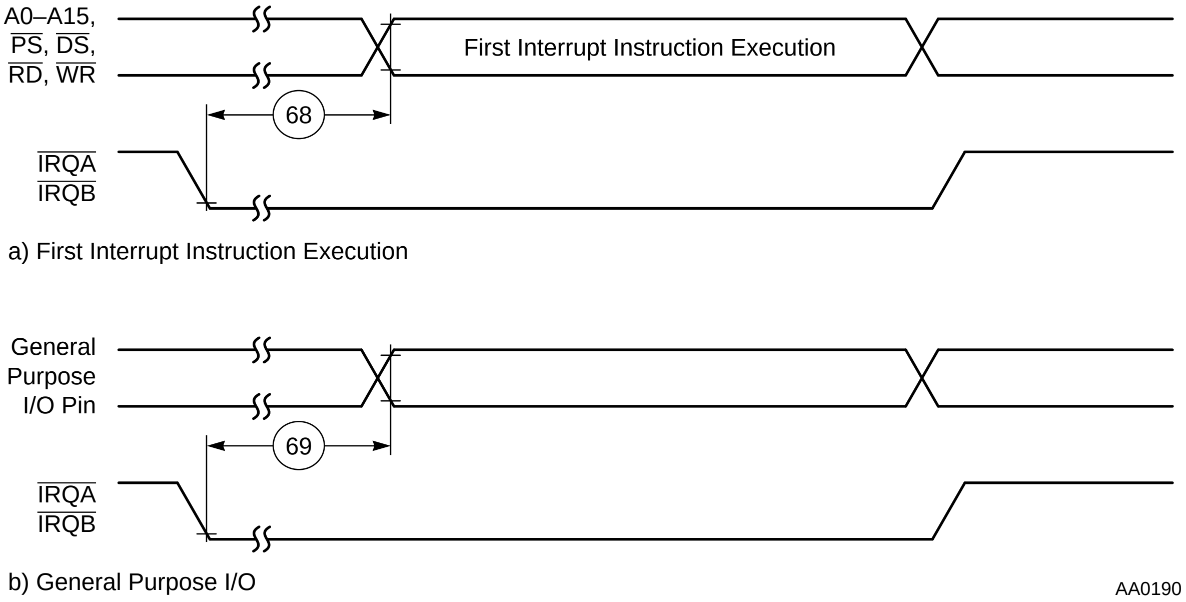


Figure 2-14 External Level-Sensitive Interrupt Timing

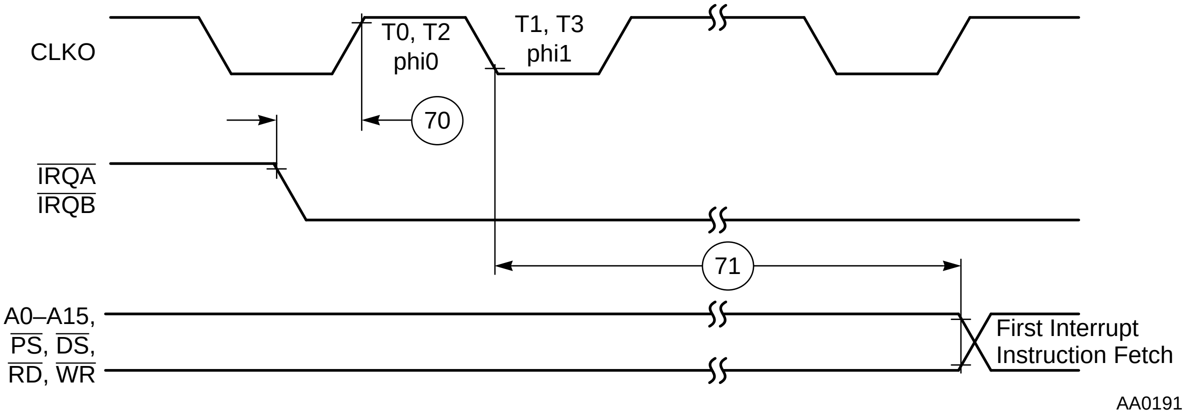


Figure 2-15 Synchronous Interrupt from Wait State Timing

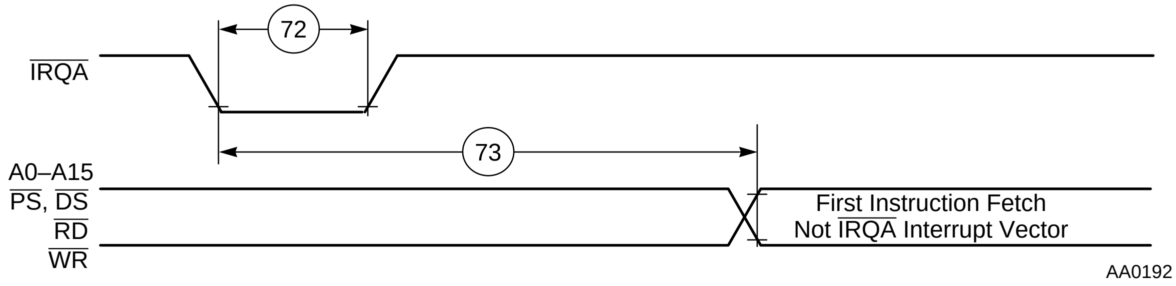


Figure 2-16 Recovery from Stop State Using Asynchronous Interrupt Timing

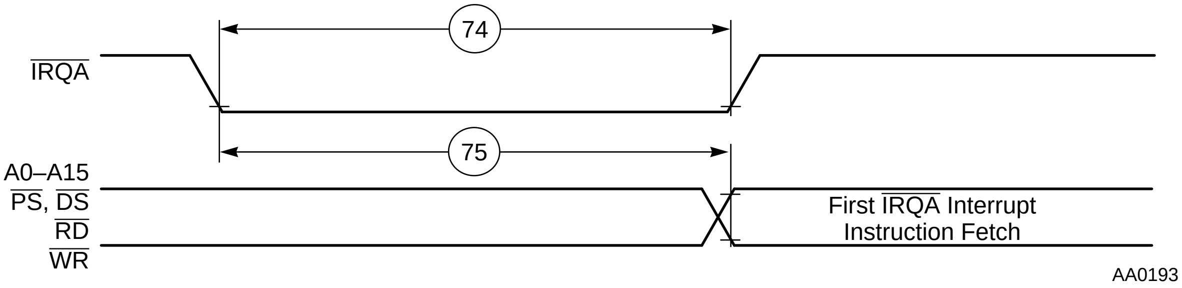


Figure 2-17 Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

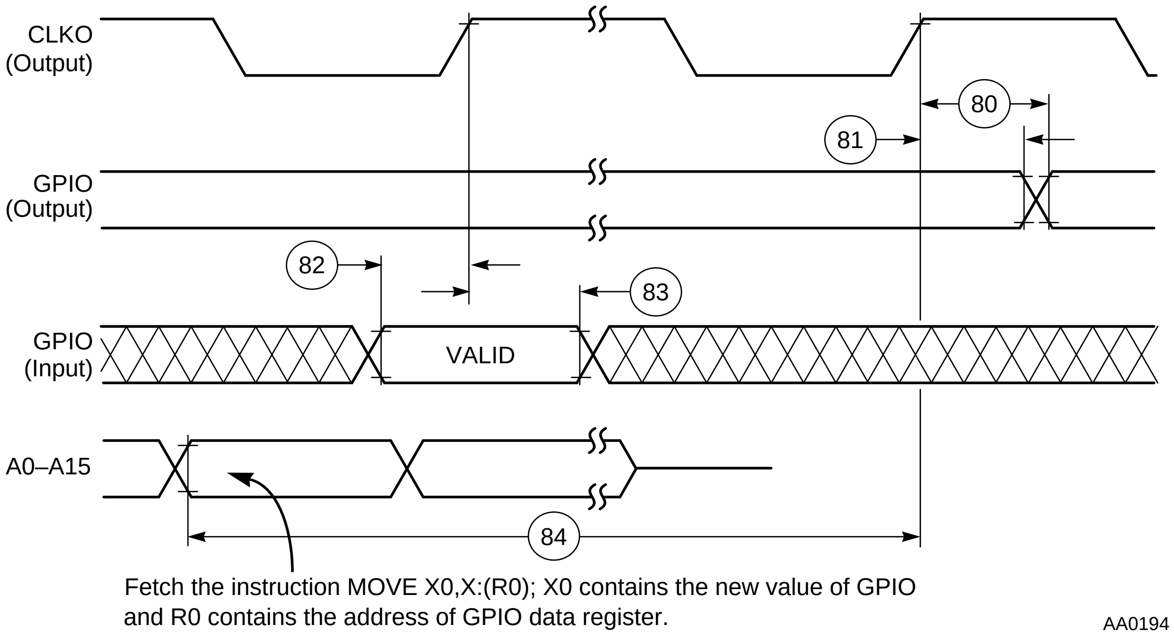
Port B and C Pin GPIO Timing

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

Table 2-11 GPIO Timing

No.	Characteristics	Min[1]	Max[1]	Unit
80	CLKO High to GPIO Out Valid (GPIO Out Delay Time)[3]	—	20	ns
81	CLKO High to GPIO Out Not Valid (GPIO Out Hold Time)	4.0	—	ns
82	GPIO In Valid to CLKO High (GPIO In Set-Up Time)	10.0	—	ns
83	CLKO High to GPIO In Not Valid (GPIO In Hold Time)	0.0	—	ns
84	Fetch to CLKO High Before GPIO Change	12T + 20	—	ns
85	Port B Interrupt Pulse Width	4T	—	ns
86	Port B Interrupt Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	27T + 6	—	ns
87	Port B Interrupt Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	31T + 27	—	ns

Notes:
1. In the formulas, T = the internal clock width (1/4 instruction cycle). For an internal frequency of 40 MHz, T = 12.5 ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   - after power-on reset, and
   - when recovering from Stopmode.
3. If a 10 kΩ pullup or pulldown resistor is connected to $\overline{\text{XCOLF}}$/PB15, add 3.9 ns for timings on $\overline{\text{XCOLF}}$/PB15.



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of GPIO data register.

Figure 2-18 GPIO Timing

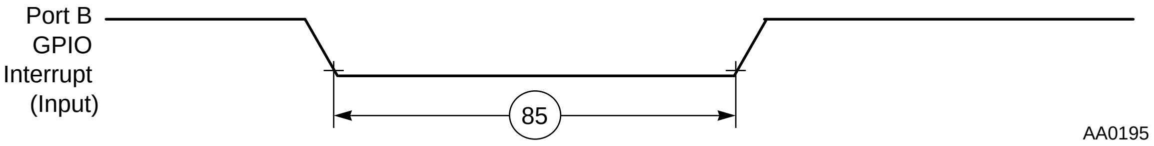


Figure 2-19 Port B Interrupt Timing (Negative Edge-Sensitive)

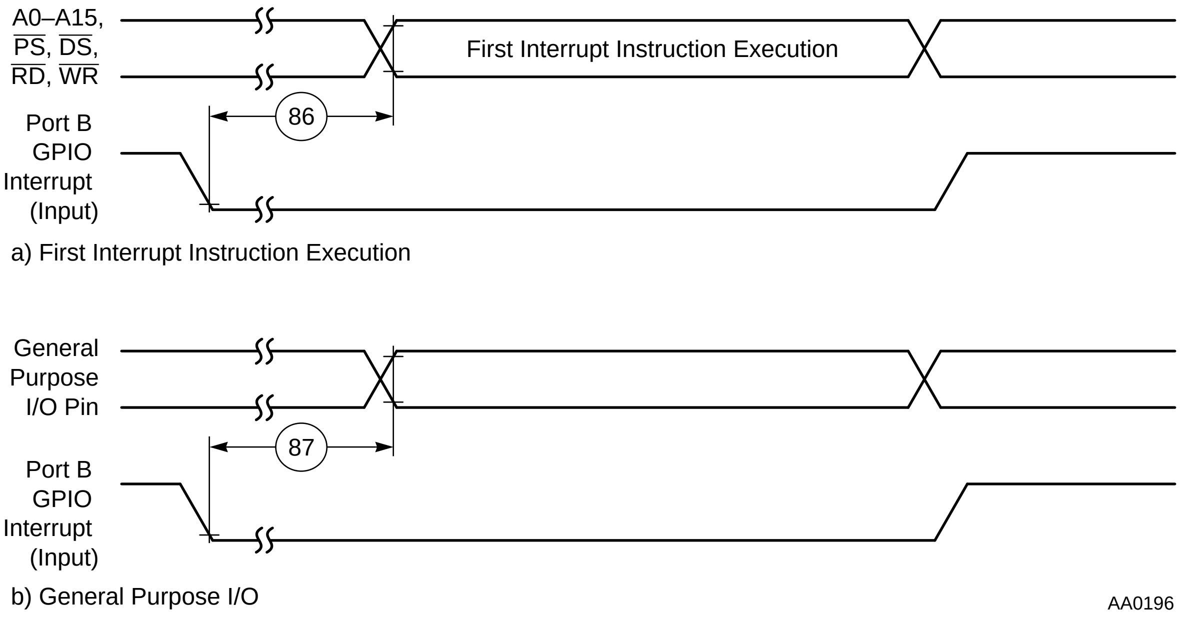


Figure 2-20 Port B GPIO Interrupt Timing

Serial Peripheral Interface (SPI) Timing

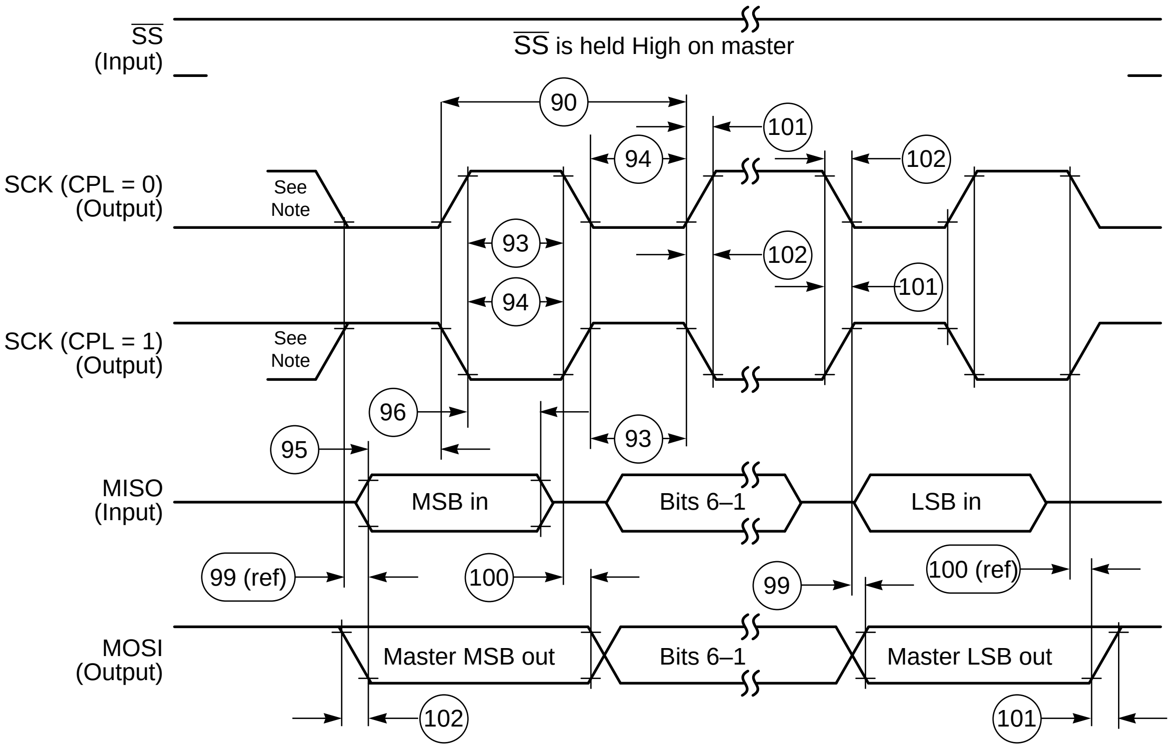
($V_{SS} = 0$ V, $V_{DD} = 2.7–3.6$ V, $T_A = –40°$ to $+85°C$)

Table 2-12 SPI Timing

No.	Characteristic	40 MHz				Unit
		20 pF Output Load		50 pF Output Load		
		Min	Max	Min	Max	
90	Cycle Time Master Slave	 100 100	 — —	 100 100	 — —	ns
91	Enable Lead Time Master Slave	 — 25	 — —	 — 25	 — —	ns
92	Enable Lag Time Master Slave	 — 100	 — —	 — 100	 — —	ns
93	Clock (SCK) High Time Master Slave	 50 40	 — —	 50 40	 — —	ns
94	Clock (SCK) Low Time Master Slave	 50 40	 — —	 50 40	 — —	ns
95	Data Setup Time (Inputs) Master Slave	 18 5	 — —	 24 5	 — —	ns
96	Data Hold Time (Inputs) Master Slave	 5 10	 — —	 5 10	 — —	ns
97	Access Time (Time to Data Active from High-Impedance State) Slave	 0	 25	 0	 35	ns
98	Disable Time (Hold Time to High-Impedance State) Slave	 —	 25	 —	 35	ns
99	Data Valid Master Slave (After Enable Edge)	 — —	 15 35	 — —	 15 40	ns

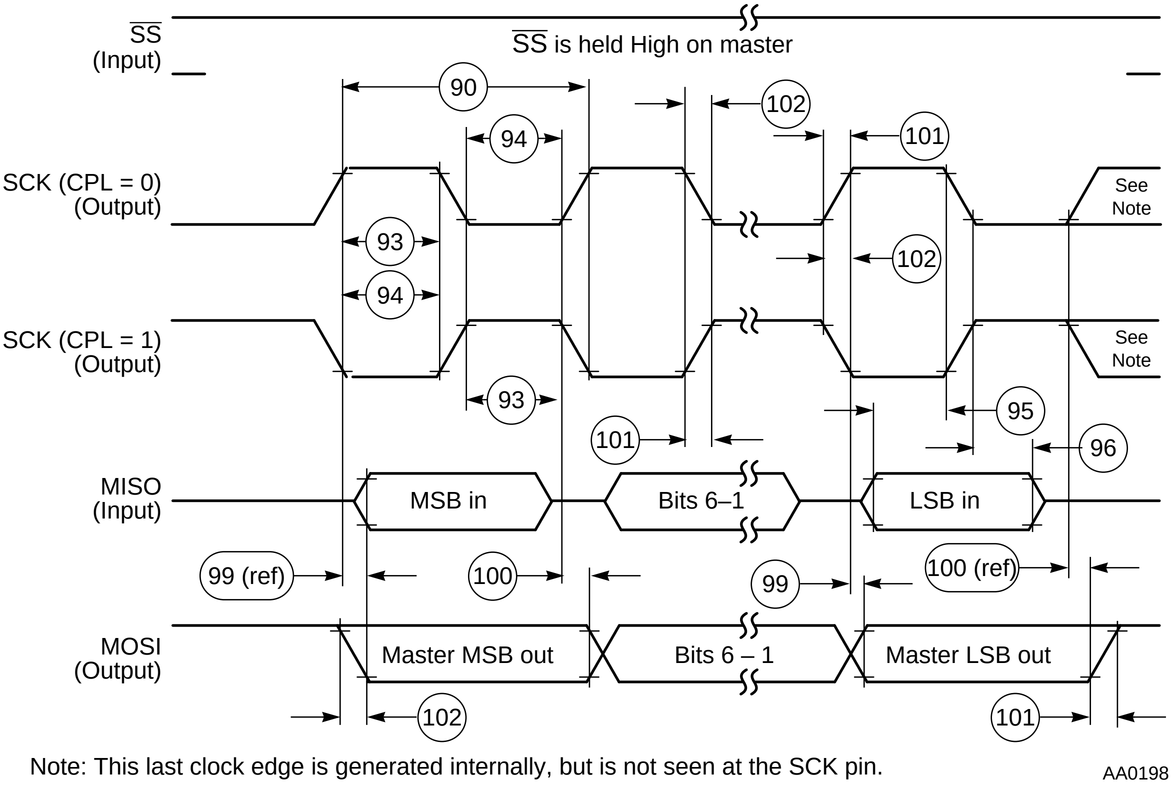
Table 2-12 SPI Timing (Continued)

No.	Characteristic	40 MHz				Unit
		20 pF Output Load		50 pF Output Load		
		Min	Max	Min	Max	
100	Data Hold Time					ns
	Master	0	—	0	—	
	Slave	0	—	0	—	
101	Rise Time					ns
	Master	2.8	8.9	3.5	13.9	
	Slave	2.8	8.9	3.5	13.9	
102	Fall Time					ns
	Master	2.2	6.9	2.8	11.7	
	Slave	2.2	6.9	2.8	11.7	



Note: This first clock edge is generated internally, but is not seen at the SCK pin.

Figure 2-21 SPI Master Timing (CPH = 0)



Note: This last clock edge is generated internally, but is not seen at the SCK pin.

Figure 2-22 SPI Master Timing (CPH = 1)

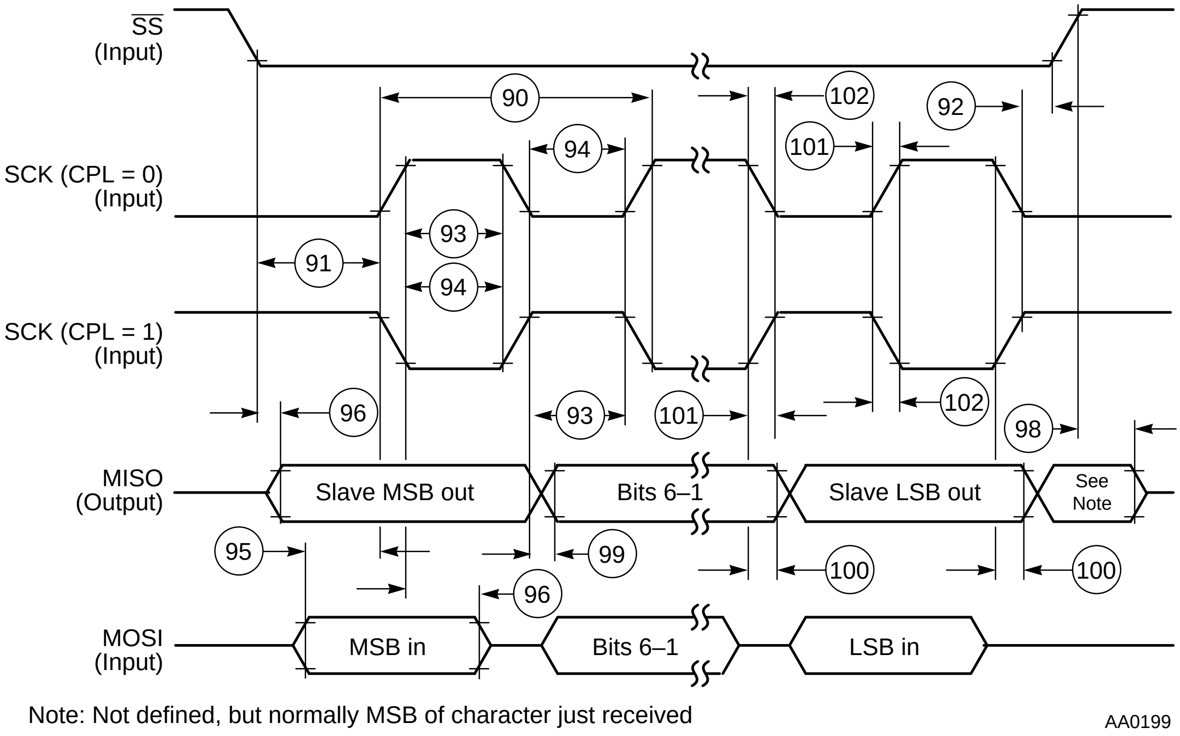


Figure 2-23 SPI Slave Timing (CPH = 0)

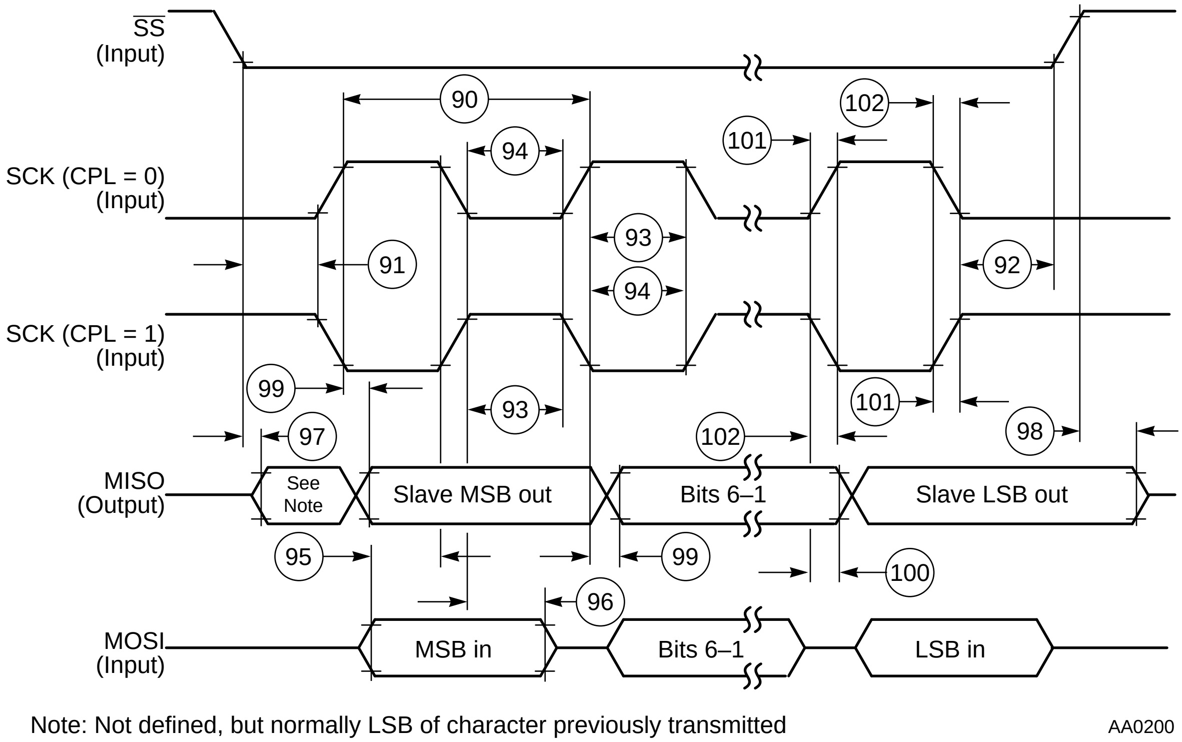


Figure 2-24 SPI Slave Timing (CPH = 1)

Synchronous Serial Interfaces (SSI) Timing

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

Table 2-13 SSI Timing

No.	Characteristic	40 MHz		Case[1]	Unit
		Min	Max		
Internal Clock Operation					
110	Clock Cycle[2]	100	—	i ck	ns
111	Clock High Period	38	—	i ck	ns
112	Clock Low Period	38	—	i ck	ns
113	Output Clock Rise/Fall Time	—	12	i ck	ns
114	STCK High to STFS (bl) High[3]	5.4	17.2	i ck	ns
115	SRCK High to SRFS (bl) High[3]	4	14.1	i ck	ns
116	STCK High to STFS (bl) Low[3]	4.9	15.6	i ck	ns
117	SRCK High to SRFS (bl) Low[3]	4	11.1	i ck	ns
118	SRD Setup Time before SRCK Low	6	—	i ck	ns
118	SRD Hold Time after SRCK Low (2T + 2)	52	—	i ck	ns
120	STCK High to STFS (wl) High[3]	7.1	21.2	i ck	ns
121	SRCK High to SRFS (wl) High[3]	5.4	17.8	i ck	ns
122	STCK High to STFS (wl) Low[3]	4.9	15.6	i ck	ns
123	SRCK High to SRFS (wl) Low[3]	4	11.1	i ck	ns
124	STCK High to STD Enable from High Impedance	2.7	5.8	i ck	ns
125	STCK High to STD Valid	3	9	i ck	ns
126	STCK High to STD Invalid	3	6.9	i ck	ns
127	STCK High to STD High Impedance	3	7.9	i ck	ns
External Clock Operation					
128	Clock Cycle[2]	100	—	x ck	ns
129	Clock High Period	46	—	x ck	ns
130	Clock Low Period	46	—	x ck	ns
131	Output Clock Rise/Fall Time	—	4	x ck	ns
132	SRD Setup Time before SRCK Low	6	—	x ck	ns

Table 2-13 SSI Timing (Continued)

No.	Characteristic	40 MHz		Case[1]	Unit
		Min	Max		
133	SRD Hold Time after SRCK Low[4] (2T + 2)	52	—	x ck	ns
134	STCK High to STFS (bl) High[3]	—	43	x ck	ns
135	SRCK High to SRFS (bl) High[3]	—	43	x ck	ns
136	STCK High to STFS (bl) Low[3]	2	—	x ck	ns
137	SRCK High to SRFS (bl) Low[3]	2	—	x ck	ns
138	STCK High to STFS (wl) High[3]	—	43	x ck	ns
139	SRCK High to SRFS (wl) High[3]	—	43	x ck	ns
140	STCK High to STFS (wl) Low[3]	2	—	x ck	ns
141	SRCK High to SRFS (wl) Low[3]	2	—	x ck	ns
142	STCK High to STD Enable from High Impedance	2.8	8.6	x ck	ns
143	STCK High to STD Valid	3.5	10.3	x ck	ns
144	STCK High to STD Invalid	2.6	8.1	x ck	ns
145	STCK High to STD High Impedance	3.2	9.1	x ck	ns
Synchronous Internal Clock Operation (in addition to standard internal clock parameters)					
146	SRD Setup before STCK Falling	7	—	i ck s	ns
147	SRD Hold after STCK Falling[4] (4T+2)	52	—	i ck s	ns
Synchronous External Clock Operation (in addition to standard external clock parameters)					
148	SRD Setup before STCK Falling	7	—	x ck s	ns
149	SRD Hold after STCK Falling[4] (4T+2)	52	—	x ck s	ns

Notes:
1. The following abbreviations are used to represent the various operational cases:
   i ck = Internal Clock and Frame Sync
   x ck = External Clock and Frame Sync
   i ck s = Internal Clock, Synchronous mode (implies that only one frame sync FS is used)
   x ck s = External Clock, Synchronous mode (implies that only one frame sync FS is used)
2. All the timings for the SSI are given for a non-inverted serial clock polarity (SCKP = 0 in CRB) and a non-inverted frame sync (FSI = 0 in CRB). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal SCK and/or the frame sync FSR/FST in the tables and in the figures.
3. bl = bit length; wl = word length.
4. T = the internal clock width (1/4 instruction cycle). For an internal frequency of 40 MHz, T = 12.5 ns.

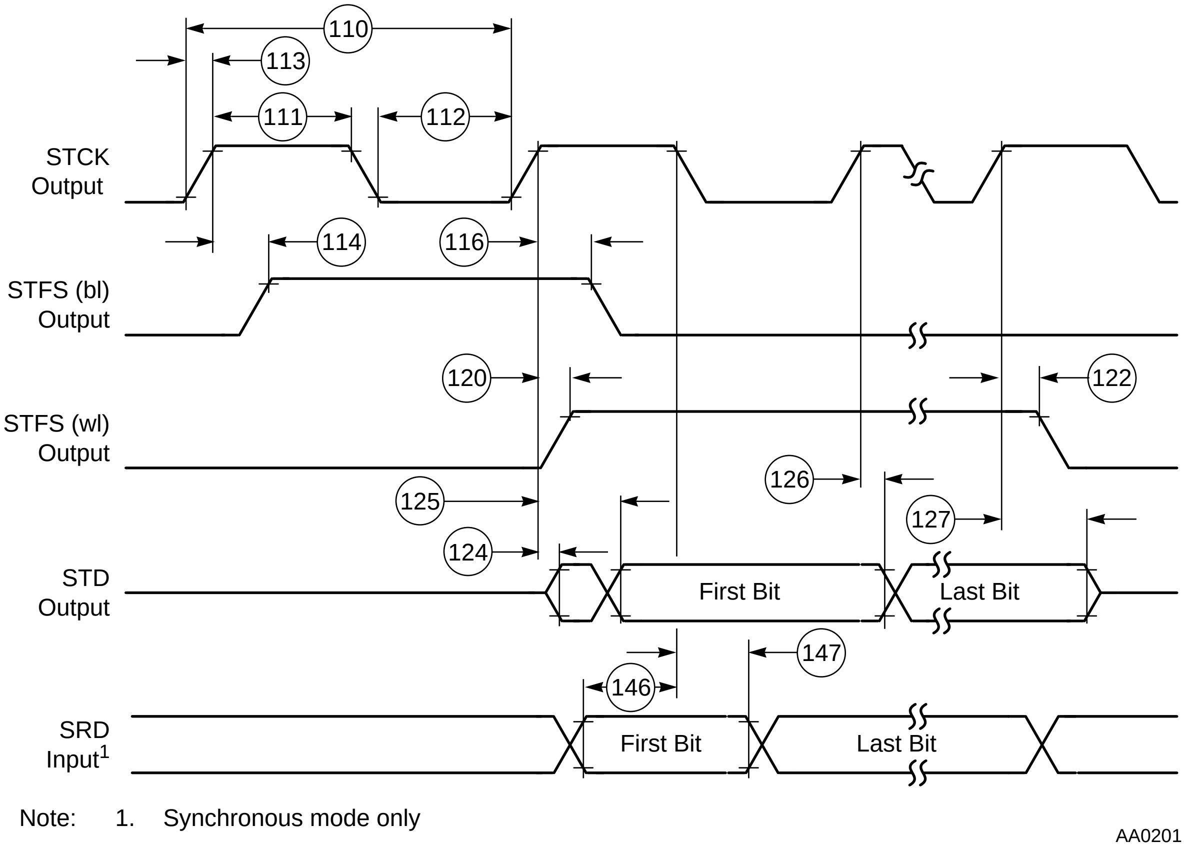


Figure 2-25 SSI Transmitter Internal Clock Timing

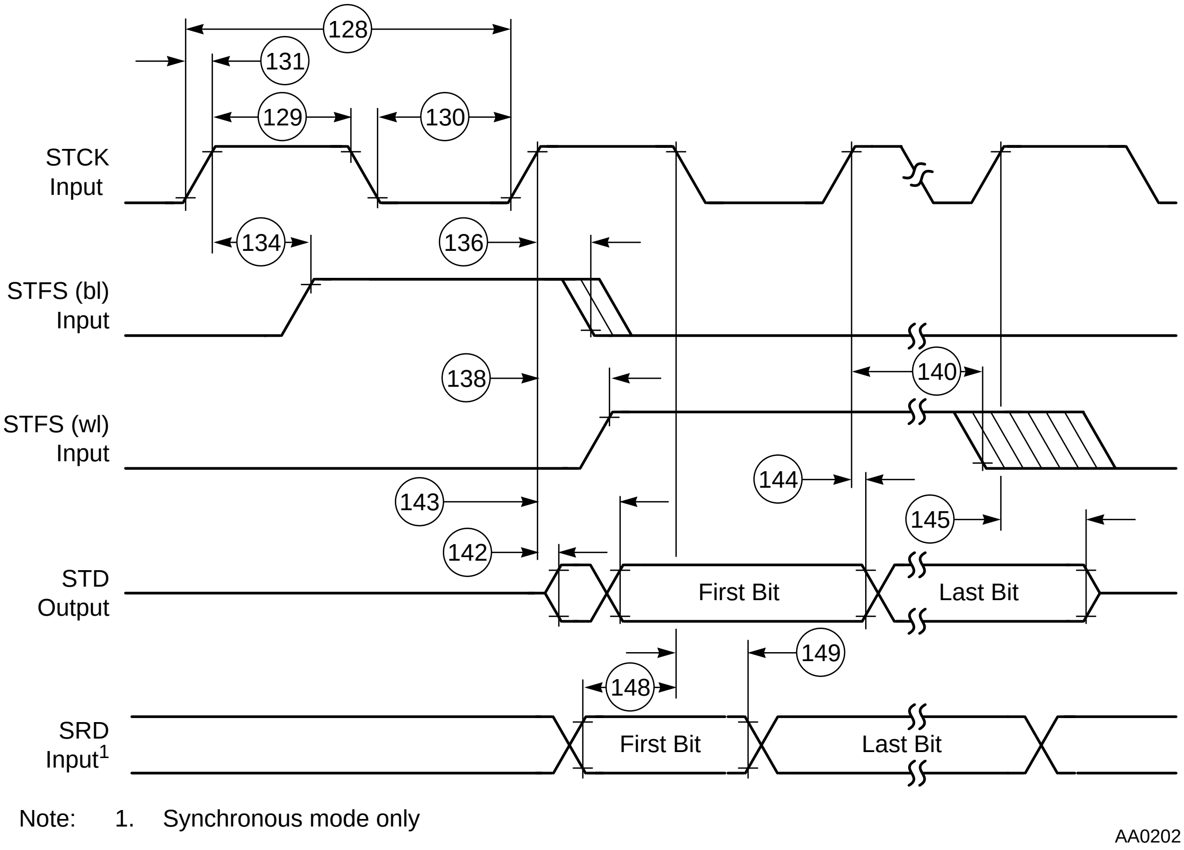


Figure 2-26 SSI Transmitter External Clock Timing

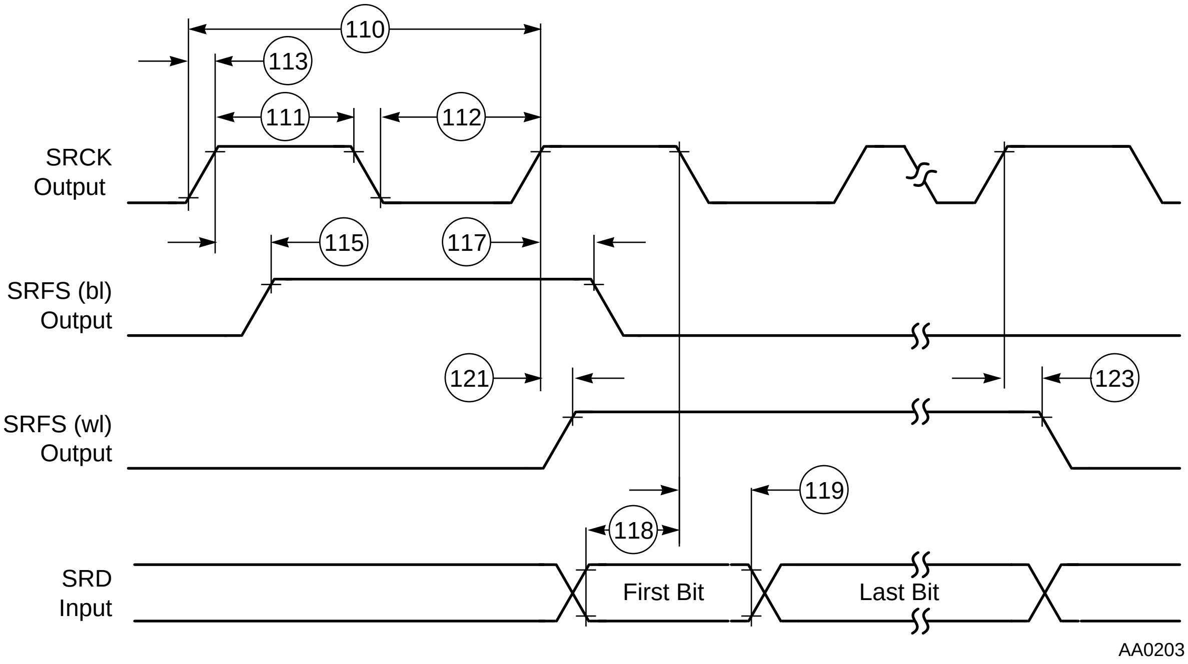


Figure 2-27 SSI Receiver Internal Clock Timing

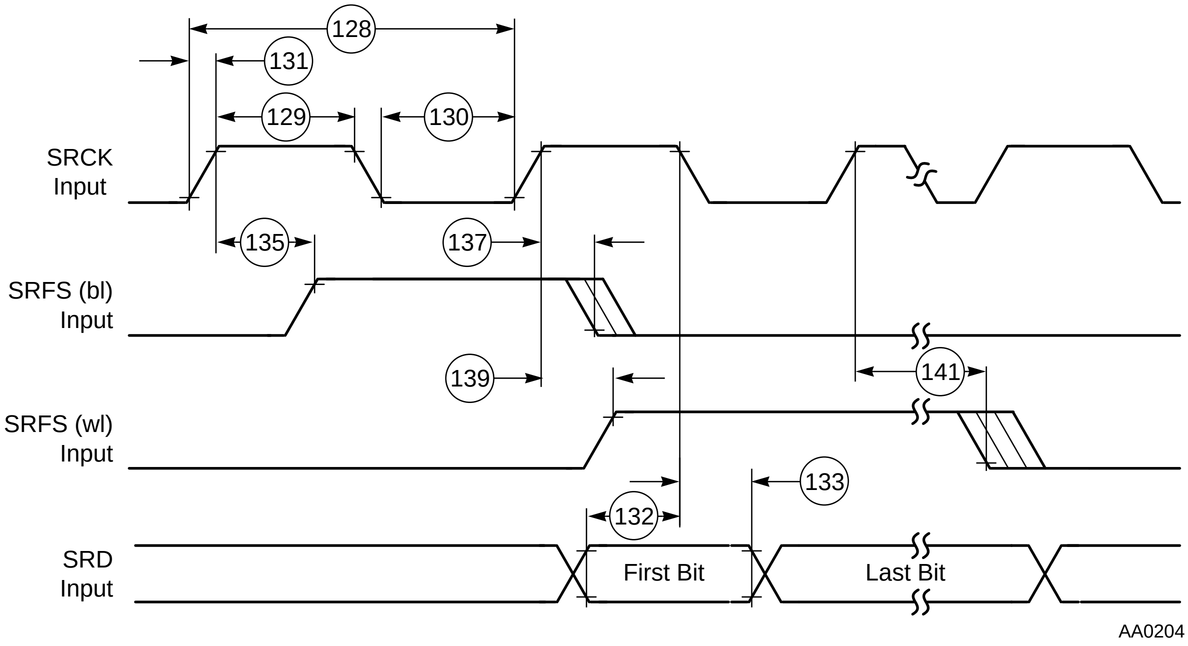


Figure 2-28 SSI Receiver External Clock Timing

Timer Timing

($V_{SS} = 0$ V, $V_{DD} = 2.7–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L = 50$ pF)

Table 2-14 Timer Timing

No.	Characteristic	40 MHz		Unit
		Min	Max	
150	Timer Input Valid to CLKO High (Setup time)	11	—	ns
151	CLKO High to Timer Input Invalid (Hold time)	0	—	ns
152	CLKO High to Timer Output Asserted	3.5	14	ns
153	CLKO High to Timer Output Deasserted	5.1	20.7	ns
154	Timer Input Period	8T	—	ns
155	Timer Input High/Low Period	4T	—	ns

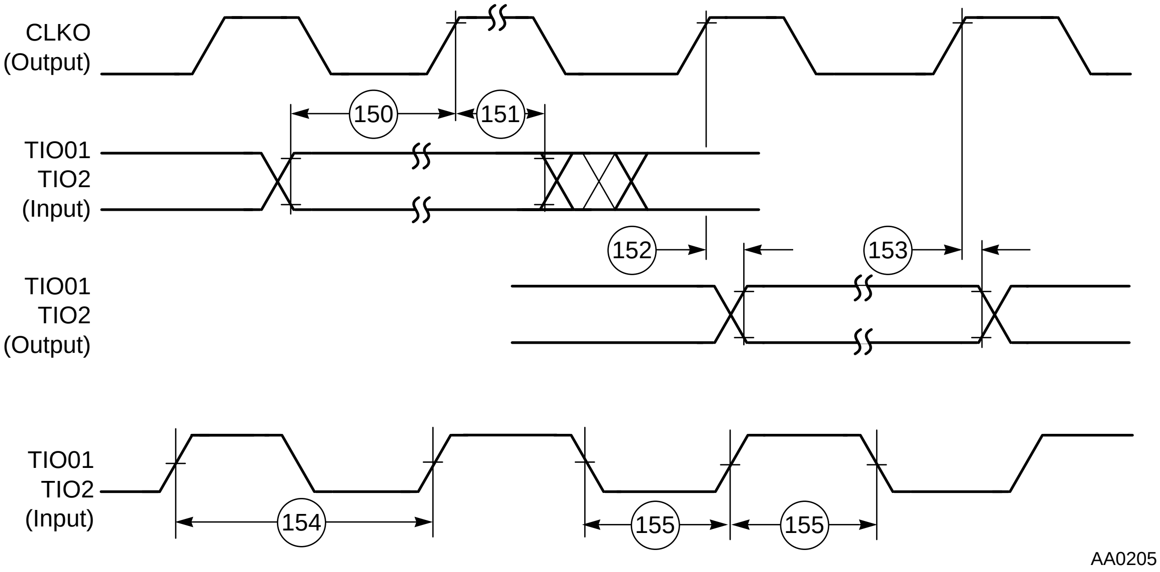


Figure 2-29 Timer Timing

JTAG Timing

(V_{SS} = 0 V, V_{DD} = 2.7–3.6 V, T_A = –40° to +85°C, C_L = 50 pF)

Table 2-15 JTAG Timing

No.	Characteristics	40 MHz		Unit
		Min	Max	
160	TCK Frequency of Operation	0.0	13.33	MHz
161	TCK Cycle Time in Crystal Mode	75.0	—	ns
162	TCK Clock Pulse Width	37.2	—	ns
163	TCK Rise and Fall Times	—	4.0	ns
164	Boundary Scan Input Data Setup Time	13.0	—	ns
165	Boundary Scan Input Data Hold Time	39.5	—	ns
166	TCK Low to Output Data Valid	—	19.0	ns
167	TCK Low to Output Tri-state	—	19.0	ns
168	TMS, TDI Data Setup Time	8.0	—	ns
169	TMS, TDI Data Hold Time	39.5	—	ns
170	TCK Low to TDO Data Valid	—	20.0	ns
171	TCK Low to TDO Tri-state	—	20.0	ns
172	$\overline{\text{TRST}}$ Assertion Time	37.5	—	ns
173	$\overline{\text{DE}}$ Assertion Time	100.0	—	ns

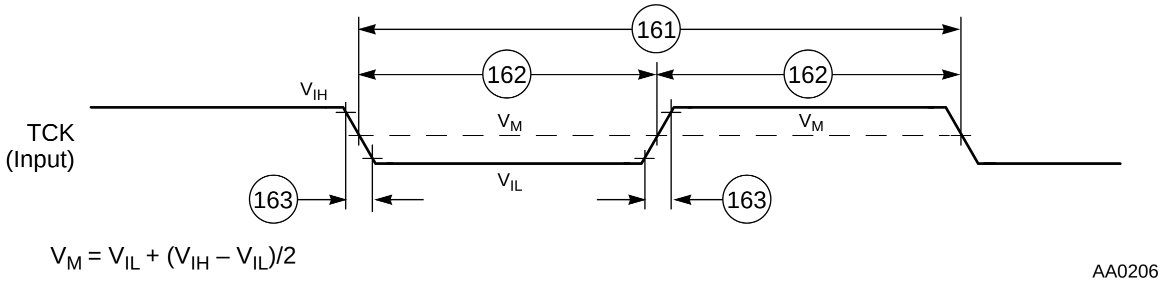


Figure 2-30 Test Clock Input Timing Diagram

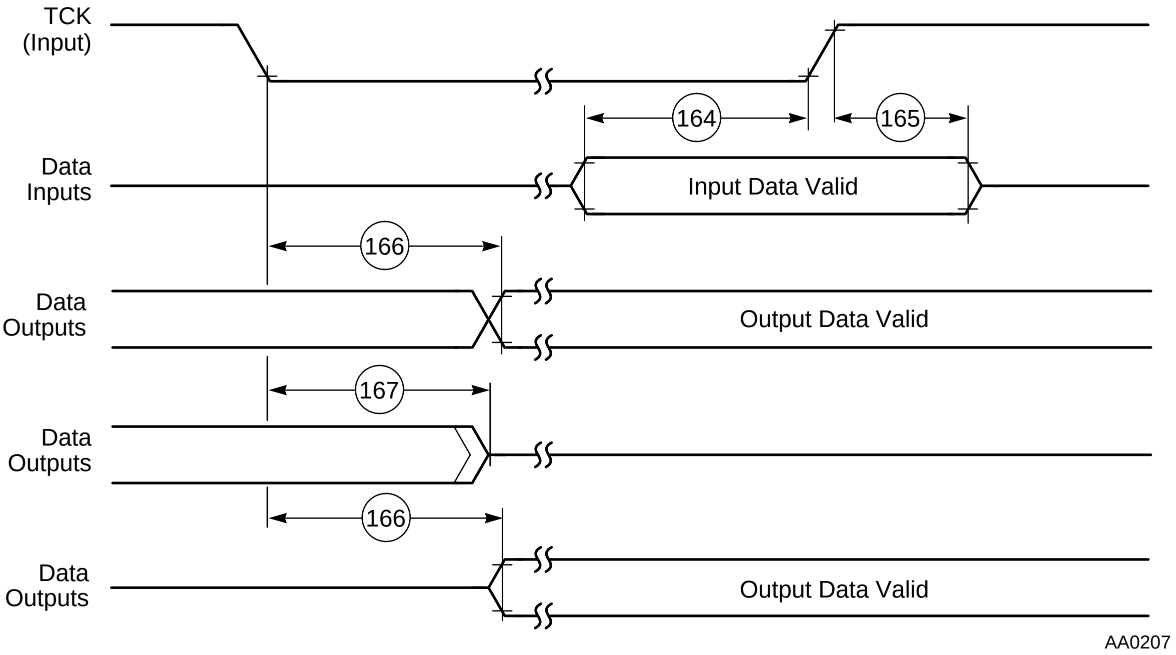


Figure 2-31 Boundary Scan (JTAG) Timing Diagram

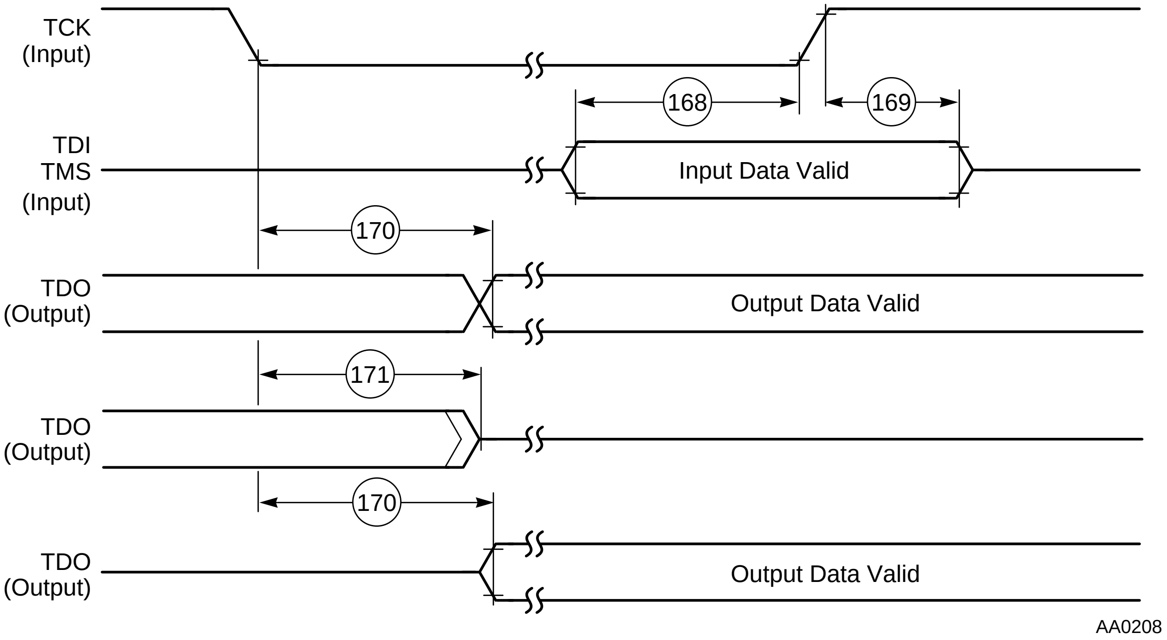


Figure 2-32 Test Access Port Timing Diagram

Figure 2-33 $\overline{\text{TRST}}$ Timing Diagram

Figure 2-34 OnCE—Debug Event

SECTION 3

PACKAGING

PACKAGE AND PIN-OUT INFORMATION

This section contains package and pin-out information for the 100-pin Thin Quad Flat Pack (TQFP) configuration of the DSP56L811.

Complete mechanical information regarding DSP56L811 packaging is available by facsimile through Motorola's Mfax™ system. Call (602) 244-6609 to obtain instructions for using this system. The automated system requests the following information:

- The receiving fax telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

  Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The mechanical drawings for the 100-pin TQFP package are referenced as 983-01.

100-pin TQFP Configuration

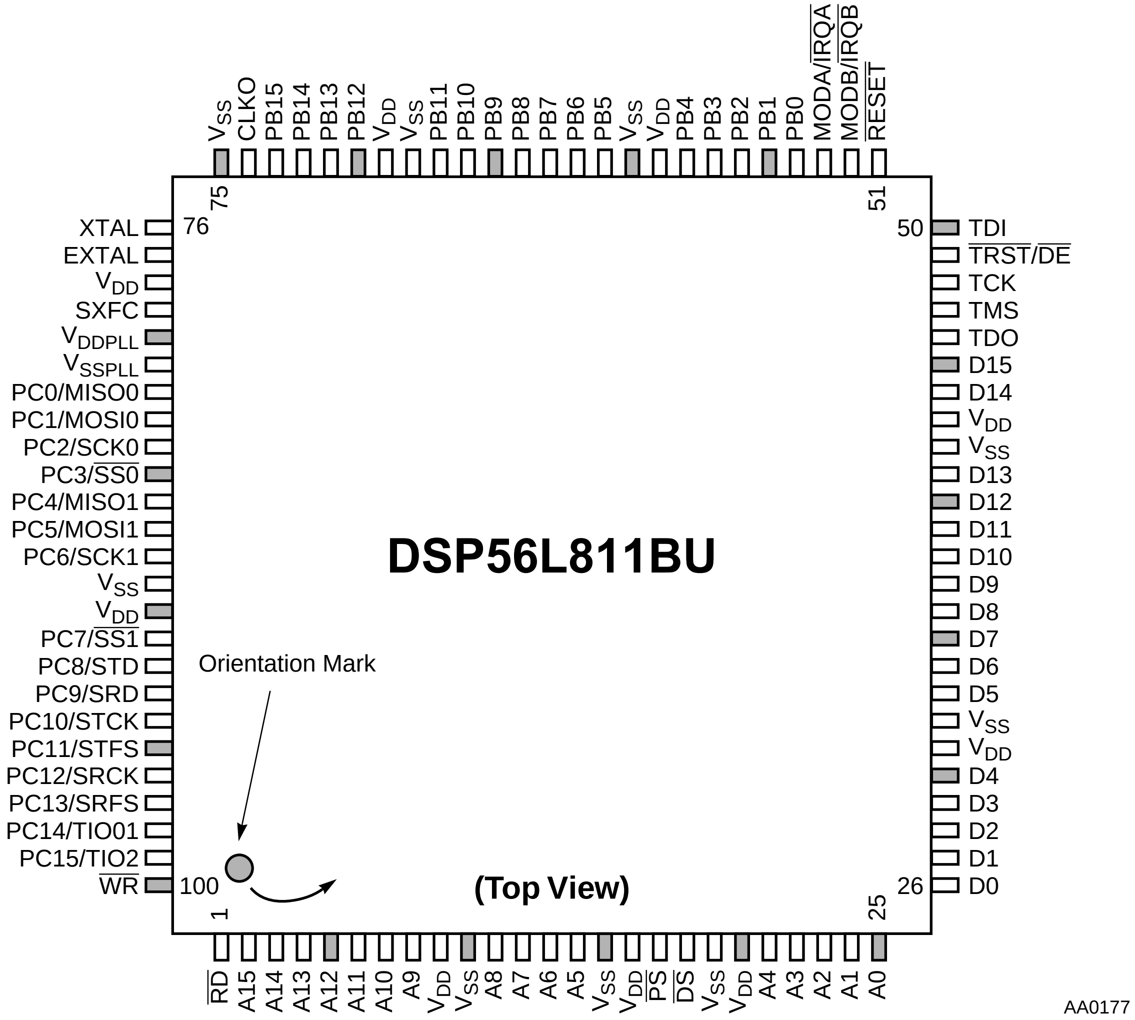


Figure 3-1 Top View of the DSP56L811 100-pin Plastic Thin Quad Flat Package (BU)

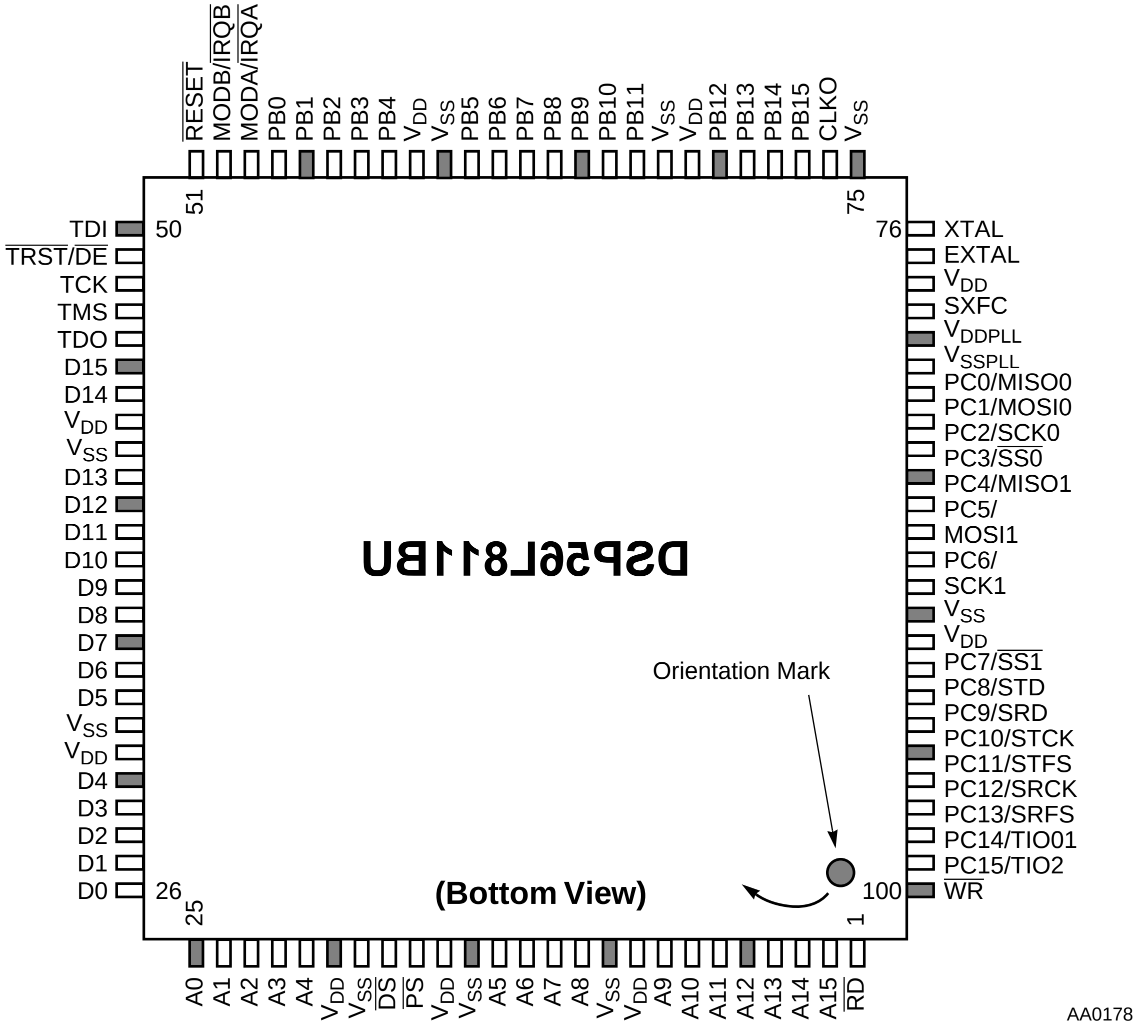


Figure 3-2 Bottom View of the DSP56L811 100-pin Plastic Thin Quad Flat Package (BU)

Table 3-1 DSP56L811 Pin Identification by Pin Number

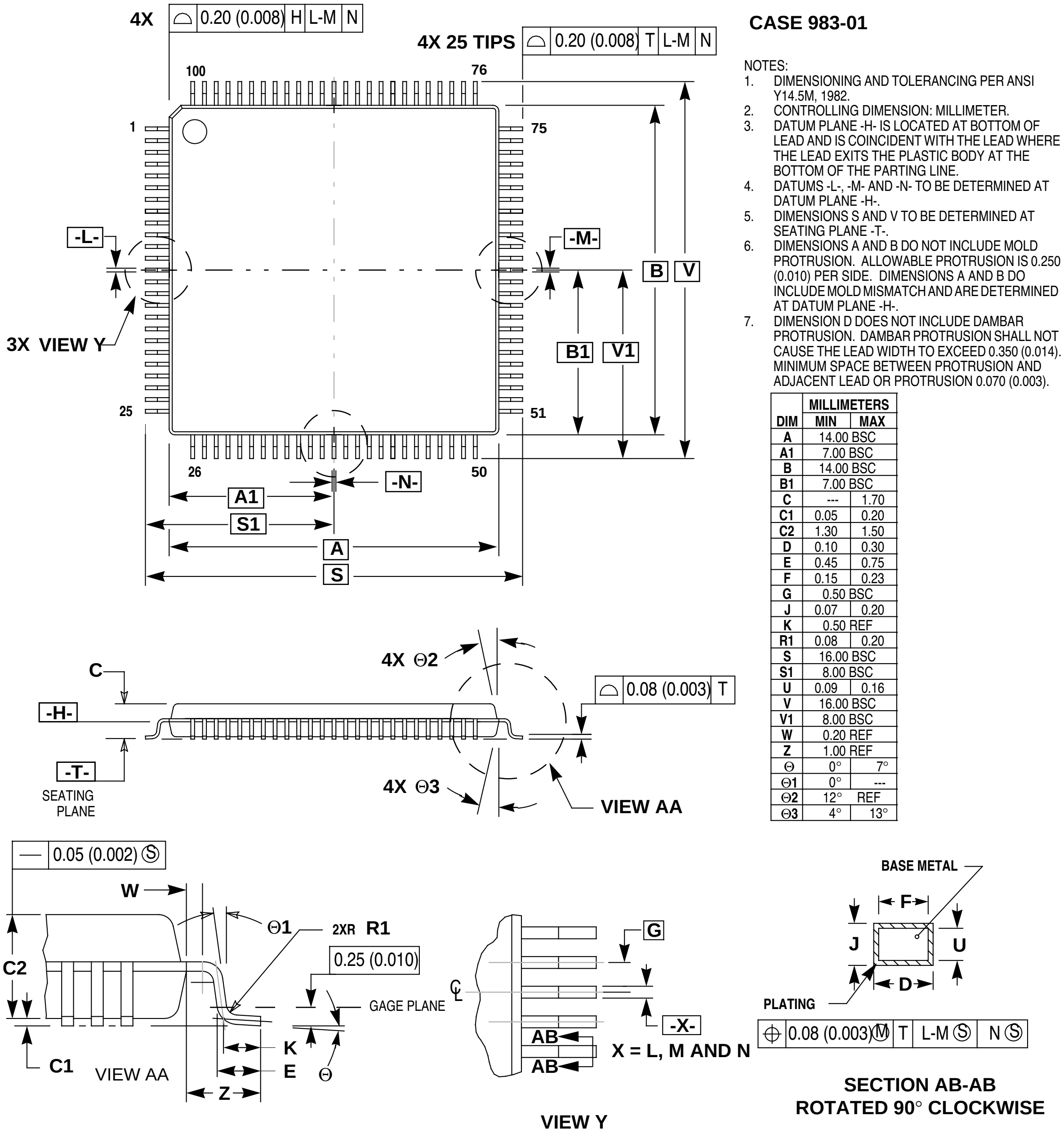
100-pin Package Pin #	Signal Name	100-pin Package Pin #	Signal Name	100-pin Package Pin #	Signal Name	100-pin Package Pin #	Signal Name
1	$\overline{RD}$	26	D0	51	$\overline{RESET}$	76	XTAL
2	A15	27	D1	52	MODB/$\overline{IRQB}$	77	EXTAL
3	A14	28	D2	53	MODA/$\overline{IRQA}$	78	V_{DD}
4	A13	29	D3	54	PB0	79	SXFC
5	A12	30	D4	55	PB1	80	V_{DDPLL}
6	A11	31	V_{DD}	56	PB2	81	V_{SSPLL}
7	A10	32	V_{SS}	57	PB3	82	PC0/MISO0
8	A9	33	D5	58	PB4	83	PC1/MOSI0
9	V_{DD}	34	D6	59	V_{DD}	84	PC2/SCK0
10	V_{SS}	35	D7	60	V_{SS}	85	PC3/$\overline{SS0}$
11	A8	36	D8	61	PB5	86	PC4/MISO1
12	A7	37	D9	62	PB6	87	PC5/MOSI1
13	A6	38	D10	63	PB7	88	PC6/SCK1
14	A5	39	D11	64	PB8	89	V_{SS}
15	V_{SS}	40	D12	65	PB9	90	V_{DD}
16	V_{DD}	41	D13	66	PB10	91	PC7/$\overline{SS1}$
17	PS	42	V_{SS}	67	PB11	92	PC8/STD
18	DS	43	V_{DD}	68	V_{SS}	93	PC9/SRD
19	V_{SS}	44	D14	69	V_{DD}	94	PC10/STCK
20	V_{DD}	45	D15	70	PB12	95	PC11/STFS
21	A4	46	TDO	71	PB13	96	PC12/SRCK
22	A3	47	TMS	72	PB14	97	PC13/SRFS
23	A2	48	TCK	73	PB15	98	PC14/TIO01
24	A1	49	$\overline{TRST}$/$\overline{DE}$	74	CLKO	99	PC15/TIO2
25	A0	50	TDI	75	V_{SS}	100	$\overline{WR}$

Table 3-2 DSP56L811 General Purpose I/O Pin Identification

100-pin Package Pin #	DSP56L811 Primary Pin Function	DSP56L811 General Purpose I/O ID
54	—	PB0
55	—	PB1
56	—	PB2
57	—	PB3
58	—	PB4
61	—	PB5
62	—	PB6
63	—	PB7
64	—	PB8
65	—	PB9
66	—	PB10
67	—	PB11
70	—	PB12
71	—	PB13
72	—	PB14
73	—	PB15
82	MISO0	PC0
83	MOSI0	PC1
84	SCK0	PC2
85	$\overline{\text{SS0}}$	PC3
86	MISO1	PC4
87	MOSI1	PC5
88	SCK1	PC6
91	$\overline{\text{SS1}}$	PC7
92	STD	PC8
93	SRD	PC9
94	STCK	PC10
95	STFS	PC11
96	SRCK	PC12
97	SRFS	PC13
98	TIO01	PC14
99	TIO2	PC15

Table 3-3 DSP56L811 Power Supply Pins

100-pin Package Pin #	Power Signal	Circuits Supplied
9	V_{DD}	Address Bus Buffers and Bus Control
20	V_{DD}	
10	V_{SS}	
19	V_{SS}	
90	V_{DD}	Port C and Bus Control
89	V_{SS}	
80	V_{DDPLL}	PLL
81	V_{SSPLL}	
78	V_{DD}	Clock, Port B, JTAG/OnCE Port
75	V_{SS}	
59	V_{DD}	
60	V_{SS}	
31	V_{DD}	Data Bus Buffers
43	V_{DD}	
32	V_{SS}	
42	V_{SS}	
69	V_{DD}	Internal Logic
16	V_{DD}	
68	V_{SS}	
15	V_{SS}	



CASE 983-01

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350 (0.014). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.070 (0.003).

DIM	MILLIMETERS	
	MIN	MAX
A	14.00 BSC	
A1	7.00 BSC	
B	14.00 BSC	
B1	7.00 BSC	
C	---	1.70
C1	0.05	0.20
C2	1.30	1.50
D	0.10	0.30
E	0.45	0.75
F	0.15	0.23
G	0.50 BSC	
J	0.07	0.20
K	0.50 REF	
R1	0.08	0.20
S	16.00 BSC	
S1	8.00 BSC	
U	0.09	0.16
V	16.00 BSC	
V1	8.00 BSC	
W	0.20 REF	
Z	1.00 REF	
Θ	0°	7°
Θ1	0°	---
Θ2	12° REF	
Θ3	4°	13°

Figure 3-3 100-pin Thin Quad Flat Pack (TQFP) Mechanical Information

SECTION 4

DESIGN CONSIDERATIONS

HEAT DISSIPATION

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature ˚C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance ˚C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ˚C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the printed circuit board, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the printed circuit board to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

1. Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
2. Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
3. Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

Note: **Table 2-3 Package Thermal Characteristics** on page 2-2 contains the package thermal values for this chip.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{DD}).

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{DD} pin on the DSP, and from the board ground to each V_{SS} (GND) pin.
- The minimum bypass requirement is to place six 0.01–0.1 µF capacitors positioned as close as possible to the package supply pins, one capacitor for each of the "Circuits Supplied" groups listed in **Table 3-3** on page 3-6∑∑. The recommended bypass configuration is to place one bypass capacitor on each of the ten V_{DD}/V_{SS} pairs, including $V_{DDPLL}/V_{SSPLL.}$
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{DD} and V_{SS} (GND) pins are less than 0.5" per capacitor lead.
- Use at least a four-layer Printed Circuit Board (PCB) with two inner layers for V_{DD} and GND.
- Bypass the V_{DD} and GND layers of the PCB with approximately 100 µF, preferably with a high-grade capacitor such as a tantalum capacitor.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and GND circuits.
- All inputs must be terminated (i.e., not allowed to float) using CMOS levels.
- Take special care to minimize noise levels on the V_{DDPLL} and V_{SSPLL} pins.

- When using Wired-OR mode on the SPI or the MODx/$\overline{\mathrm{IRQx}}$ pins, the user must provide an external pull-up device.
- Designs that utilize the $\overline{\mathrm{TRST}}$/$\overline{\mathrm{DE}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\mathrm{TRST}}$ whenever $\overline{\mathrm{RESET}}$ is asserted, as well as a means to assert $\overline{\mathrm{TRST}}$ independently of $\overline{\mathrm{RESET}}$. Designs that do not require debugging functionality, such as consumer products, should tie these pins together.

SECTION 5

ORDERING INFORMATION

Table 5-1 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 5-1 DSP56L811 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56L811	2.7–3.6V	Plastic Thin Quad Flat Pack (TQFP)	100	40	DSP56L811BU40

OnCE and Mfax are trademarks of Motorola, Inc.

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters which may be provided in Motorola data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and Ⓜ are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/ Affirmative Action Employer.

How to reach us:

UUSA/Europe/Locations Not Listed:
Motorola Literature Distribution
P.O. Box 5405
Denver, Colorado 80217
303-675-2140
1 (800) 441-2447

Mfax™:
RMFAX0@email.sps.mot.com
TOUCHTONE (602) 244-6609

Asia/Pacific:
Motorola Semiconductors H.K. Ltd.
8B Tai Ping Industrial Park
51 Ting Kok Road
Tai Po, N.T., Hong Kong
852-2662928

Technical Resource Center:
1 (800) 521-6274

DSP Helpline
dsphelp@dsp.sps.mot.com

Japan:
Nippon Motorola Ltd.
Tatsumi-SPD-JLDC
6F Seibu-Butsuryu-Center
3-14-2 Tatsumi Koto-Ku
Tokyo 135, Japan
81-3-3521-8315

Internet:
http://www.motorola-dsp.com

MOTOROLA