DSP56602

Advance Information

16-BIT DIGITAL SIGNAL PROCESSOR

The DSP56602 is a ROM-based 16-bit fixed-point CMOS Digital Signal Processor (DSP) designed for low-power digital cellular subscriber applications. The DSP56602 is optimized for processing-intensive, yet cost-effective, low power consumption digital mobile communications applications. The DSP56602 is a member of the DSP56600 core family of DSPs, and is capable of executing one instruction per clock cycle. The DSP56602 provides for customer-specifiable, factory-programmed ROM. Application development can be performed using the DSP56603EVM Evaluation Module or the DSP56603ADS Application Development System. **Figure 1** provides a block diagram of the DSP56602, showing the core structures and the expansion areas. The DSP56600 core includes the Data Arithmetic Logic Unit (Data ALU), Address Generation Unit (AGU), Program Controller, Program Patch Detector, Bus Interface Unit, On-Chip Emulation (OnCE™) module, JTAG port, and a Phase Lock Loop (PLL)-based clock generator. The expansion areas provide the program and data memories, as well as a versatile set of on-chip peripherals and external ports.

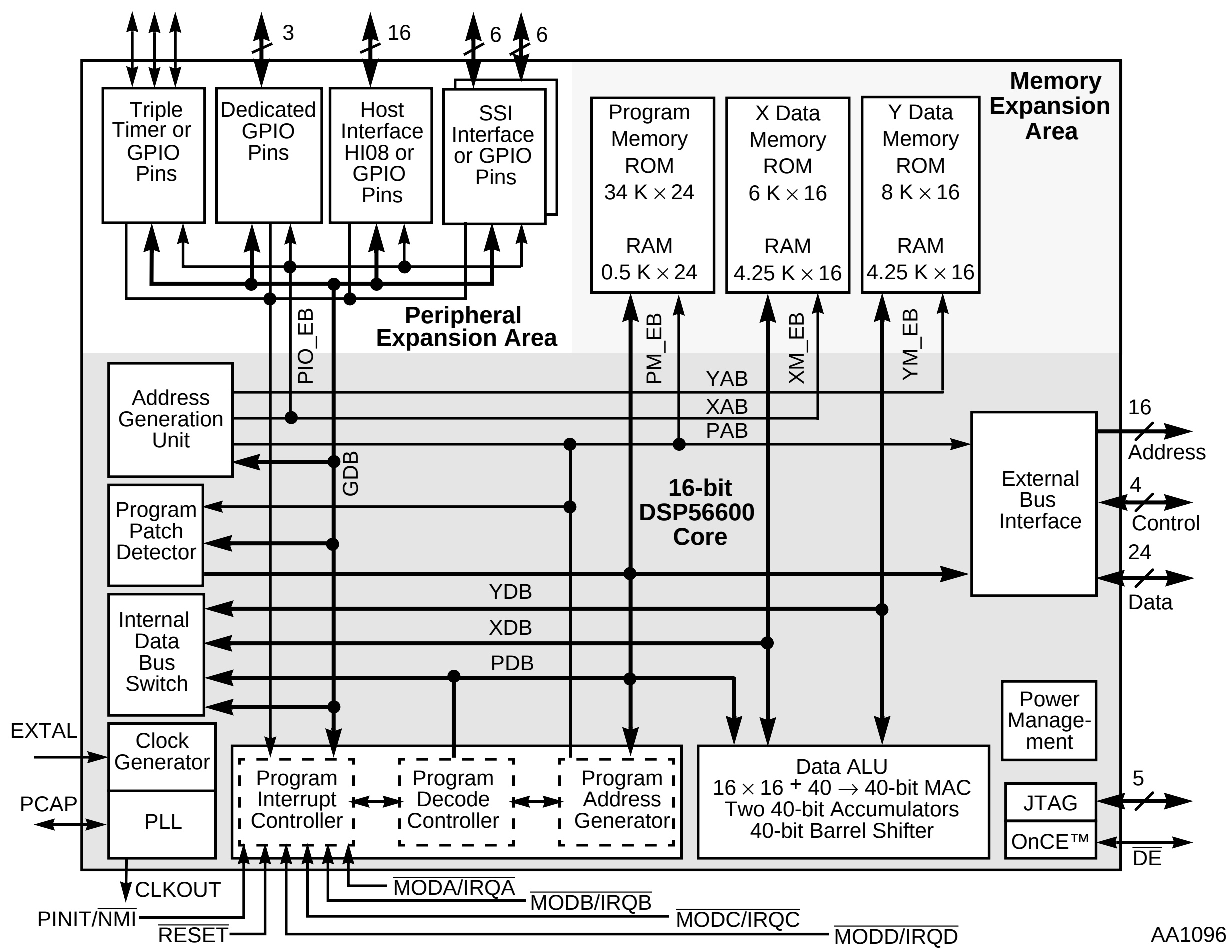

Figure 1 DSP56602 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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DATA SHEET CONVENTIONS

This data sheet uses the following conventions:

$\overline{\text{OVERBAR}}$	This is used to indicate a signal that is active when pulled low. For example, the $\overline{\text{RESET}}$ pin is active when low.
"asserted"	A high true (active high) signal is high or a low true (active low) signal is low.
"deasserted"	A high true (active high) signal is low or a low true (active low) signal is high.

Examples:

Signal/Symbol	Logic State	Signal State	Voltage[1]
$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
PIN	True	Asserted	V_{IH}/V_{OH}
PIN	False	Deasserted	V_{IL}/V_{OL}

Note: 1. Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

DSP56602 FEATURES

Digital Signal Processing Core

- High-performance DSP56600 core
- Up to 60 Million Instructions Per Second (MIPS) at 2.7–3.3 V
- Fully pipelined 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 40-bit accumulators including extension bits
- 40-bit parallel barrel shifter
- Highly parallel instruction set with unique DSP addressing modes
- Code-compatible with the DSP56300 core
- Position-independent code support
- User-selectable stack extension
- Nested hardware DO loops
- Fast auto-return interrupts
- On-chip support for software patching and enhancements
- On-chip Phase Lock Loop (PLL) circuit
- Real-time trace capability via external address bus
- On-Chip Emulation (OnCE) module and JTAG port

Memory

- 34 K × 24 of customer-specifiable factory-programmed Program ROM
- 0.5 K × 24 of Program RAM
- 10.25 K × 16 of X data memory, organized as follows:
  - 6 K × 16 of X data ROM
  - 4.25 K × 16 of X data RAM
- 12.25 K × 16 of Y data memory, organized as follows:
  - 8 K × 16 of Y data ROM
  - 4.25 K × 16 of Y data RAM
- Off-chip expansion for both program fetch and program data transfers
- No additional logic needed for interface to external SRAM memories

Peripheral Circuits

- Three dedicated General Purpose Input/Output (GPIO) pins and as many as thirty-one additional GPIO pins (user-selectable as peripherals or GPIO pins)
- Host Interface (HI08) support: one 8-bit parallel port (or as many as sixteen additional GPIO pins)
  - Direct interface to Motorola HC11, Hitachi H8, 8051 family, and Thomson P6 family
  - Minimal logic interface to standard ISA bus, Motorola 68K family, and Intel x86 microprocessor family.
- Synchronous Serial Interface (SSI) support: two 6-pin ports (or twelve additional GPIO pins)
  - Supports serial devices with one or more industry-standard codecs, other DSPs, microprocessors, and Motorola SPI-compliant peripherals
  - Independent transmitter and receiver sections and a common SSI clock generator
  - Network mode using frame sync and up to 32 time slots
  - 8-bit, 12-bit, and 16-bit data word lengths
- Three programmable timers (or as many as three additional GPIO pins)
- Three external interrupt/mode control lines
- One external reset pin for hardware reset

Energy Efficient Design

- Very low power CMOS design
  - Operating voltage range: 1.8 V to 3.3 V
  - < 0.85 mA/MIPS at 2.7 V
  - < 0.55 mA/MIPS at 1.8 V
- Low power Wait for interrupt standby mode, and ultra low power Stop standby mode
- Fully static, HCMOS design for operating frequencies from 60 MHz down to 0 Hz (dc)
- Special power management circuitry

PRODUCT DOCUMENTATION

The three documents listed in **Table 1** are required for a complete description of the DSP56602 and are necessary to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet (the source for the latest information).

Table 1 DSP56602 Chip Documentation

Document Name	Description of Contents	Order Number
DSP56600 Family Manual	Detailed description of the DSP56600 family architecture, and 16-bit DSP core processor and the instruction set	DSP56600FM/AD
DSP56602 User's Manual	Detailed description of memory, peripherals, and interfaces of the DSP56602	DSP56602UM/AD
DSP56602 Technical Data	Electrical and timing specifications, pin descriptions, and package descriptions	DSP56602/D

FOR THE LATEST INFORMATION

Refer to the back cover of this document for:

- Motorola contact addresses
- Motorola Mfax™ service
- Motorola DSP Internet address
- Motorola DSP Helpline

The Mfax service and the DSP Internet connection maintain the most current specifications, documents, and drawings. These two services are available on demand 24 hours a day.

SECTION 1

SIGNAL/CONNECTION DESCRIPTIONS

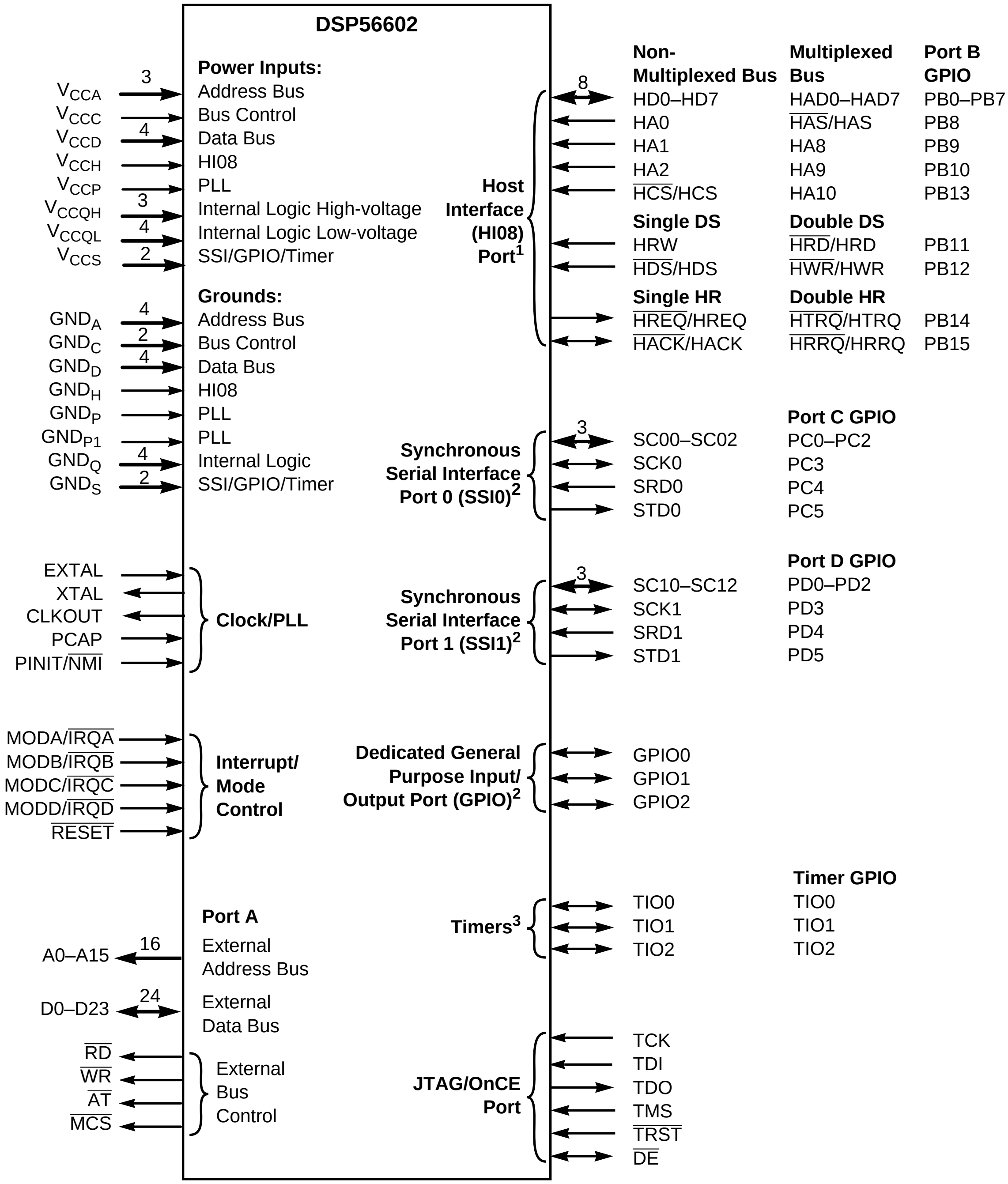
INTRODUCTION

The input and output signals of the DSP56602 are organized into functional groups, as shown in **Table 1-1** and as illustrated in **Figure 1-1**. In **Table 1-2** through **Table 1-12**, each table row describes the signal or signals present on a pin.

The DSP56602 is operated from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1-1 Functional Group Signal Allocations

Functional Group		**Number of Signals**	**Detailed Description**
Power (V_{CC})		19	**Table 1-2**
Ground (GND)		19	**Table 1-3**
PLL and Clock Signals		5	**Table 1-4**
Interrupt and Mode Control		5	**Table 1-5**
External Memory Port (also referred to as Port A)	Address Bus	16	**Table 1-6**
	Data Bus	24	
	Bus Control	4	
Host Interface (HI08)	Port B (GPIO)	16	**Table 1-7**
Synchronous Serial Interface 0 (SSI0)	Port C (GPIO)	6	**Table 1-8**
Synchronous Serial Interface 1 (SSI1)	Port D (GPIO)	6	**Table 1-9**
General Purpose Input/Output (GPIO)		3	**Table 1-10**
Triple Timer		3	**Table 1-11**
JTAG/On-Chip Emulation (OnCE) Module		6	**Table 1-12**



Note:
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double Data Strobe (DS), and single or double Host Request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. The HI08 signals can also be configured alternately as GPIO signals (PB0–PB15).
2. The SSI0 and SSI1 signals can be configured alternatively as Port C GPIO signals (PC0–PC5) and Port D GPIO signals (PD0–PD5), respectively.
3. TIO0–TIO2 can be configured alternatively as GPIO signals.

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Figure 1-1 DSP56602 Signals Identified by Functional Group

POWER

Table 1-2 Power Inputs

Signal Name (number of pins)	**Signal Description**
V_{CCA} (3)	**Address Bus Power—**V_{CCA} is an isolated power for sections of address bus I/O drivers, and must be tied externally to all other chip power inputs, except for the V_{CCQL} input. The user must provide adequate external decoupling capacitors.
V_{CCC} (1)	**Bus Control Power—**V_{CCC} is an isolated power for the bus control I/O drivers, and must be tied to all other chip power inputs externally, except for the V_{CCQL} input. The user must provide adequate external decoupling capacitors.
V_{CCD} (4)	**Data Bus Power—**V_{CCD} is an isolated power for sections of data bus I/O drivers, and must be tied to all other chip power inputs externally, except for the V_{CCQL} input. The user must provide adequate external decoupling capacitors.
V_{CCH} (1)	**Host Power—**V_{CCH} is an isolated power for the HI08 logic, and must be tied to all other chip power inputs externally, except for the V_{CCQL} input. The user must provide adequate external decoupling capacitors.
V_{CCP} (1)	**PLL Power—**V_{CCP} is V_{CC} dedicated for Phase Lock Loop (PLL) use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail.
V_{CCQH} (3)	**Quiet Power High-voltage—**V_{CCQH} is an isolated power for the CPU logic, and must be tied to all other chip power inputs externally, except for the V_{CCQL} input. The user must provide adequate external decoupling capacitors. The voltage supplied to these inputs should equal the voltage supplied to I/O power inputs V_{CCA}, V_{CCC}, V_{CCD}, V_{CCH}, and V_{CCS}.
V_{CCQL} (4)	**Quiet Power Low-voltage—**V_{CCQL} is an isolated power for the CPU logic, and should not be tied to the other chip power inputs. The user must provide adequate external decoupling capacitors.
V_{CCS} (2)	**SSIs, GPIO and Timers Power—**V_{CCS} is an isolated power for the SSIs, GPIO, and Timers logic, and must be tied to all other chip power inputs externally, except for the V_{CCQL} input. The user must provide adequate external decoupling capacitors.

GROUND

Table 1-3 Grounds

Signal Name (number of pins)	Signal Description
GND_A (4)	**Address Bus Ground—**GND_A is an isolated ground for sections of address bus I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_C (2)	**Bus Control Ground—**GND_C is an isolated ground for the bus control I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_D (4)	**Data Bus Ground—**GND_D is an isolated ground for sections of the data bus I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_H (1)	**Host Ground**—GND_H is an isolated ground for the HI08 I/O drivers, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_P (1)	**PLL Ground—**GND_P is ground dedicated for PLL use, and should be provided with an extremely low impedance path to ground. V_{CCP} should be bypassed to GND_P with a 0.1 µF capacitor located as close as possible to the chip package.
GND_{P1} (1)	**PLL Ground 1—**GND_{P1} is ground dedicated for PLL use, and should be provided with an extremely low impedance path to ground.
GND_Q (4)	**Quiet Ground—**GND_Q is an isolated ground for the CPU logic, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
GND_S (2)	**SSIs, GPIO, and Timers Ground**—GND_S is an isolated ground for the SSIs, GPIO, and Timers logic, and must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

CLOCK AND PHASE LOCK LOOP

Table 1-4 Clock and PLL Signals

Signal Name	Signal Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input—**EXTAL interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output—**XTAL connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.
PCAP	Input	Indeter-minate	**PLL Capacitor—**PCAP is an input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}. If the PLL is not used, PCAP may be tied to V_{CC}, GND, or left floating.
CLKOUT	Output	Chip-driven	**Clock Output—**CLKOUT provides an output clock synchronized to the internal core clock phase. When the PLL is enabled, the Division Factor (DF) equals one, and the Multiplication Factor (MF) is less than or equal to four, CLKOUT is also synchronized to EXTAL. When the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.
PINIT $\overline{NMI}$	Input Input	Input	**PLL Initialize—**During assertion of $\overline{RESET}$, the value of PINIT is written into the PLL Enable (PEN) bit of the PLL Control Register 1 (PCTL1) , determining whether the PLL is enabled or disabled. When this input is high during $\overline{RESET}$ assertion, the PLL is enabled following $\overline{RESET}$ deassertion. **Non-Maskable Interrupt—**After $\overline{RESET}$ deassertion and during normal instruction processing, the PINIT/$\overline{NMI}$ Schmitt-trigger input is a negative-edge-triggered Non-Maskable Interrupt (NMI) request internally synchronized to CLKOUT. This input can tolerate 5 V.

INTERRUPT AND MODE CONTROL

Table 1-5 Interrupt And Mode Control Signals

Signal Name	Signal Type	State During Reset	Signal Description
$\overline{\text{RESET}}$	Input	Input	**Reset—**$\overline{\text{RESET}}$ is an active low, Schmitt-trigger input. Deassertion of the $\overline{\text{RESET}}$ signal is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input, such as a capacitor charging, to reliably reset the chip. If the $\overline{\text{RESET}}$ signal is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start up synchronously and operate together. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. In addition, the value on the PINIT/$\overline{\text{NMI}}$ pin is latched to the PEN bit in the PCTL1 register. This input can tolerate 5 V.
MODA $\overline{\text{IRQA}}$	Input Input	Input	**Mode Select A—**During hardware reset, MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the Operating Mode Register (OMR) when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request A—**Following $\overline{\text{RESET}}$ deassertion, MODA becomes $\overline{\text{IRQA}}$, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If $\overline{\text{IRQA}}$ is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting $\overline{\text{IRQA}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQA}}$ is asserted, the processor exits the Stop state. This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.
MODB $\overline{\text{IRQB}}$	Input Input	Input	**Mode Select B—**During hardware reset, MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the Operating Mode Register (OMR) when the $\overline{\text{RESET}}$ signal is deasserted. **External Interrupt Request B—**Following $\overline{\text{RESET}}$ deassertion, MODB becomes $\overline{\text{IRQB}}$, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If $\overline{\text{IRQB}}$ is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting $\overline{\text{IRQB}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQB}}$ is asserted, the processor exits the Stop state. This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.

Table 1-5 Interrupt And Mode Control Signals (Continued)

Signal Name	Signal Type	State During Reset	Signal Description
MODC	Input	Input	**Mode Select C—**During hardware reset, MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the Operating Mode Register (OMR) when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQC}}$	Input		**External Interrupt Request C—**Following $\overline{\text{RESET}}$ deassertion, MODC becomes $\overline{\text{IRQC}}$, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If $\overline{\text{IRQC}}$ is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting $\overline{\text{IRQC}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQC}}$ is asserted, the processor exits the Stop state. This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.
MODD	Input	Input	**Mode Select D—**During hardware reset, MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes latched into the Operating Mode Register (OMR) when the $\overline{\text{RESET}}$ signal is deasserted.
$\overline{\text{IRQD}}$	Input		**External Interrupt Request—**Following $\overline{\text{RESET}}$ deassertion, MODD becomes $\overline{\text{IRQD}}$, a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If $\overline{\text{IRQD}}$ is asserted synchronous to CLKOUT, multiple processors can be resynchronized using the WAIT instruction and asserting $\overline{\text{IRQD}}$ to exit the Wait state. If the processor is in the Stop standby state and $\overline{\text{IRQD}}$ is asserted, the processor exits the Stop state. This is an active low Schmitt-trigger input, internally synchronized to CLKOUT. This input can tolerate 5 V.

EXTERNAL MEMORY INTERFACE (PORT A)

Table 1-6 External Memory Interface (Port A) Signals

Signal Name	Signal Type	State During Reset	Signal Description
A0–A15	Output	Set according to chip operating mode*	**Address Bus—**These active high outputs specify the address for external program memory accesses. To minimize power dissipation, A0–A15 do not change state when external memory spaces are not being accessed.
D0–D23	Bi-directional	Tri-stated	**Data Bus—**These active high, bidirectional input/outputs provide the bidirectional data bus for external program memory accesses. D0–D23 are tri-stated when no external bus activity occurs.
$\overline{\text{MCS}}$	Output	Pulled high internally	**Memory Chip Select—**This signal is an active low output, and is asserted when an external memory access occurs.
$\overline{\text{RD}}$	Output	Pulled high internally	**Read Enable—**This signal is an active low output. $\overline{\text{RD}}$ is asserted to read external memory on the data bus (D0–D23).
$\overline{\text{WR}}$	Output	Pulled high internally	**Write Enable—**This signal is an active low output. $\overline{\text{WR}}$ is asserted to write external memory on the data bus (D0–D23).
$\overline{\text{AT}}$	Output	Pulled high internally	**Address Tracing—**This signal is an active low output. $\overline{\text{AT}}$ is asserted (for half of a clock cycle) whenever a new address is driven on the address bus (A0–A15) in the Program Address Tracing mode. The new address is either a reflection of internal fetch or internal program space move instruction or an external address driven for an external access.
Note:	* The A0–A15 pins are asserted according to the selected chip operating mode, as determined by the values on the MODA–MODD pins. Each mode has a different reset address. A0–A15 are latched to the value of that reset address minus 1. For example, if the reset address for a selected operating mode is $0800, the address bus is asserted to $07FF.		

HOST INTERFACE (HI08)

The HI08 provides a fast parallel data to 8-bit port that can be connected directly to the host bus. The HI08 supports a variety of standard buses, and can be directly connected to a number of industry standard microcomputers, microprocessors, DSPs, and DMA hardware. The direction and polarity of all pins on the HI08 is programmable. All pins also have programmable GPIO functionality.

Table 1-7 Host Interface Signals

Signal Name	Signal Type	State During Reset	Signal Description
HD0–HD7	Bi-directional	Tri-stated	**Host Data Bus—**When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the Host Data bidirectional tri-state bus (HD0–HD7).
HAD0–HAD7	Bi-directional		**Host Address and Data Bus—**When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the Host Address/Data multiplexed bidirectional tri-state bus (HAD0–HAD7).
PB0–PB7	Input or Output		**Port B 0–7—**When the HI08 is configured as GPIO through the HI08 Port Control Register (HPCR), these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register (HDDR). When configured as an input, this pin can tolerate 5 V.
HA0	Input	Tri-stated	**Host Address Input 0—**When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line 0 of the Host Address input bus (HA0).
$\overline{\text{HAS}}$/HAS	Input		**Host Address Strobe—**When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is the Host Address Strobe ($\overline{\text{HAS}}$) Schmitt-trigger input. The polarity of the address strobe is programmable.
PB8	Input or Output		**Port B 8—**When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.

Table 1-7 Host Interface Signals (Continued)

Signal Name	Signal Type	State During Reset	Signal Description
HA1	Input	Tri-stated	**Host Address Input 1—**When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line one of the Host Address input bus (HA1).
HA8	Input		**Host Address 8—**When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line eight of the input Host Address bus (HA8).
PB9	Input or Output		**Port B 9—**When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.
HA2	Input	Tri-stated	**Host Address Input 2—**When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is line two of the Host Address input bus (HA2).
HA9	Input		**Host Address 9—**When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line nine of the input Host Address bus (HA9).
PB10	Input or Output		**Port B 10—**When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.

Table 1-7 Host Interface Signals (Continued)

Signal Name	Signal Type	State During Reset	Signal Description
HRW	Input	Tri-stated	**Host Read/Write—**When the HI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Read/$\overline{\text{Write}}$ input (HRW).
$\overline{\text{HRD}}$/HRD	Input		**Host Read Data—**When the HI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the Read Data strobe Schmitt-trigger input ($\overline{\text{HRD}}$). The polarity of the data strobe is programmable.
PB11	Input or Output		**Port B 11—**When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.
$\overline{\text{HDS}}$/HDS	Input	Tri-stated	**Host Data Strobe—**When the HI08 is programmed to interface a single-data-strobe host bus and the HI function is selected, this signal is the Host Data Strobe Schmitt-trigger input ($\overline{\text{HDS}}$). The polarity of the data strobe is programmable.
$\overline{\text{HWR}}$/HWR	Input		**Host Write Enable—**When the HI08 is programmed to interface a double-data-strobe host bus and the HI function is selected, this signal is the Write Data Strobe Schmitt-trigger input ($\overline{\text{HWR}}$). The polarity of the data strobe is programmable.
PB12	Input or Output		**Port B 12—**When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.

Table 1-7 Host Interface Signals (Continued)

Signal Name	Signal Type	State During Reset	Signal Description
$\overline{HCS}$/HCS	Input	Tri-stated	**Host Chip Select—**When the HI08 is programmed to interface a non-multiplexed host bus and the HI function is selected, this signal is the Host Chip Select input ($\overline{HCS}$). The polarity of the chip select is programmable.
HA10	Input		**Host Address 10—**When the HI08 is programmed to interface a multiplexed host bus and the HI function is selected, this signal is line 10 of the input Host Address bus (HA10).
PB13	Input or Output		**Port B 13—**When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.
$\overline{HREQ}$/ HREQ	Output	Tri-stated	**Host Request—**When the HI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the Host Request output ($\overline{HREQ}$). The polarity of the host request is programmable. The host request can be programmed as a driven or open-drain output.
$\overline{HTRQ}$ / HTRQ	Output		**Transmit Host Request—**When the HI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the Transmit Host Request output ($\overline{HTRQ}$). The polarity of the host request is programmable. The host request can be programmed as a driven or open-drain output.
PB14	Input or Output		**Port B 14—**When the HI08 is programmed to interface a multiplexed host bus and the signal is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.

Table 1-7 Host Interface Signals (Continued)

Signal Name	Signal Type	State During Reset	Signal Description
$\overline{HACK}$/ HACK	Input	Tri-stated	**Host Acknowledge—**When the HI08 is programmed to interface a single host request host bus and the HI function is selected, this signal is the Host Acknowledge Schmitt-trigger input ($\overline{HACK}$). The polarity of the host acknowledge is programmable.
$\overline{HRRQ}$ / HRRQ	Output		**Receive Host Request—**When the HI08 is programmed to interface a double host request host bus and the HI function is selected, this signal is the Receive Host Request output ($\overline{HRRQ}$). The polarity of the host request is programmable. The host request can be programmed as a driven or open-drain output.
PB15	Input or Output		**Port B 15—**When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed as an input or output through the HDDR. When configured as an input, this pin can tolerate 5 V.

SYNCHRONOUS SERIAL INTERFACE 0 (SSI0)

Two identical Synchronous Serial Interfaces (SSI0 and SSI1) provide a full-duplex serial port for serial communication with a variety of serial devices including one or more industry-standard codecs, other DSPs, or microprocessors. When either SSI port is disabled, it can be used for General Purpose I/O (GPIO).

Table 1-8 Synchronous Serial Interface 0 (SSI0)

Signal Name	Signal Type	State During Reset	Signal Description
SC00 PC0	Input or Output Input or Output	Tri-stated	**Serial Control Signal 0—**The function of SC00 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for or for Serial I/O Flag 0. **Port C 0—**When configured as PC0, signal direction is controlled through the SSI0 Port Direction Control Register (PRRC). The signal can be configured as SSI signal SC00 through the SSI0 Port Control Register (PCRC). When configured as an input, this pin can tolerate 5 V.
SC01 PC1	Input or Output Input or Output	Tri-stated	**Serial Control Signal 1—**The function of SC00 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for Serial I/O Flag 1. **Port C 1—**When configured as PC1, signal direction is controlled through the PRRC. The signal can be configured as an SSI signal SC01 through the PCRC. When configured as an input, this pin can tolerate 5 V.

Table 1-8 Synchronous Serial Interface 0 (SSI0) (Continued)

Signal Name	Signal Type	State During Reset	Signal Description
SC02	Input or Output	Tri-stated	**Serial Control Signal 2—**SC02 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2—**When configured as PC2, signal direction is controlled through the PRRC. The signal can be configured as an SSI signal SC02 through the PCRC. When configured as an input, this pin can tolerate 5 V.
SCK0	Input or Output	Tri-stated	**Serial Clock—**SCK0 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the SSI. The SCK0 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (i.e., the system clock frequency must be at least three times the external SSI clock frequency). The SSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3—**When configured as PC3, signal direction is controlled through the PRRC. The signal can be configured as an SSI signal SCK0 through the PCRC. When configured as an input, this pin can tolerate 5 V.
SRD0	Input	Tri-stated	**Serial Receive Data—**SRD0 receives serial data and transfers the data to the SSI Receive Shift Register.
PC4	Input or Output		**Port C 4—**When configured as PC4, signal direction is controlled through the PRRC. The signal can be configured as an SSI signal SRD0 through the PCRC. When configured as an input, this pin can tolerate 5 V.

Table 1-8 Synchronous Serial Interface 0 (SSI0) (Continued)

Signal Name	Signal Type	State During Reset	Signal Description
STD0	Output	Tri-stated	**Serial Transmit Data—**STD0 is used for transmitting data from the SSI Transmit Shift Register.
PC5	Input or Output		**Port C 5—**When configured as PC5, signal direction is controlled through the PRRC. The signal can be configured as an SSI signal STD0 through the PCRC. When configured as an input, this pin can tolerate 5 V.

SYNCHRONOUS SERIAL INTERFACE 1 (SSI1)

Table 1-9 Synchronous Serial Interface 1 (SSI1)

Signal Name	Signal Type	State during Reset	Signal Description
SC10	Input or Output	Tri-stated	**Serial Control Signal 0—**The function of SC10 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for or for Serial I/O Flag 0.
PD0	Input or Output		**Port D 0—**When configured as PD0, signal direction is controlled through the SSI1 Port Direction Control Register (PRRD). The signal can be configured as SSI signal SC10 through the SSI1 Port Control Register (PCRD). When configured as an input, this pin can tolerate 5 V.
SC11	Input or Output	Tri-stated	**Serial Control Signal 1—**The function of SC11 is determined by the selection of either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is used for Serial I/O Flag 1.
PD1	Input or Output		**Port D 1—**When configured as PD1, signal direction is controlled through the PRRD. The signal can be configured as an SSI signal SC11 through the PCRD. When configured as an input, this pin can tolerate 5 V.
SC12	Input or Output	Tri-stated	**Serial Control Signal 2—**SC12 is used for frame sync I/O. SC12 is the frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PD2	Input or Output		**Port D 2—**When configured as PD2, signal direction is controlled through the PRRD. The signal can be configured as an SSI signal SC12 through the PCRD. When configured as an input, this pin can tolerate 5 V.

Table 1-9 Synchronous Serial Interface 1 (SSI1) (Continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCK1	Input or Output	Tri-stated	**Serial Clock—**SCK1 is a bidirectional Schmitt-trigger input signal providing the serial bit rate clock for the SSI. The SCK1 is a clock input or output used by both the transmitter and receiver in Synchronous modes, or by the transmitter in Asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (i.e., the system clock frequency must be at least three times the external SSI clock frequency). The SSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3—**When configured as PD3, signal direction is controlled through the PRRD. The signal can be configured as an SSI signal SCK1 through the PCRD. When configured as an input, this pin can tolerate 5 V.
SRD1	Input	Tri-stated	**Serial Receive Data—**SRD1 receives serial data and transfers the data to the SSI Receive Shift Register.
PD4	Input or Output		**Port D 4—**When configured as PD4, signal direction is controlled through the PRRD. The signal can be configured as an SSI signal SRD1 through the PCRD. When configured as an input, this pin can tolerate 5 V.
STD1	Output	Tri-stated	**Serial Transmit Data—**STD1 is used for transmitting data from the SSI Transmit Shift Register.
PD5	Input or Output		**Port D 5—**When configured as PD5, signal direction is controlled through the PRRD. The signal can be configured as an SSI signal STD1 through the PCRD. When configured as an input, this pin can tolerate 5 V.

GENERAL PURPOSE I/O (GPIO)

Three dedicated General Purpose Input/Output (GPIO) signals are provided on the DSP56602. Each is reconfigurable as input, output, or tri-state. These signals are exclusively defined as GPIO, and do not offer additional functionality.

Table 1-10 General Purpose I/O (GPIO)

Signal Name	Signal Type	State during Reset	Signal Description
GPIO0	Input or Output	Input	**General Purpose I/O**—When a GPIO signal is used as input, the logic state is reflected to an internal register and can be read by the software. When a GPIO signal is used as output, the logic state is controlled by the software. This input can tolerate 5 V.
GPIO1	Input or Output	Input	**General Purpose I/O**—When a GPIO signal is used as input, the logic state is reflected to an internal register and can be read by the software. When a GPIO signal is used as output, the logic state is controlled by the software. This input can tolerate 5 V.
GPIO2	Input or Output	Input	**General Purpose I/O**—When a GPIO signal is used as input, the logic state is reflected to an internal register and can be read by the software. When a GPIO signal is used as output, the logic state is controlled by the software. This input can tolerate 5 V.

TRIPLE TIMER

Three identical and independent timers are implemented. The three timers can use internal or external clocking and can interrupt the DSP after a specified number of events (clocks), or can signal an external device after counting a specific number of internal events. When a timer port is disabled, it can be used for General Purpose I/O (GPIO).

Table 1-11 Triple Timer Signals

Signal Name	Signal Type	State during Reset	Signal Description
TIO0	Input or Output	GPIO Input	**Timer 0 Schmitt-Trigger Input/Output—**When TIO0 is used as an input, the timer module functions as an external event counter or measures external pulse width or signal period. When TIO0 is used as an output, the timer module functions as a timer and TIO0 provides the timer pulse.
	Input or Output		When the TIO0 is not used by the timer module, it can be used for GPIO.
			When configured as an input, this pin can tolerate 5 V.
TIO1	Input or Output	GPIO Input	**Timer 1 Schmitt-Trigger Input/Output—**When TIO1 is used as an input, the timer module functions as an external event counter or measures external pulse width or signal period. When TIO1 is used as an output, the timer module functions as a timer and TIO1 provides the timer pulse.
	Input or Output		When TIO1 is not used by the timer module, it can be used for GPIO.
			When configured as an input, this pin can tolerate 5 V.
TIO2	Input or Output	GPIO Input	**Timer 2 Schmitt-Trigger Input/Output—**When TIO2 is used as an input, the timer module functions as an external event counter or measures external pulse width or signal period. When TIO2 is used as an output, the timer module functions as a timer and TIO2 provides the timer pulse.
	Input or Output		When TIO2 is not used by the timer module, it can be used for GPIO.
			When configured as an input, this pin can tolerate 5 V.

JTAG/OnCE INTERFACE

Table 1-12 JTAG/On-Chip Emulation (OnCE) Interface Signals

Signal Name	Signal Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock—**TCK is a test clock input signal used to synchronize the JTAG test logic. The TCK pin can be tri-stated. This input can tolerate 5 V.
TDI	Input	Input	**Test Data Input—**TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of the TCK signal and has an internal pull-up resistor. This input can tolerate 5 V.
TDO	Output	Tri-state	**Test Data Output—**TDO is a test data serial output signal used for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of the TCK signal.
TMS	Input	Input	**Test Mode Select—**TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of the TCK signal and has an internal pull-up resistor. This input can tolerate 5 V.
$\overline{TRST}$	Input	Input	**Test Reset—**$\overline{TRST}$ is an active-low Schmitt-trigger input signal used to asynchronously initialize the test controller. $\overline{TRST}$ has an internal pull-up resistor. $\overline{TRST}$ must be asserted during the power up sequence. This input can tolerate 5 V.
$\overline{DE}$	Bi-directional	Input	**Debug Event—**$\overline{DE}$ is an open-drain bidirectional active-low signal providing, as an input, a means of entering the Debug mode of operation from an external command controller, and as an output, a means of acknowledging that the chip has entered the Debug mode. The $\overline{DE}$ has an internal pull-up resistor. When this pin is an input, it can tolerate 5 V.

Preliminary

SECTION 2

SPECIFICATIONS

GENERAL CHARACTERISTICS

The DSP56602 is fabricated in high-density CMOS with Transistor-Transistor Logic (TTL)-compatible inputs and outputs.

Functional operating conditions are given in **Table 2-4** on page 2-3. Absolute maximum ratings given in **Table 2-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The DSP56602 dc/ac electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

Table 2-1 Absolute Maximum Ratings (GND = 0 V)

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	–0.3 to +4	V
All input voltages excluding "5 Volt Tolerant" inputs	V_{IN}	GND – 0.3 to V_{CC} + 0.3	V
All "5 Volt Tolerant" input voltages*	V_{IN5}	GND – 0.3 to V_{CC} + 3.95	V
Current drain per pin excluding V_{CC} and GND	I	10	mA
Operating temperature range	T_A	–40 to 85	˚C
Storage temperature	T_{stg}	–55 to +150	˚C
Note: * "5 Volt Tolerant" inputs are inputs that tolerate 5 V. All "5 Volt Tolerant" input voltages can not be more than 3.95 V greater than supply voltage. This restriction applies to power-on, as well as to normal operation. .			

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either or V_{CC} or GND).

Table 2-2 Recommended Operating Conditions

Rating	Symbol	Value	Unit
Supply voltage	V_{CC}	2.7 to 3.3	V
Ambient temperature	T_A	–40 to +85	°C

Table 2-3 Package Thermal Characteristics

Characteristic	Symbol	TQFP Value	PBGA[3] Value	PBGA[4] Value	Units
Junction-to-ambient thermal resistance[1]	$R_{\theta JA}$ or θ_{JA}	49	73	35	°C/W
Junction-to-case thermal resistance[2]	$R_{\theta JC}$ or θ_{JC}	8.2	—	—	°C/W
Thermal characterization parameter	Ψ_{JT}	5.5	5	—	°C/W

Notes:
1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided Printed Circuit Board per SEMI G38-87 in natural convection.(SEMI is Semiconductor Equipment and Materials International, 805 East Middlefield Rd., Mountain View, CA 94043, (415) 964-5111.)
2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
3. These are simulated values. Test board has 2-ounce copper traces routed to the outer row of balls.
4. These are simulated values. The test board has two, 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

Table 2-4 DC Electrical Characteristics for the DSP56602

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage for V_{CCA}, V_{CCC}, V_{CCD}, V_{CCH}, V_{CCP}, V_{CCQH}, V_{CCQL}, and V_{CCS}[1]	V_{CC}	2.7	3.0	3.3	V
Input high voltage • D0–D23 • MOD/$\overline{\text{IRQ}}$[2], $\overline{\text{RESET}}$, PINIT/$\overline{\text{NMI}}$, and all JTAG/HI08/SSI/Timer/GPIO pins • EXTAL	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 V_{CC} – 0.4	 — — —	 V_{CC} 5.75 V_{CC}	 V V V
Input low voltage • D0–D23, MOD/$\overline{\text{IRQ}}$[2], $\overline{\text{RESET}}$, PINIT/$\overline{\text{NMI}}$ • All JTAG/HI08/SSI/Timer/GPIO pins • EXTAL	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 0.4	 V V V
Input leakage current	I_{IN}	–10.0	—	10.0	µA
High-impedance (off-state) input current (2.4 V/0.4 V)	I_{TSI}	–10.0	—	10.0	µA
Output high voltage (I_{OH} = –0.4 mA)	V_{OH}	2.4	—	—	V
Output low voltage (I_{OL} = 3.0 mA, open drain pins I_{OL} = 6.7 mA)	V_{OL}	—	—	0.4	V
Internal supply current at 60 MHz • In Normal mode[3, 6] • In Wait mode[4, 6] • In Stop mode[5, 6]	 I_{CCI} I_{CCW} I_{CCS}	 — — —	 57 4.6 50	 — — —	 mA mA µA
PLL supply current in Stop mode (PLL on)[6]	I_{PLL}	—	3.5	—	mA
Input capacitance[6]	C_{IN}	—	—	10	pF

Notes:
1. Throughout the data sheet, assume that V_{CCA}, V_{CCC}, V_{CCD}, V_{CCH}, V_{CCP}, V_{CCQH}, V_{CCQL}, and V_{CCS} power pins have the same voltage level.
2. This specification applies to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
3. **Power Consumption Considerations** on page 4-4 provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CC} = 2.7 V at T_J = 100°C. The actual current consumption varies with the operating conditions and the program being executed.
4. In order to obtain these results, all inputs must be terminated (i.e., not allowed to float).
5. In order to obtain these results, all inputs that are not disconnected at Stop mode must be terminated.
6. These values are periodically sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS

The timing specifications in **AC Electrical Characteristics** are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels set forth in **DC Electrical Characteristics**. AC timing specifications referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. Timings specified relative to a CLKOUT edge are measured with respect to the 50% point of the applicable CLKOUT transition. All other DSP56602 output timing specifications are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V, respectively.

Note: Unless specifically noted otherwise, all references to CLKOUT edges assume that the PLL is enabled. All timings except those that specifically relate to the EXTAL input are guaranteed by test with the PLL enabled.

AC Electrical Characteristics—Internal Clock Operation

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

For each occurrence of T_H, T_L, T_C, or I_{CYC}, substitute the numbers given in **Table 2-5**. (The terms Ef, ET_H, ET_L, and ET_C are described in **Table 2-6**.)

Table 2-5 Internal Clocks

Characteristics	Symbol	Expression
Internal operation frequency with PLL enabled[1, 2, 3]	f	$(Ef \times MF)/(PDF \times D^3)$
Internal operation frequency with PLL disabled	f	Ef/2
Internal clock high period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_H	ET_C (Min) $0.49 \times ET_C \times PDF \times DF/MF$ (Max) $0.51 \times ET_C \times PDF \times DF/MF$ (Min) $0.47 \times ET_C \times PDF \times DF/MF$ (Max) $0.53 \times ET_C \times PDF \times DF/MF$

Table 2-5 Internal Clocks (Continued)

Characteristics	Symbol	Expression
Internal clock low period • With PLL disabled • With PLL enabled and MF ≤ 4 • With PLL enabled and MF > 4	T_L	ET_C (Min) $0.49 \times ET_C \times PDF \times DF/MF$ (Max) $0.51 \times ET_C \times PDF \times DF/MF$ (Min) $0.47 \times ET_C \times PDF \times DF/MF$ (Max) $0.53 \times ET_C \times PDF \times DF/MF$
Internal clock cycle time with PLL enabled	T_C	$ET_C \times PDF \times DF/MF$
Internal clock cycle time with PLL disabled	T_C	$2 \times ET_C$
Instruction cycle time	I_{CYC}	T_C
Notes: 1. MF represents the PLL Multiplication Factor. 2. PDF represents the PLL Predivision Factor. 3. DF represents the PLL Division Factor.		

AC Electrical Characteristics—External Clock Operation

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85˚C, C_L = 50 pF + 2 TTL Loads)

The DSP56602 system clock can be derived from the on-chip crystal oscillator, or it can be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically not connected to the board or socket (see **Figure 2-2** on page 2-7). The rise and fall time of this external clock should be 3 ns maximum

Table 2-6 Clock Operation

Num	Characteristics	Symbol	Min	Max
1	Frequency of EXTAL (EXTAL pin frequency)	Ef	0	60.0 MHz
2	Clock input high[1, 2] • PLL disabled (46.7–53.3% duty cycle) • PLL enabled (42.5–57.5% duty cycle, at 60 MHz)	ET_H	 7.8 ns 7.1 ns	 ∞ 157.0 µs
3	Clock input low[1, 2] • PLL disabled (46.7–53.3% duty cycle) • PLL enabled (42.5–57.5% duty cycle)	ET_L	 7.8 ns 7.1 ns	 ∞ 157.0 µs

Table 2-6 Clock Operation (Continued)

Num	Characteristics	Symbol	Min	Max
4	Clock cycle time [2] • With PLL disabled • With PLL enabled	ET_C	 16.7 ns 16.7 ns	 ∞ 273.1 µs
5	CLKOUT change from EXTAL Fall, PLL disabled	—	4.3ns	11.0 ns
6	CLKOUT from EXTAL with PLL enabled (MF = PDF × DF, MF ≤ 4, Ef > 15 MHz)[4]	—	0	1.8 ns
7	Instruction cycle time = $I_{CYC} = T_C$ [1, 3] • With PLL disabled • With PLL enabled	I_{CYC}	 33.3 ns 16.7 ns	 ∞ 8.53 µs

Notes:
1. External Clock Input High, External Clock Input Low, and CLKOUT are measured at 50% of the signal transition.
2. The maximum value for PLL enabled is given for minimum VCO and maximum MF.
3. The maximum value for PLL enabled is given for minimum VCO and maximum DF.
4. These timings are periodically sampled and not 100% tested.

Fundamental Frequency Fork Crystal Oscillator

Suggested Component Values:

f_{OSC} = 32.768 kHz
R1 = 3.9 MΩ ± 10%
R2 = 200 kΩ ± 10%
C = 22 pF ± 20%

Calculations were done for a 32.768 kHz crystal with the following parameters:
a load capacitance (C_L) of 12.5 pF,
a shunt capacitance (C_0) of 1.8 pF,
a series resistance of 40 kΩ, and
a drive level of 1 µW.

Fundamental Frequency Crystal Oscillator

Suggested Component Values:

f_{OSC} = 4 MHz	f_{OSC} = 20 MHz
R = 680 kΩ ± 10%	R = 680 kΩ ± 10%
C = 56 pF ± 20%	C = 22 pF ± 20%

Calculations were done for a 4/20 MHz crystal with the following parameters:
a load capacitance C_L of 30/20 pF,
a shunt capacitance C_0 of 7/6 pF,
a series resistance of 100/20 Ω, and
a drive level of 2 mW.

AA1071

Figure 2-1 Crystal Oscillator Circuits

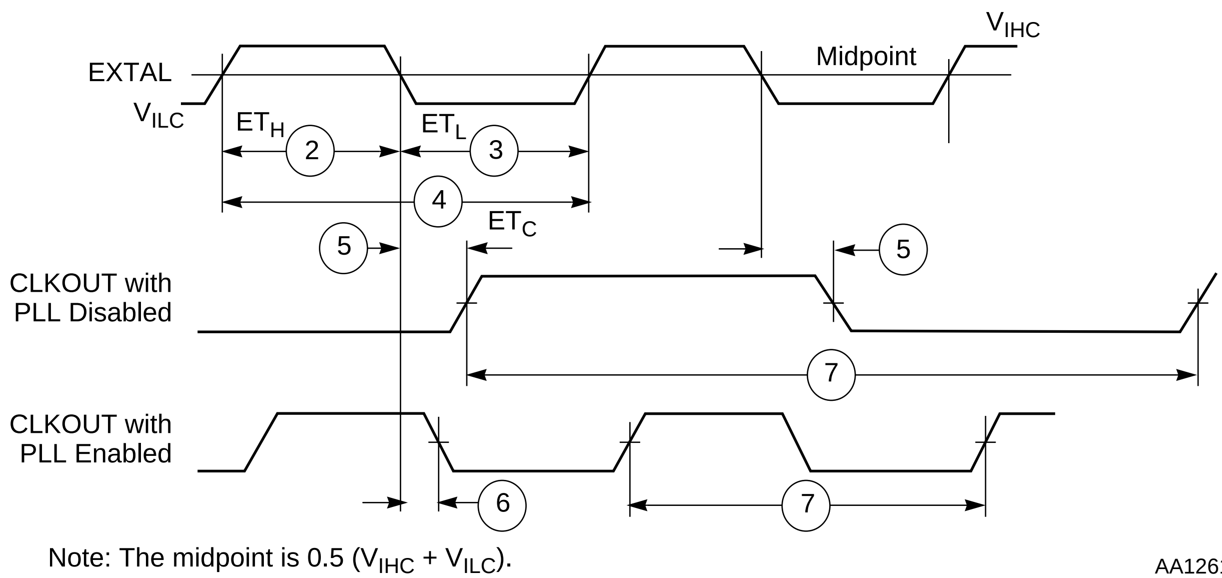


Figure 2-2 External Clock Timing

AC Electrical Characteristics—Phase Lock Loop (PLL) Characteristics

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85° C, C_L = 50 pF + 2 TTL Loads)

Table 2-7 Phase Lock Loop Characteristics

Characteristics	Expression	Min	Max	Unit
VCO frequency when PLL enabled [1]	MF × Ef × 2 / PDF	30	120	MHz
PLL external capacitor (PCAP pin to V_{CCP}) • MF ≤ 4 • MF > 4	Cpcap [2]	 MF × 425 – 125 MF × 520	 MF × 590 – 175 MF × 920	 pF pF

Notes: 1. The VCO output is further divided by 2 when PLL is enabled. If the Division Factor (DF) is 1, the operating frequency is $\frac{VCO}{2}$.

2. Cpcap is the value of the PLL capacitor (connected between PCAP pin and V_{CCP}). (The recommended value for Cpcap is (500 × MF – 150) pF for MF ≤ 4 and (690 × MF) pF for MF > 4.)

AC Electrical Characteristics—Reset, Stop, Mode Select, and Interrupt Timing

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

WS = Number of Wait States (measured in clock cycles, number of T_C)

Table 2-8 Reset Timing

Num	Characteristics	Expression	60 MHz		Unit
			Min	Max	
8	Delay from $\overline{RESET}$ assertion to all pins at reset value[1]	20.0 + T_C	—	333.34	ns
9	Required $\overline{RESET}$ duration [2, 3] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled • Power on, internal oscillator • During Stop, XTAL disabled • During Stop, XTAL enabled • During normal operation	 $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$	 833.3 16.72 1.25 1.25 41.7 41.7	 — — — — — —	 ns µs µs ms ns ns
10	Delay from asynchronous $\overline{RESET}$ deassertion to first external address output (internal reset deassertion)[4] • Minimum • Maximum	 $3.25 \times T_C + 2.2$ $20.25T_C + 12.1$	 56.4 —	 — 349.6	 ns ns
11	Synchronous reset setup time from $\overline{RESET}$ deassertion to first CLKOUT transition	T_C	9.0	16.7	ns
12	Synchronous reset deassertion, delay time from the first CLKOUT transition to the first external address output • Minimum • Maximum	 $3.25 \times T_C + 1.1$ $20.25T_C + 5.5$	 55.3 —	 — 343.0	 ns ns

Notes:
1. These timings are periodically sampled and not 100% tested.
2. For an external clock generator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid. For internal oscillator, $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
3. When V_{CC} is powered up and the “Required $\overline{RESET}$ Duration” conditions as specified above are not yet met, the device circuitry is in an uninitialized state that may result in significant power consumption. Designs should minimize this state to the shortest possible duration.
4. This specification is valid if the PLL does not lose lock.

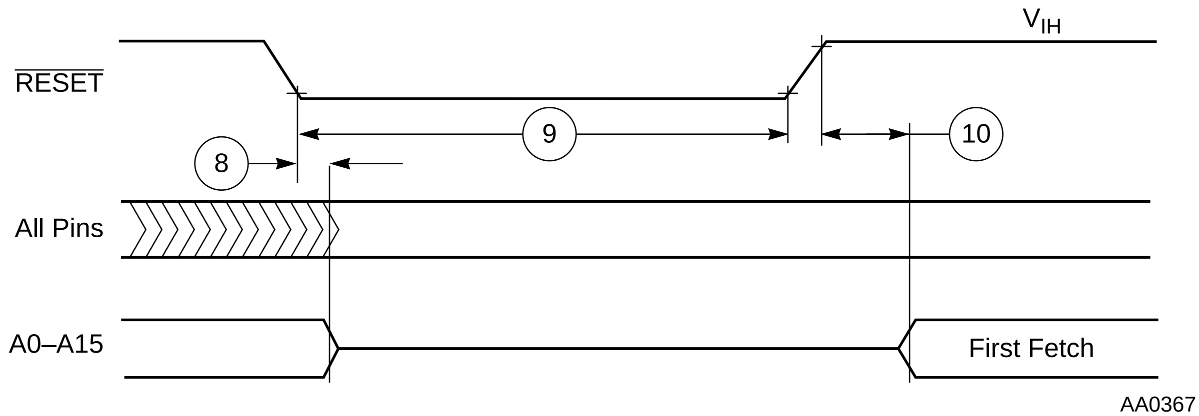


Figure 2-3 Reset Timing

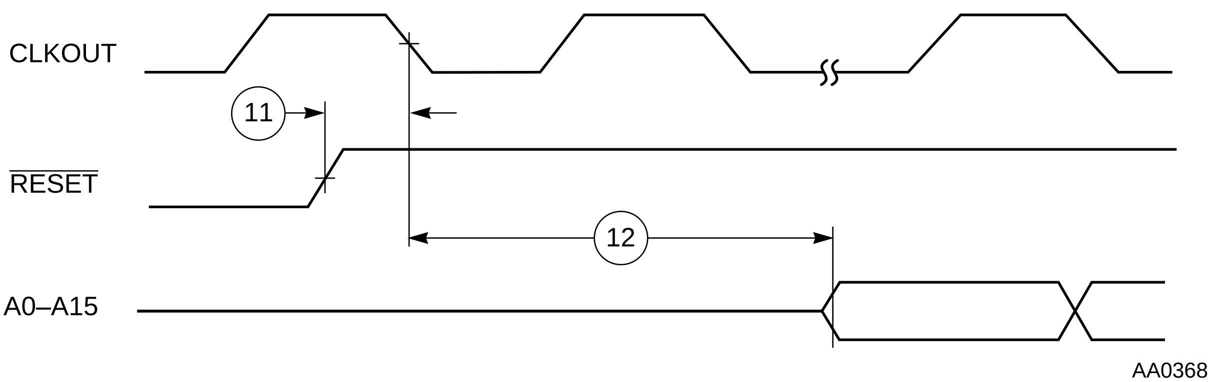


Figure 2-4 Synchronous Reset Timing

Table 2-9 Mode Select and Interrupt Timings

Num	Characteristics	Expression	60 MHz		Unit
			Min	Max	
13	Mode select setup time	—	30.0	—	ns
14	Mode select hold time	—	0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width	—	10.0	—	ns
16	Minimum edge-triggered interrupt request deassertion width	—	10.0	—	ns

Table 2-9 Mode Select and Interrupt Timings (Continued)

Num	Characteristics	Expression	60 MHz		Unit
			Min	Max	
17	Delay from $\overline{IRQ}$ or $\overline{NMI}$ assertion to external memory access address out valid • Caused by first interrupt instruction fetch • Caused by first interrupt instruction execution	 $4.25 \times T_C + 2.2$ $7.25 \times T_C + 2.2$	 73.0 123.0	 — —	 ns ns
18	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to general purpose transfer output valid caused by first interrupt instruction execution	$10 \times T_C + 5.5$	172.2	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level-sensitive fast interrupts[1]	$3.75 \times T_C +$ $WS \times T_C - 15.4$	—	63.8	ns
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level-sensitive fast interrupts[1]	$3.25 \times T_C +$ $WS \times T_C - 15.4$	—	55.4	ns
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level-sensitive fast interrupts[1] • SRAM WS = 1 • SRAM WS = 2, 3 • SRAM WS ≥ 4	 $(3.5 + WS) \times T_C - 15.4$ $(3.0 + WS) \times T_C - 15.4$ $(2.5 + WS) \times T_C - 15.4$	 — — —	 59.6 51.3 26.3	 ns ns ns
22	Synchronous interrupt setup time from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to the second CLKOUT transition	T_C	9.0	16.7	ns
23	Synchronous interrupt delay time from CLKOUT's second transition to the first external address output valid caused by the first instruction fetch after coming out of Wait • Minimum • Maximum	 $9.25 \times T_C + 1.1$ $24.75 \times T_C + 5.5$	 155.3 —	 — 418.0	 ns ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop	—	9.0	—	ns

Table 2-9 Mode Select and Interrupt Timings (Continued)

Num	Characteristics	Expression	60 MHz		Unit
			Min	Max	
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop) [2, 3]				
	• PLL not active during Stop and Stop Delay enabled (PCTL1 Bit 6 = 0, OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	2.2	22.6	ms
	• PLL not active during Stop, Stop Delay not enabled (PCTL1 Bit 6 = 0, OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (23.75 \pm 0.5) \times T_C$	388.3 ns	20.4 ms	
	• PLL active during Stop, no Stop Delay (PCTL1 Bit 6 = 1)	$PLC \times ET_C$ $(8.25 \pm 0.5) \times T_C$	129.2	145.8	ns
26	Duration of level-sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop) [2,3]				
	• PLL not active during Stop, Stop Delay enabled (PCTL1 Bit 6 = 0, OMR Bit 6 = 0)	$PLC \times ET_C \times PDF + (128K - PLC/2) \times T_C$	22.6	—	ns
	• PLL not active during Stop, Stop Delay not enabled (PCTL1 Bit 6 = 0, OMR Bit 6 = 1)	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$	20.4	—	ns
	• PLL active during Stop, no Stop Delay (PCTL1 Bit 6 = 1)	$5.5 \times T_C$	91.7	—	ns
27	Interrupt requests rate				
	• HI08, SSI, Timer	$12T_C$	—	200.4	ns
	• $\overline{IRQ}$ (edge trigger)	$8T_C$	—	133.6	ns
	• $\overline{IRQ}$ (level trigger)	$12T_C$	—	200.4	ns

Table 2-9 Mode Select and Interrupt Timings (Continued)

Num	Characteristics	Expression	60 MHz		Unit
			Min	Max	

Notes:
1. When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, then timings 14 through 16 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. This timing depends on several settings:
   - For PLL disabled, using internal oscillator (PLL Control Register 1 (PCTL1) Bit 4 = 0) and oscillator disabled during Stop (PCTL1 Bit 5 = 0), a stabilization delay is required to assure the oscillator is stable before executing programs. In that case, resetting the Stop delay (Operating Mode Register (OMR) Bit 6 = 0) provides the proper delay. While it is possible to set OMR Bit 6 = 1, it is not recommended and these specifications do not guarantee timings for that case.
   - For PLL disabled, using internal oscillator (PCTL1 Bit 4 = 0) and oscillator enabled during Stop (PCTL1 Bit 5 = 1), no stabilization delay is required and recovery time is minimal (OMR Bit 6 setting is ignored).
   - For PLL disabled, using external clock (PCTL1 Bit 4 = 1), no stabilization delay is required and recovery time is defined by the PCTL1 Bit 6 and OMR Bit 6 settings.
   - For PLL disabled, using external clock (PCTL1 Bit 4 = 1), no stabilization delay is required and recovery time is defined by the PCTL1 Bit 6 and OMR Bit 6 settings.
   - For PLL enabled, if PCTL1 Bit 6 is 0, the PLL is shut down during Stop. Recovering from Stop requires the PLL to re-lock. The PLL lock procedure duration, PLC (PLL Lock Cycles), may be in the range of 0 to 300 cycles. This procedure occurs in parallel to the Stop Delay counter, and Stop recovery ends when the last of these two events occurs (the Stop Delay counter completes its count, or the PLL lock procedure completes).
   - PLC value for PLL disabled is 0.
   - Maximum value for ET_C is 4096 (maximum multiplication factor) divided by the desired internal frequency (i.e., for 60 MHz it is 4096/60 MHz = 68.26 μs). During the stabilization period, T_C, T_H, and T_L will not be constant. Their width may vary, so timing may vary as well.
3. These timings are periodically sampled and not 100% tested.

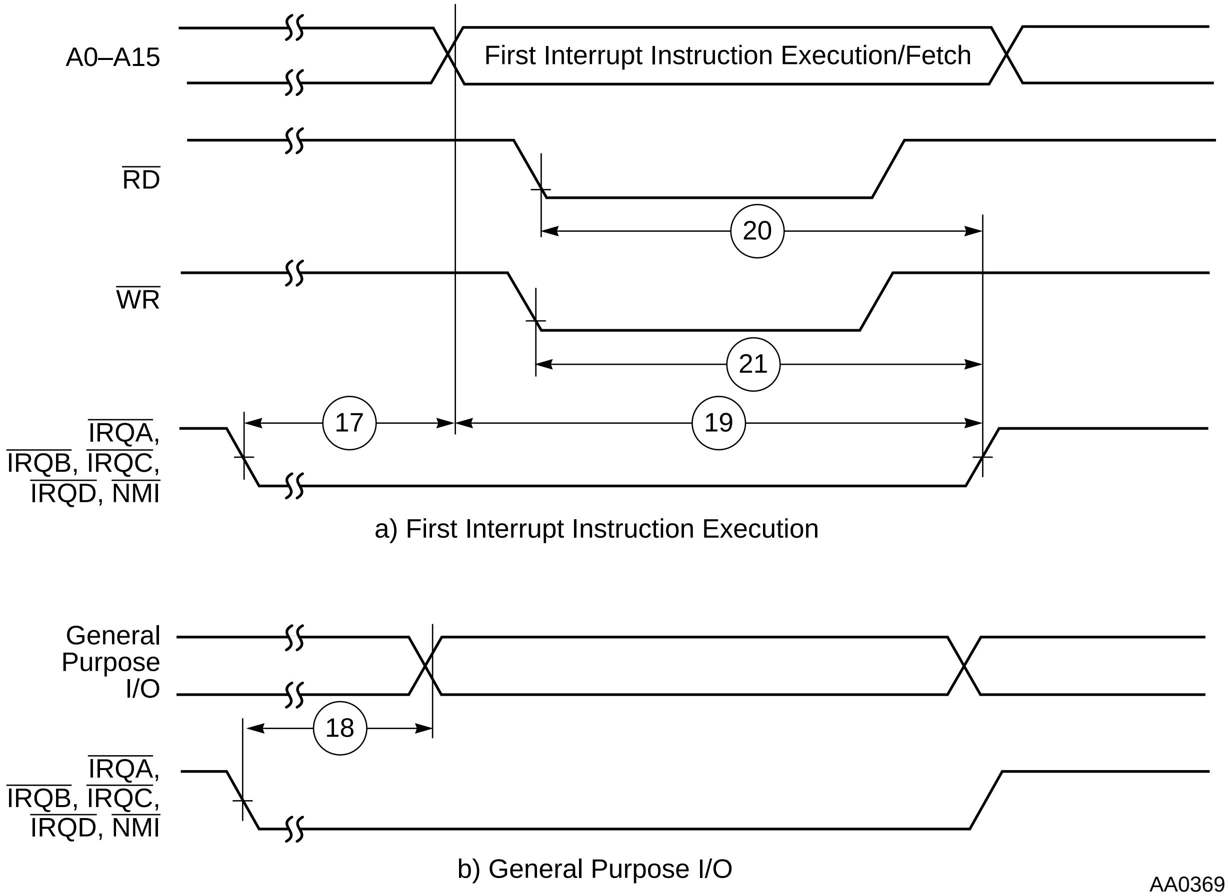


Figure 2-5 External Level-Sensitive Fast Interrupt Timing

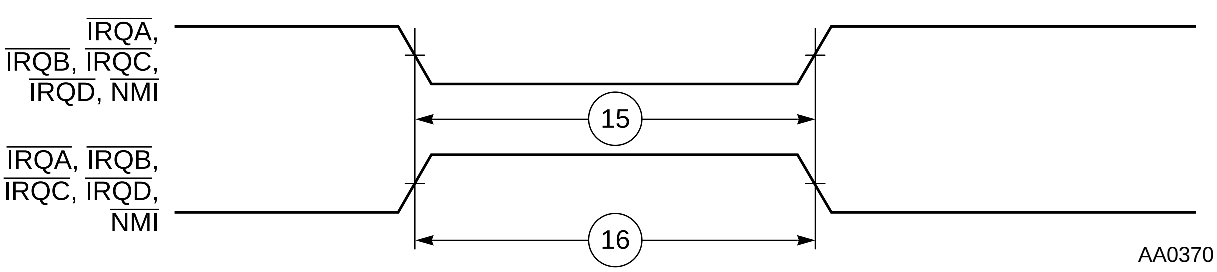


Figure 2-6 External Interrupt Timing (Negative-Edge-Triggered)

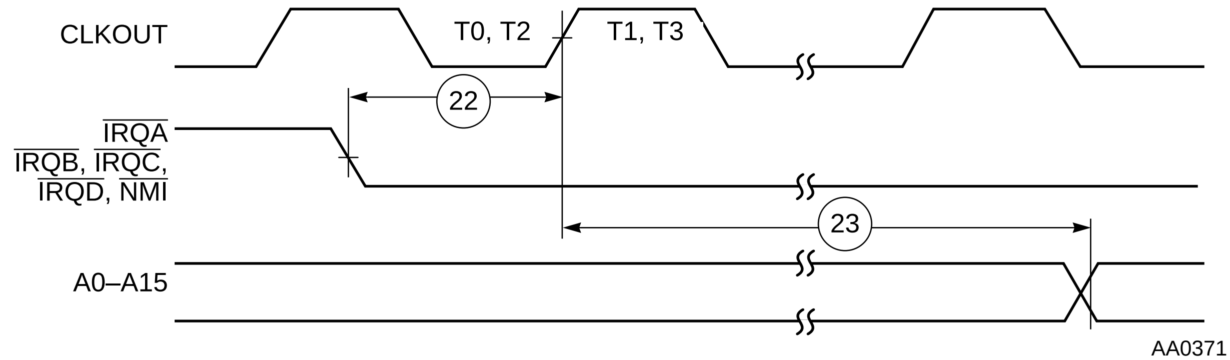


Figure 2-7 Synchronous Interrupt from Wait Timing

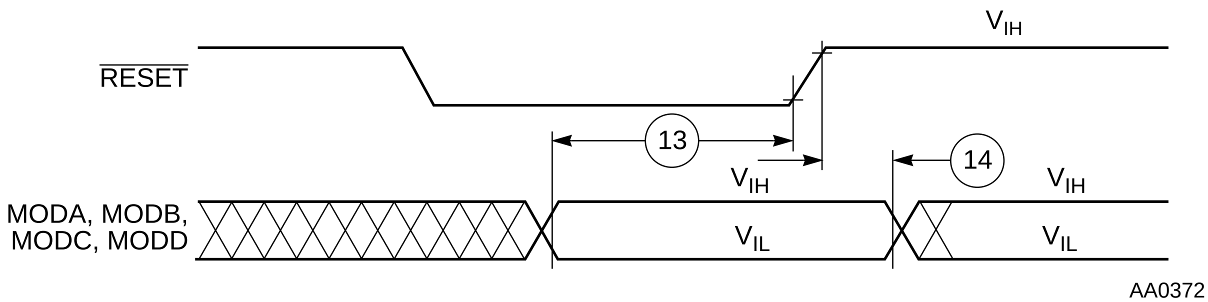


Figure 2-8 Operating Mode Select Timing

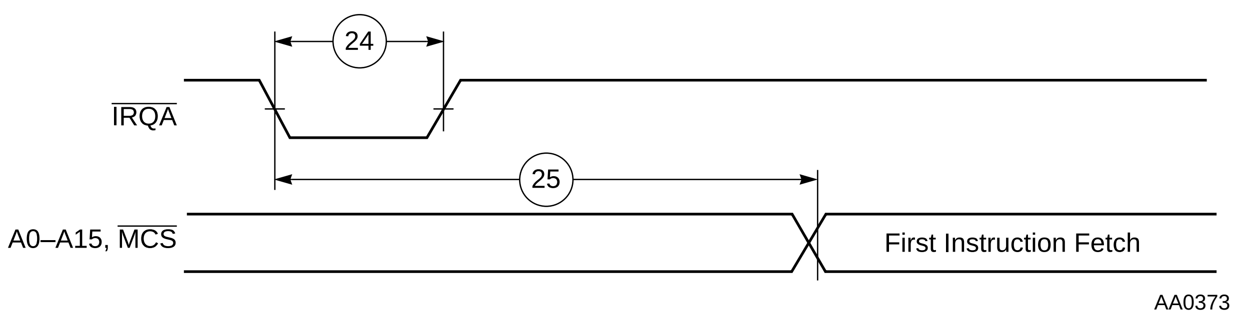


Figure 2-9 Recovery from Stop Using $\overline{\text{IRQA}}$

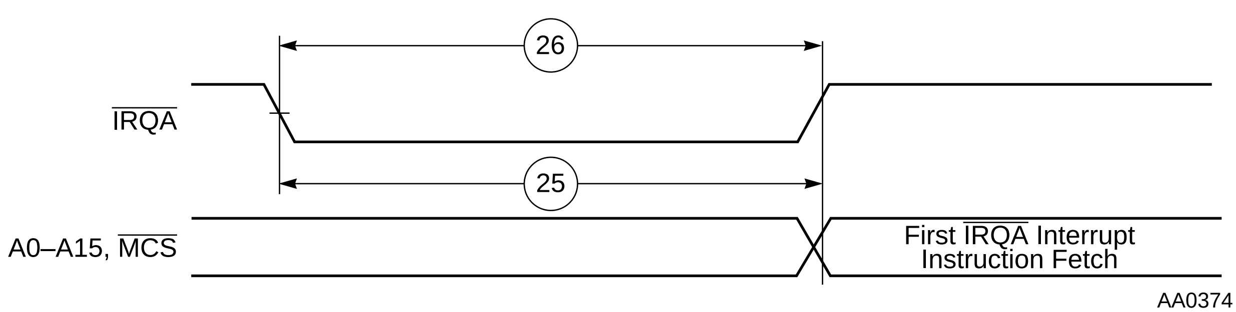


Figure 2-10 Recovery from Stop Using $\overline{\text{IRQA}}$ Interrupt Service

Preliminary

AC Electrical Characteristics—Port A

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

Table 2-10 SRAM Read and Write Access

Num	Characteristics	Symbol	Expression	60 MHz		Unit
				Min	Max	
100	Address valid and $\overline{MCS}$ assertion pulse width • 1 ≤ WS ≤ 3 • 4 ≤ WS ≤ 7 • WS ≥ 8	t_{RC}, t_{WC}	 (WS + 1) × T_C – 4.4 (WS + 2) × T_C – 4.4 (WS + 3) × T_C – 4.4	 28.9 95.6 178.9	 — — —	 ns ns ns
101	Address valid and $\overline{MCS}$ assertion to $\overline{WR}$ assertion • WS = 1 • 2 ≤ WS ≤ 3 • WS ≥ 4	t_{AS}	 0.25 × T_C – 3.7 0.75 × T_C – 4.4 1.25 × T_C – 4.4	 0.5 8.1 16.4	 — — —	 ns
102	$\overline{WR}$ assertion pulse width • WS = 1 • 2 ≤ WS ≤ 3 • WS ≥ 4	t_{WP}	 1.5 × T_C – 5.7 WS × T_C – 4.4 (WS – 0.5) × T_C – 4.4	 19.3 28.9 53.9	 — — —	 ns ns ns
103	$\overline{WR}$ deassertion to address invalid and $\overline{MCS}$ deassertion • 1 ≤ WS ≤ 3 • 4 ≤ WS ≤ 7 • WS ≥ 8	t_{WR}	 0.25 × T_C – 3.8 1.25 × T_C – 4.4 2.25 × T_C – 4.4	 0.4 16.4 33.1	 — — —	 ns ns ns
104	Address and $\overline{MCS}$ valid to input data valid, WS ≥ 1	t_{AA}, t_{AC}	(WS + 0.75) × T_C – 8.5	—	20.7	ns
105	$\overline{RD}$ assertion to input data valid, WS ≥ 1	t_{OE}	(WS + 0.5) × T_C – 8.5	—	16.5	ns
106	$\overline{RD}$ deassertion to data invalid (data hold time)	t_{OHZ}	—	0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion, WS ≥ 1	t_{AW}	(WS + 0.75) × T_C – 4.4	24.8	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time), WS ≥ 1	t_{DS} (t_{DW})	(WS – 0.25) × T_C – 3.9	8.6	—	ns

Table 2-10 SRAM Read and Write Access (Continued)

Num	Characteristics	Symbol	Expression	60 MHz		Unit
				Min	Max	
109	Data hold time from $\overline{WR}$ deassertion • $1 \le WS \le 3$ • $4 \le WS \le 7$ • $WS \ge 8$	t_{DH}	 $0.25 \times T_C - 3.8$ $1.25 \times T_C - 3.8$ $2.25 \times T_C - 3.8$	 0.4 17.0 33.7	 — — —	 ns ns ns
110	$\overline{WR}$ assertion to data active • $WS = 1$ • $2 \le WS \le 3$ • $WS \ge 4$	—	 $0.75 \times T_C - 3.7$ $0.25 \times T_C - 3.7$ $-0.25 \times T_C - 3.7$	 8.8 0.5 –7.9	 — — —	 ns ns ns
111	$\overline{WR}$ deassertion to data high impedance • $1 \le WS \le 3$ • $4 \le WS \le 7$ • $WS \ge 8$	—	 $0.25 \times T_C + 0.6$ $1.25 \times T_C + 0.6$ $2.25 \times T_C + 0.6$	 — — —	 4.8 21.4 38.1	 ns ns ns
112	Previous $\overline{RD}$ deassertion to data active (write) • $1 \le WS \le 3$ • $4 \le WS \le 7$ • $WS \ge 8$	—	 $1.25 \times T_C - 4.4$ $2.25 \times T_C - 4.4$ $3.25 \times T_C - 4.4$	 16.4 33.1 49.8	 — — —	 ns ns ns
113	$\overline{RD}$ deassertion time • $1 \le WS \le 3$ • $4 \le WS \le 7$ • $WS \ge 8$	—	 $0.75 \times T_C - 4.4$ $1.75 \times T_C - 4.4$ $2.75 \times T_C - 4.4$	 8.1 24.8 41.4	 — — —	 ns
114	$\overline{WR}$ deassertion time • $WS = 1$ • $2 \le WS \le 3$ • $4 \le WS \le 7$ • $WS \ge 8$	—	 $0.5 \times T_C - 3.1$ $T_C - 3.1$ $2.5 \times T_C - 3.1$ $3.5 \times T_C - 3.1$	 5.2 13.6 38.6 55.2	 — — — —	 ns ns ns ns
115	Address valid to $\overline{RD}$ assertion	—	$0.5 \times T_C - 4.0$	4.3	—	ns
116	$\overline{RD}$ assertion pulse width	—	$(WS + 0.25) \times T_C - 3.8$	17.0	—	ns
117	$\overline{RD}$ deassertion to address invalid • $1 \le WS \le 3$ • $4 \le WS \le 7$ • $WS \ge 8$	—	 $0.25 \times T_C - 3.0$ $1.25 \times T_C - 3.0$ $2.25 \times T_C - 3.0$	 1.2 17.8 34.5	 — — —	 ns ns ns

Table 2-10 SRAM Read and Write Access (Continued)

Num	Characteristics	Symbol	Expression	60 MHz		Unit
				Min	Max	

Notes: 1. WS refers to the number of Wait States, as specified in the Bus Control Register (BCR).
2. The asynchronous delays specified in the expressions are valid for DSP56602-60.
3. The Address Trace ($\overline{AT}$) pin is also active on accesses to internal program memory if the Address Trace Enable (ATE) bit (Bit 15) of the OMR is set. In this case, the $\overline{MCS}$, $\overline{RD}$, and $\overline{WR}$ signals are deasserted and the data bus is tri-stated while the address bus is driven with the address of the internal access.

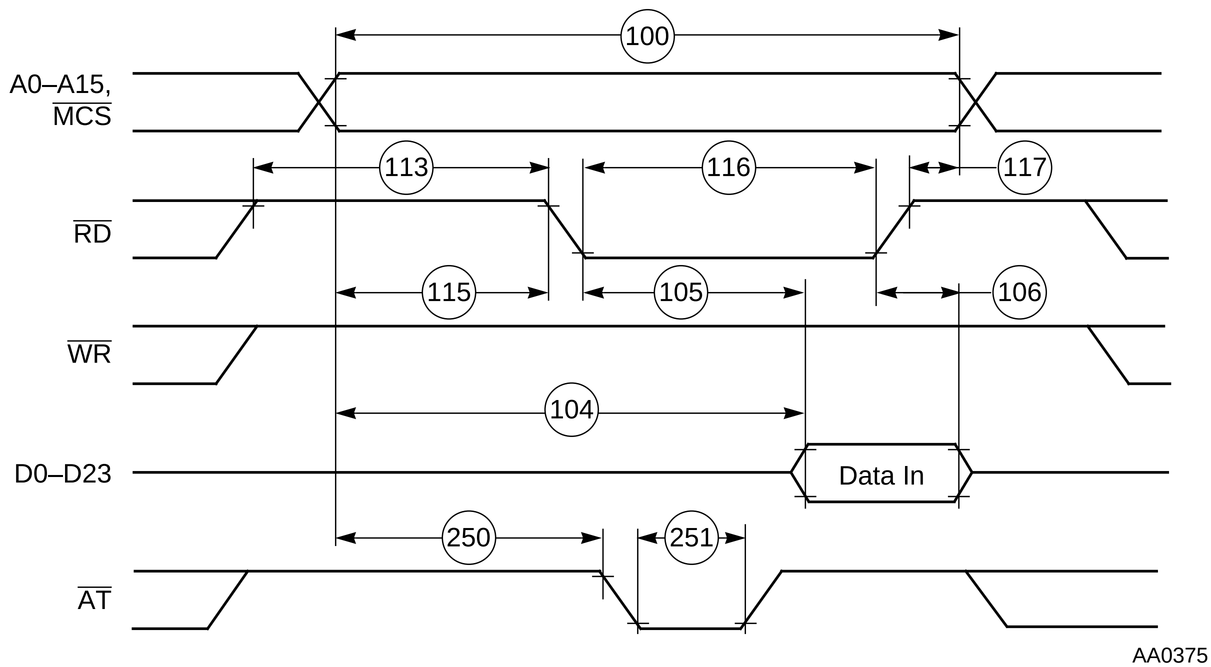


Figure 2-11 SRAM Read Access

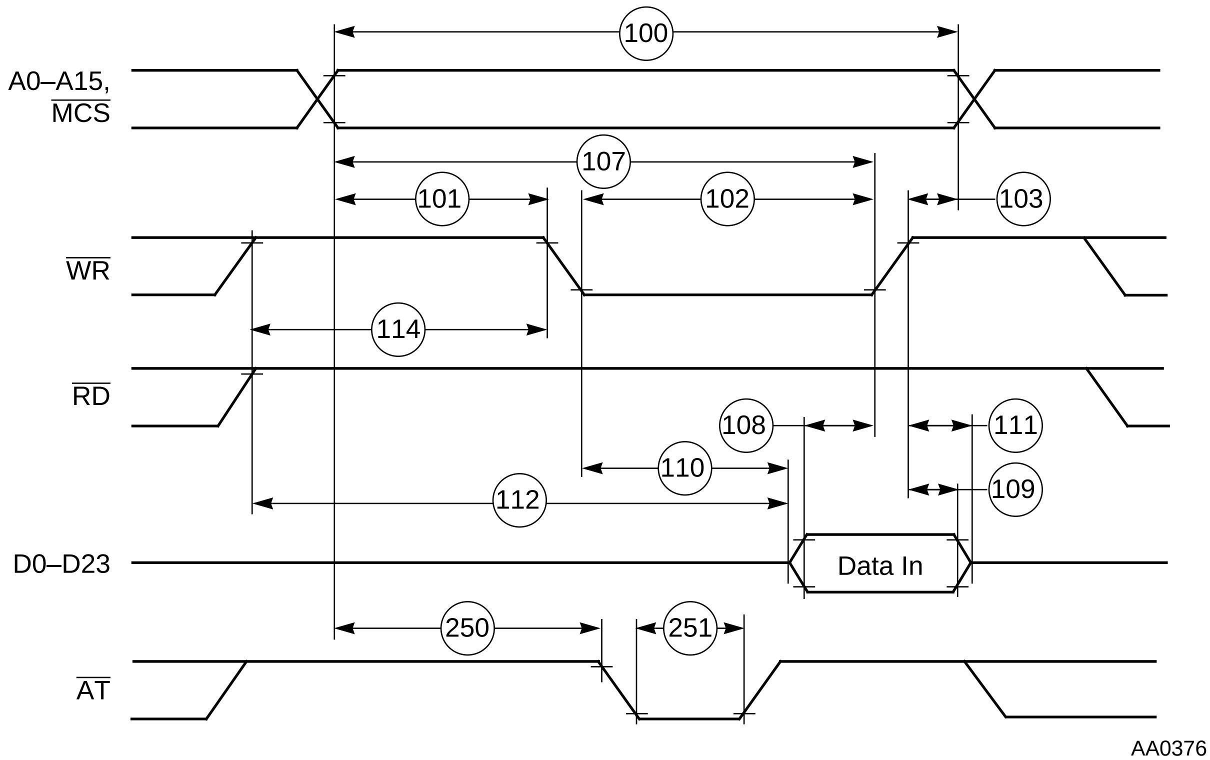


Figure 2-12 SRAM Write Access

Table 2-11 External Bus Synchronous Timings (SRAM Access)[1]

Num	Characteristics	Expression[2]	60 MHz		Unit
			Min	Max	
198	CLKOUT low to address valid and $\overline{MCS}$ assertion	$0.25 \times T_C + 5.5$	—	9.7	ns
199	CLKOUT low to address invalid and $\overline{MCS}$ deassertion	$0.25 \times T_C$	4.2	—	ns
202	CLKOUT low to data out active[3]	$0.25 \times T_C$	4.2	—	ns
203	CLKOUT low to data out valid	$0.25 \times T_C + 5.5$	—	9.7	ns
204	CLKOUT low to data out invalid	$0.25 \times T_C$	4.2	—	ns
205	CLKOUT low to data out high impedance[3]	$0.25 \times T_C + 1.1$	—	5.3	ns
206	Data in valid to CLKOUT low (setup)	—	3.0	—	ns
207	CLKOUT low to data in invalid (hold)	—	0.0	—	ns

Table 2-11 External Bus Synchronous Timings (SRAM Access)[1] (Continued)

Num	Characteristics	Expression[2]	60 MHz		Unit
			Min	Max	
208	CLKOUT low to $\overline{\text{RD}}$ assertion • Minimum • Maximum	 $0.5 \times T_C + 1.1$ $0.5 \times T_C + 5.5$	 9.4 —	 — 13.8	 ns ns
209	CLKOUT low to $\overline{\text{RD}}$ deassertion	—	0.0	5.5	ns
210	CLKOUT low to $\overline{\text{WR}}$ assertion[4,5] • WS = 1 • $2 \le WS \le 3$ • $WS \ge 4$	 $0.5 \times T_C + 6.2$ — $0.5 \times T_C + 6.2$	 10.1 1.8 10.1	 14.5 6.2 14.5	 ns ns ns
211	CLKOUT low to $\overline{\text{WR}}$ deassertion	—	0.0	4.9	ns

Notes:
1. "External Bus Synchronous Timings" should be used only for reference to the clock and **not** for relative timings.
2. The asynchronous delays specified in the expressions are valid for DSP56602-60.
3. These timings are periodically sampled and are not 100% tested.
4. WS is the number of Wait States specified in the BCR.
5. If WS > 1, $\overline{\text{WR}}$ assertion refers to the next rising edge of CLKOUT.

Table 2-12 Address Trace Timings (Synchronous and Asynchronous)

Num	Characteristics	Expression	60 MHz		Unit
			Min	Max	
250	Address setup time to $\overline{\text{AT}}$ assertion	$0.5 \times T_C - 4.4$	3.9	—	ns
251	$\overline{\text{AT}}$ pulse width*	$0.5 \times T_C - 4.4$	3.9	—	ns
252	CLKOUT low to $\overline{\text{AT}}$ assertion	$0.75 \times T_C + 5.5$	18.0	—	ns
253	CLKOUT low to $\overline{\text{AT}}$ deassertion • Minimum • Maximum	 $0.25 \times T_C + 1.1$ $0.25 \times T_C + 5.5$	 5.3 —	 — 9.7	 ns ns

Note: * The Address Trace ($\overline{\text{AT}}$) pin is also active on accesses to internal program memory if the Address Trace Enable (ATE) bit (Bit 15) of the OMR is set. In this case, the $\overline{\text{MCS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$ signals are deasserted and the data bus is tri-stated while the address bus is driven with the address of the internal access.

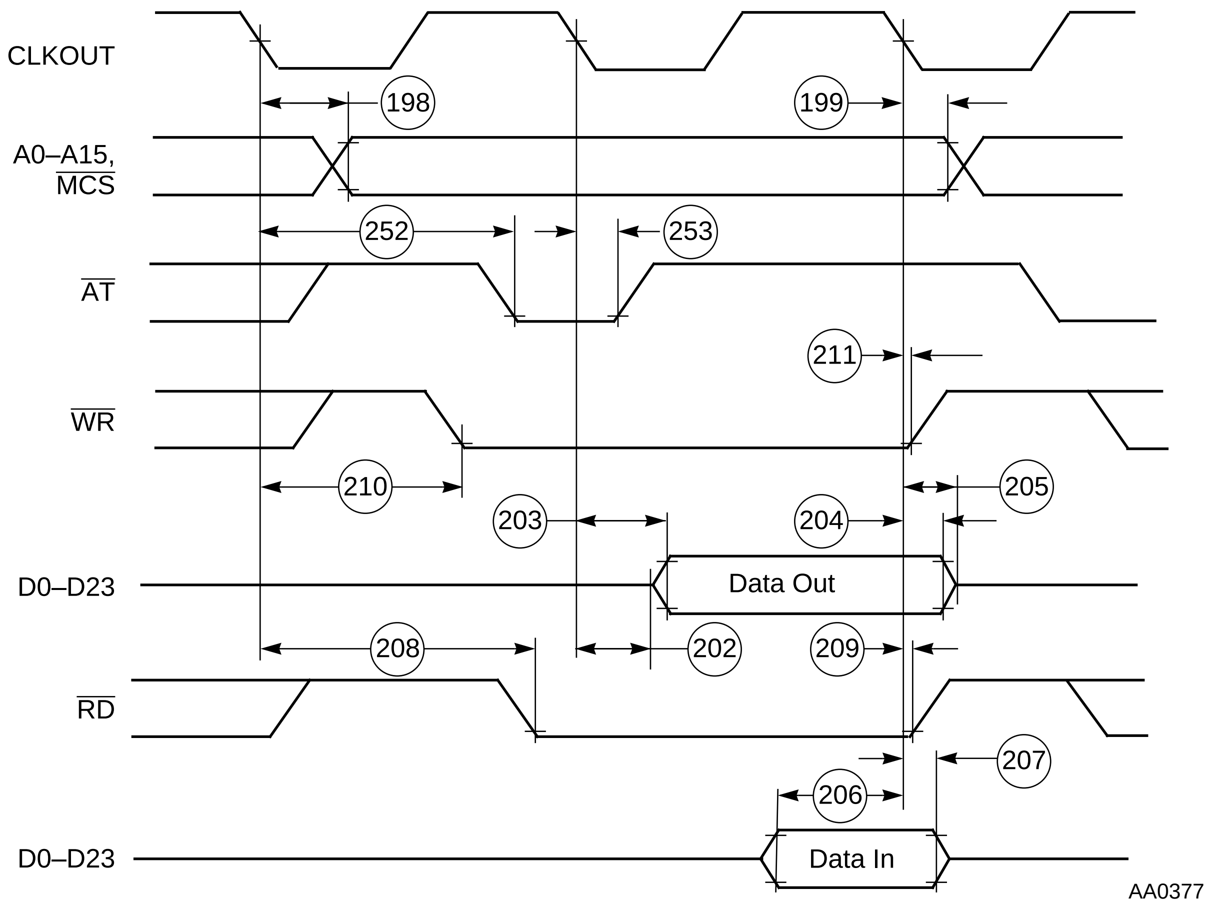


Figure 2-13 Synchronous Bus Timings SRAM 1 WS

AC Electrical Characteristics—Host Interface (HI08) Timing

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

Host Port Usage Considerations

Careful synchronization is required when reading multi-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the Host port. The considerations for proper operation are discussed below.

1. **Asynchronous Reading of Receive Byte Registers**—When reading the receive byte registers, RXH or RXL, the Host programmer should use

interrupts or poll the RXDF flag, which indicates that data is available. This assures that the data in the receive byte registers will be valid.

2. **Overwriting Transmit Byte Registers**—The Host programmer should not write to the transmit byte registers, TXH or TXL, unless the TXDE bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers can transfer valid data to the HRX register.
3. **Overwriting the Host Vector—**The Host Vector register should be changed only when the Host Command bit (HC) is clear. This guarantees that the DSP56602 interrupt control logic can receive a stable vector.

Table 2-13 Host Interface Timing[1, 2]

Num	Characteristic	Symbol	Expression	60 MHz		Unit
				Min	Max	
301	Read data strobe assertion width[3] $\overline{\text{HACK}}$ assertion width	—	T_C + 16.5	33.2		ns
302	Read data strobe deassertion width[3] $\overline{\text{HACK}}$ deassertion width	—	—	16.5	—	ns
303	Read data strobe deassertion width between two consecutive “Last Data Register” reads, two consecutive CVR reads, two consecutive ICR reads, or two consecutive ISR reads[3, 4, 5]	—	$2.5 \times T_C + 11.0$	52.7	—	ns
304	Write data strobe assertion width[6]	—	—	22.0	—	ns
305	Write data strobe deassertion width[6]	—	$2.5 \times T_C + 11.0$	52.7	—	ns
306	$\overline{\text{HAS}}$ assertion width	—	—	16.5	—	ns
307	$\overline{\text{HAS}}$ deassertion to data strobe assertion[7]	—	—	0	—	ns
308	Host data input setup time before write data strobe deassertion[6]	—	—	16.5	—	ns
309	Host data input hold time after write data strobe deassertion[6]	—	—	5.5	—	ns
310	Read data strobe assertion to output data active from high impedance[3, 8] $\overline{\text{HACK}}$ assertion to output data active from high impedance [8]	—	—	5.0	—	ns
311	Read data strobe assertion to output data valid[3] $\overline{\text{HACK}}$ assertion to output data valid	—	—	—	33.0	ns

Table 2-13 Host Interface Timing[1, 2] (Continued)

Num	Characteristic	Symbol	Expression	60 MHz Min	60 MHz Max	Unit
312	Read data strobe deassertion to output data high impedance[3, 8] $\overline{\text{HACK}}$ deassertion to output data high impedance [8]	—	—	—	16.5	ns
313	Output data hold time after read data strobe deassertion[3] Output data hold time after $\overline{\text{HACK}}$ deassertion	—	—	5.5	—	ns
314	$\overline{\text{HCS}}$ assertion to read data strobe deassertion	—	$T_C + 16.5$	33.2	—	ns
315	$\overline{\text{HCS}}$ assertion to write data strobe deassertion[6]	—	—	16.5	—	ns
316	$\overline{\text{HCS}}$ assertion to output data valid	—	—	—	27.5	ns
317	$\overline{\text{HCS}}$ hold time after data strobe deassertion[6, 7]	—	—	0	—	ns
318	Address (HAD0–HAD7) setup time before $\overline{\text{HAS}}$ deassertion (HMUX = 1)	—	—	7.7	—	ns
319	Address (HAD0–HAD7) hold time after $\overline{\text{HAS}}$ deassertion (HMUX = 1)	—	—	5.5	—	ns
320	HA8–HA10 (HMUX = 1), HA0–HA2 (HMUX = 0), HRW setup time before data strobe assertion[7] • Read • Write	 — —	 — —	 0 7.8	 — —	 ns ns
321	HA8–HA10 (HMUX = 1), HA0–HA2 (HMUX = 0), HRW hold time after data strobe deassertion[7]	—	—	5.5	—	ns
322	Delay from read data strobe deassertion to host request assertion for “Last Data Register” read[3, 5, 9, 10]	—	$2 \times T_C + 27.5$	60.8	—	ns
323	Delay from write data strobe deassertion to host request assertion for “Last Data Register” write[5, 6, 9, 10]	—	$1.5 \times T_C + 27.5$	52.5	—	ns
324	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 0)[5, 7, 9]	—	—	—	27.5	ns
325	Delay from data strobe assertion to host request deassertion for “Last Data Register” read or write (HROD = 1, open drain host request) [5, 7, 9, 10]	—	—	—	300.0	ns

Table 2-13 Host Interface Timing[1, 2] (Continued)

Num	Characteristic	Symbol	Expression	60 MHz		Unit
				Min	Max	

Notes:
1. See **Host Port Usage Considerations** on page 2-20.
2. In the following timing diagrams (**Figure 2-14** through **Figure 2-18**), the controls pins are drawn as active low. Pin polarity is programmable.
3. The Read Data Strobe is HRD in the Dual Data Strobe mode, HDS in the Single Data Strobe mode.
4. This timing must be adhered to only if two consecutive reads from one of these registers are executed.
5. The “Last Data Register” is the register at address $7, which is the last location to be read or written in data transfers.
6. The Write Data Strobe is HWR in the Dual Data Strobe mode, HDS in the Single Data Strobe mode.
7. The Data Strobe is HRD or HWR in the Dual Data Strobe mode, HDS in the Single Data Strobe mode.
8. These timings are periodically sampled and are not 100% tested.
9. The Host Request is HREQ in the Single Host Request mode, HRRQ and HTRQ in the Double Host Request mode.
10. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open Drain mode.

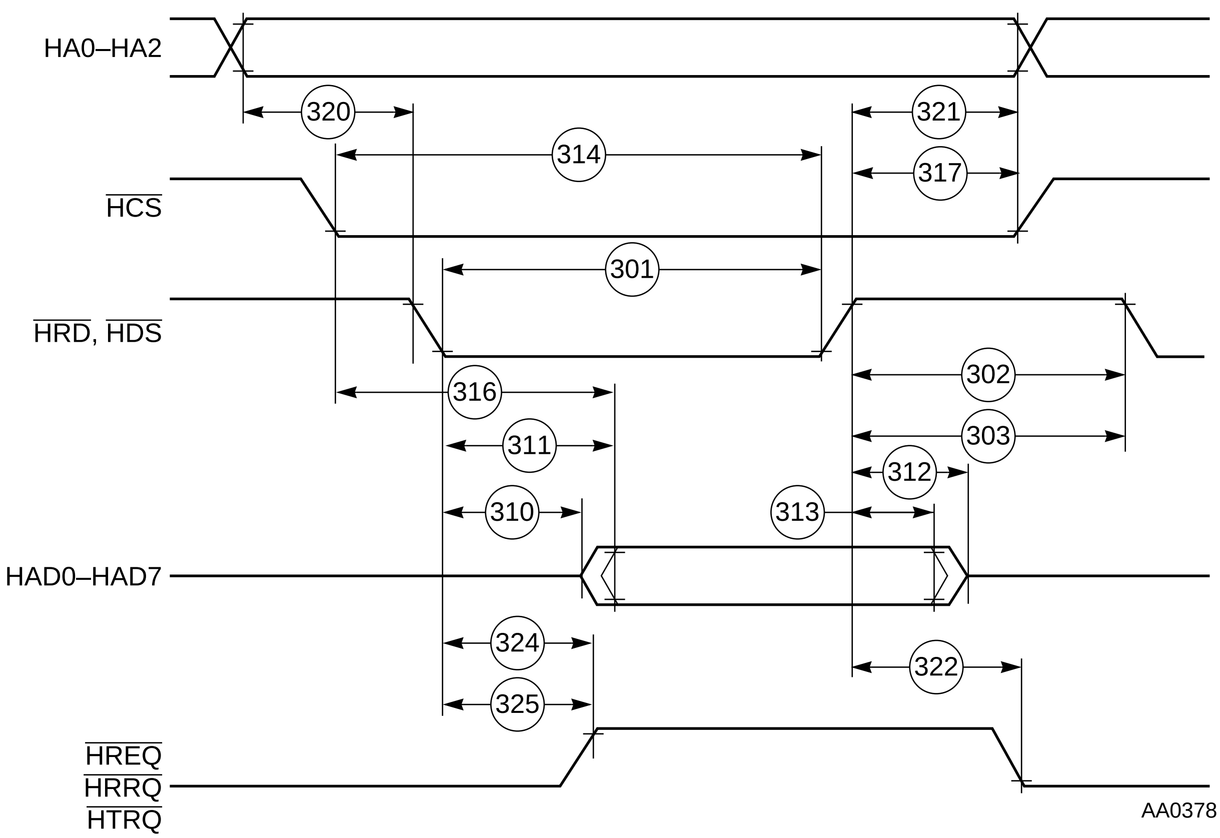


Figure 2-14 Read Timing Diagram—Non-Multiplexed Bus

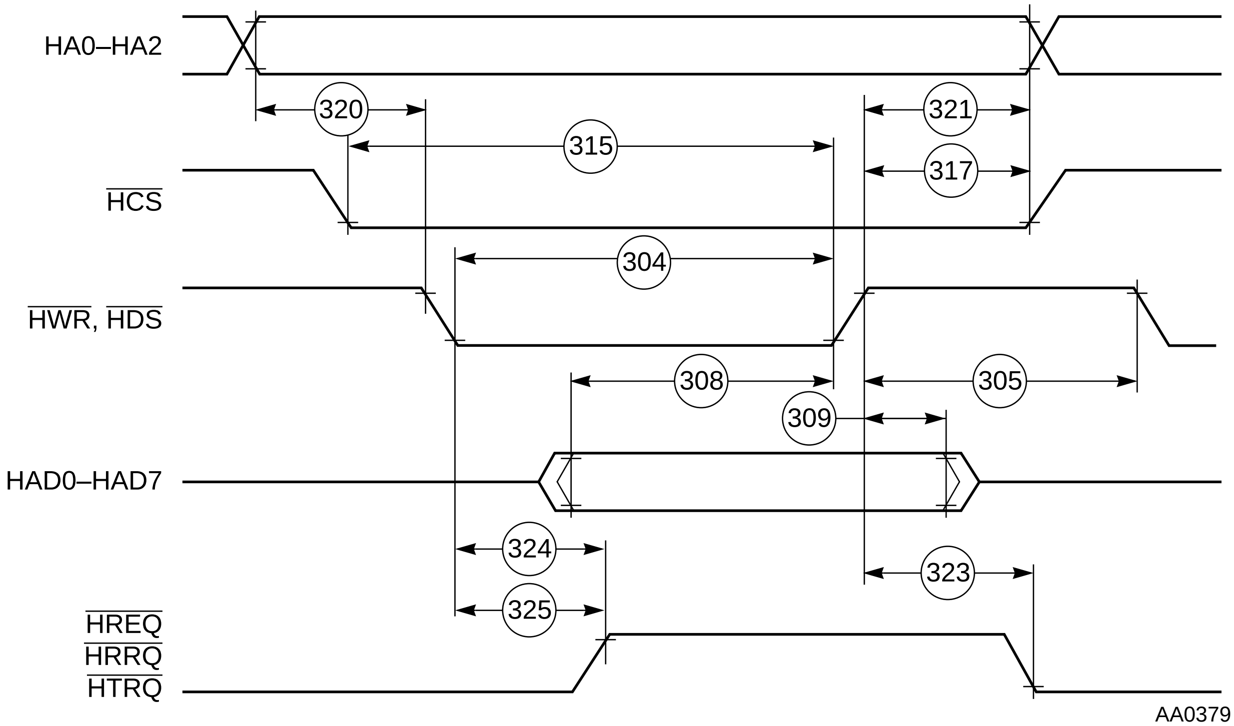


Figure 2-15 Write Timing Diagram—Non-Multiplexed Bus

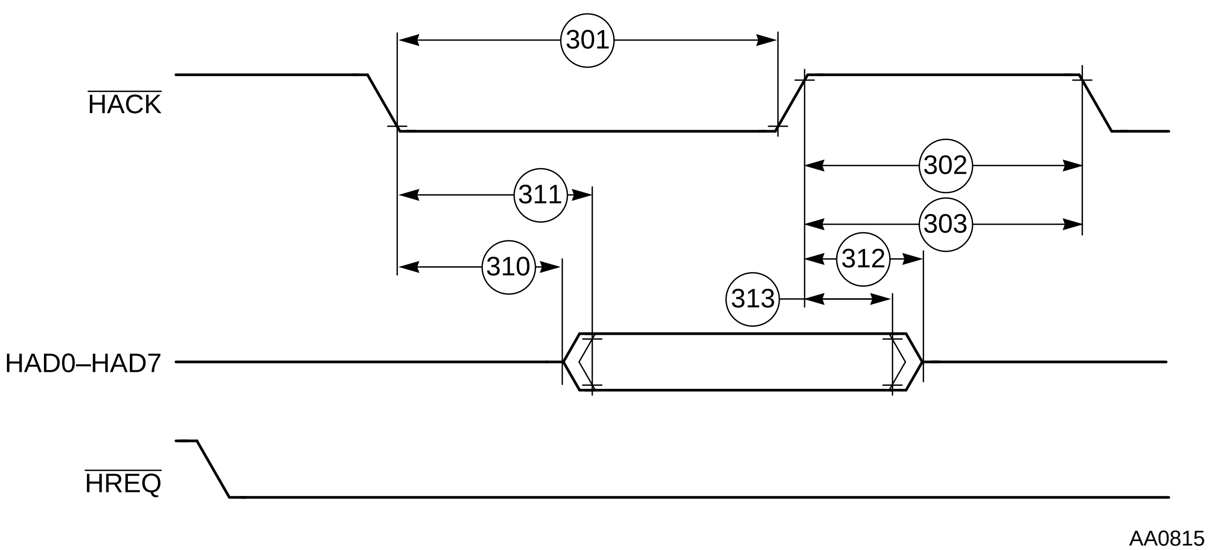


Figure 2-16 Host Interrupt Vector Register (IVR) Read Timing Diagram

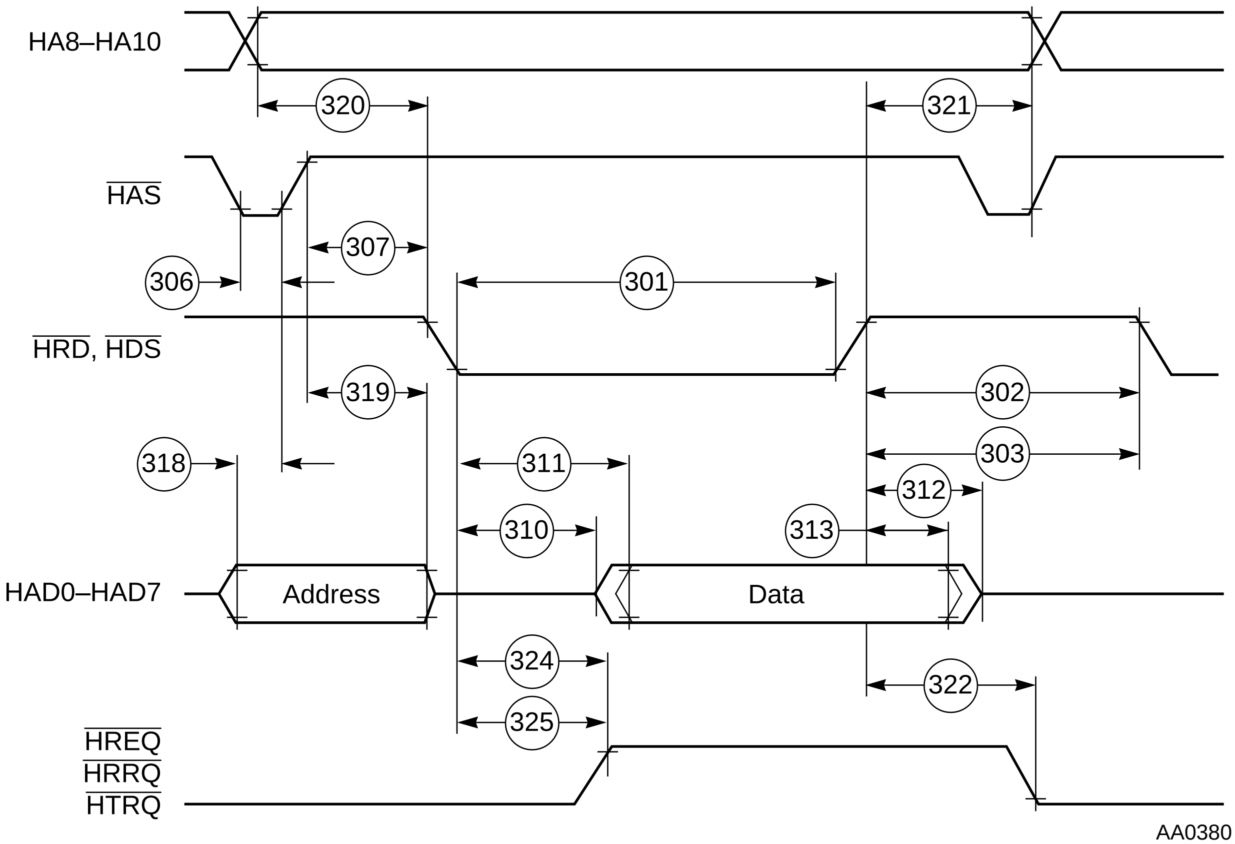


Figure 2-17 Read Timing Diagram—Multiplexed Bus

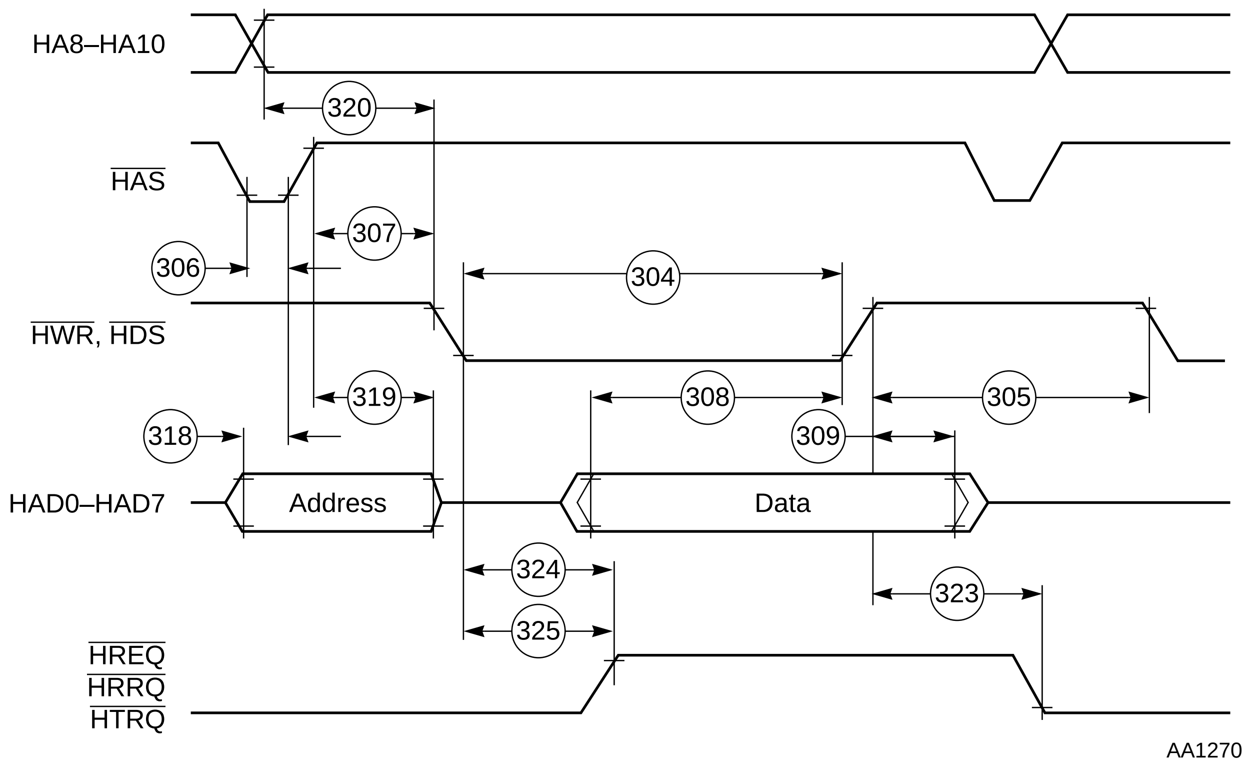


Figure 2-18 Write Timing Diagram—Multiplexed Bus

AC Electrical Characteristics—SSI0/SSI1 Timing

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

Table 2-14 Key to Table 2-15 SSI Timing

Case	Meaning
t_{SSICC}	SSI clock cycle time
TXC	Transmit clock (on SCK pin)
RXC	Receive clock (on SC0 or SCK pin)
FST	Transmit frame sync (on SC2 pin)
FSR	Receive frame sync (SC1 or SC2 pin)
i ck	Internal Clock
x ck	External clock

Table 2-14 Key to Table 2-15 SSI Timing (Continued)

Case	Meaning
i ck a	Internal clock, Asynchronous mode (Asynchronous implies that TXC and RXC are two different clocks)
i ck s	Internal clock, Synchronous mode (Synchronous implies that TXC and RXC are the same clock)
bl	Bit length
wl	Word length
wr	Word length relative

Table 2-15 SSI Timing

Num	Characteristics	Symbol	Expression	60 MHz		Case	Unit
				Min	Max		
430	Clock cycle [1]	t_{SSICC}	$4 \times T_C$ $3 \times T_C$	66.7 50.0	— —	i ck x ck	ns ns
431	Clock high period • For internal clock • For external clock	—	$2 \times T_C - 12.2$ $1.5 \times T_C$	21.1 25.0	— —	i ck x ck	ns ns
432	Clock low period • For internal clock • For external clock	—	$2 \times T_C - 12.2$ $1.5 \times T_C$	21.1 25.0	— —	i ck x ck	ns ns
433	RXC rising edge to FSR Out (bl) high	—	—	— —	45.1 26.8	x ck i ck a	ns ns
434	RXC rising edge to FSR out (bl) low	—	—	— —	45.1 26.8	x ck i ck a	ns ns
435	RXC rising edge to FSR out (wr) high[3]	—	—	— —	47.6 29.3	x ck i ck a	ns ns
436	RXC rising edge to FSR out (wr) low[3]	—	—	— —	47.6 29.3	x ck i ck a	ns ns
437	RXC rising edge to FSR out (wl) high	—	—	— —	45.9 25.6	x ck i ck a	ns ns
438	RXC rising edge to FSR out (wl) low	—	—	— —	45.1 26.8	x ck i ck a	ns ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge	—	—	0.0 23.2	— —	x ck i ck	ns ns

Table 2-15 SSI Timing (Continued)

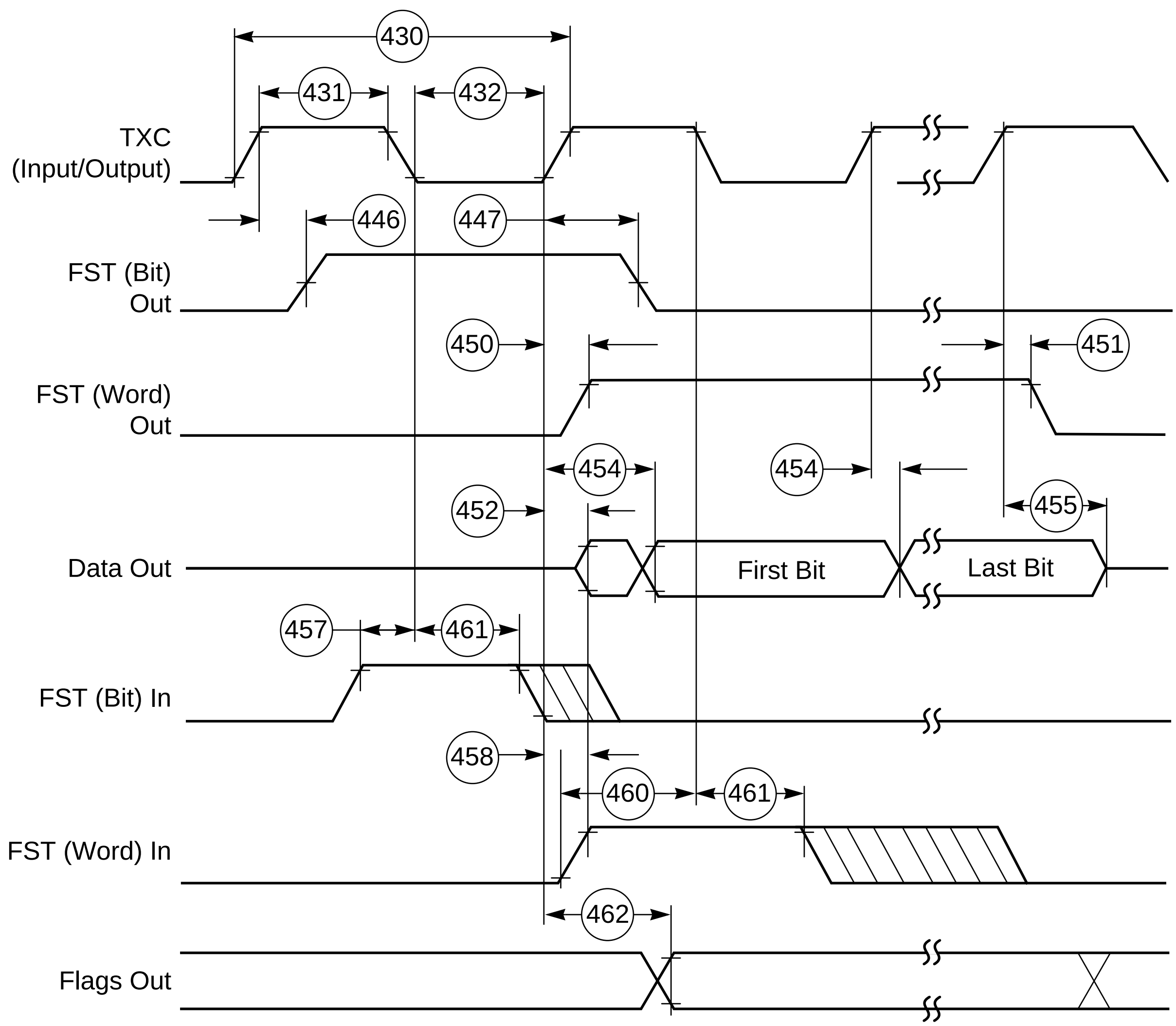
Num	Characteristics	Symbol	Expression	60 MHz		Case	Unit
				Min	Max		
440	Data in hold time after RXC falling edge	—	—	6.1 3.6	— —	x ck i ck	ns ns
441	FSR input (bl, wr) high before RXC falling edge[3]	—	—	28.0 1.2	— —	x ck i ck a	ns ns
442	FSR input (wl) high before RXC falling edge	—	—	28.0 1.2	— —	x ck i ck a	ns ns
443	FSR input hold time after RXC falling edge	—	—	3.6 0.0	— —	x ck i ck a	ns ns
444	Flags input setup before RXC falling edge	—	—	0.0 23.2	— —	x ck i ck s	ns ns
445	Flags input hold time after RXC falling edge	—	—	7.3 0.0	— —	x ck i ck s	ns ns
446	TXC rising edge to FST out (bl) high	—	—	— —	35.4 18.3	x ck i ck	ns ns
447	TXC rising edge to FST out (bl) low	—	—	— —	37.8 20.7	x ck i ck	ns ns
448	TXC rising edge to FST out (wr) high[3]	—	—	— —	37.8 20.7	x ck i ck	ns ns
449	TXC rising edge to FST out (wr) low[3]	—	—	— —	40.3 23.2	x ck i ck	ns ns
450	TXC rising edge to FST out (wl) high	—	—	— —	36.6 19.5	x ck i ck	ns ns
451	TXC rising edge to FST out (wl) low	—	—	— —	37.8 20.7	x ck i ck	ns ns
452	TXC rising edge to data out enable from high impedance	—	—	— —	37.8 20.7	x ck i ck	ns ns
454	TXC rising edge to data out valid	—	$35 + 0.5 \times T_C$	— —	52.8 25.6	x ck i ck	ns ns
455	TXC rising edge to data out high impedance[2]	—	—	— —	37.8 19.5	x ck i ck	ns ns
457	FST input (bl, wr) setup time before TXC falling edge [3]	—	—	2.0 21.0	— —	x ck i ck	ns ns
458	FST input (wl) to data out enable from high impedance[2]	—	—	—	32.9	x ck i ck	ns

Preliminary

Table 2-15 SSI Timing (Continued)

Num	Characteristics	Symbol	Expression	60 MHz		Case	Unit
				Min	Max		
460	FST input (wl) setup time before TXC falling edge	—	—	2.0 21.0	— —	x ck i ck	ns ns
461	FST input hold time after TXC falling edge	—	—	4.0 0.0	— —	x ck i ck	ns ns
462	Flag output valid after TXC rising edge	—	—	— —	39.0 22.0	x ck i ck	ns ns

Notes:
1. For the internal clock, the external clock cycle is defined by I_{cyc} and SSI control register.
2. These timings are periodically sampled and are not 100% tested.
3. The Word Relative Frame Sync signal is related to the clock signal as the Bit Length Frame Sync signal, but has a period that extends from one serial clock pulse prior to the first bit clock pulse (the same as the Bit Length Frame Sync signal) until one serial clock pulse prior to the last bit clock pulse of the first word in the frame.



Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

AA0382

Figure 2-19 SSI Transmitter Timing

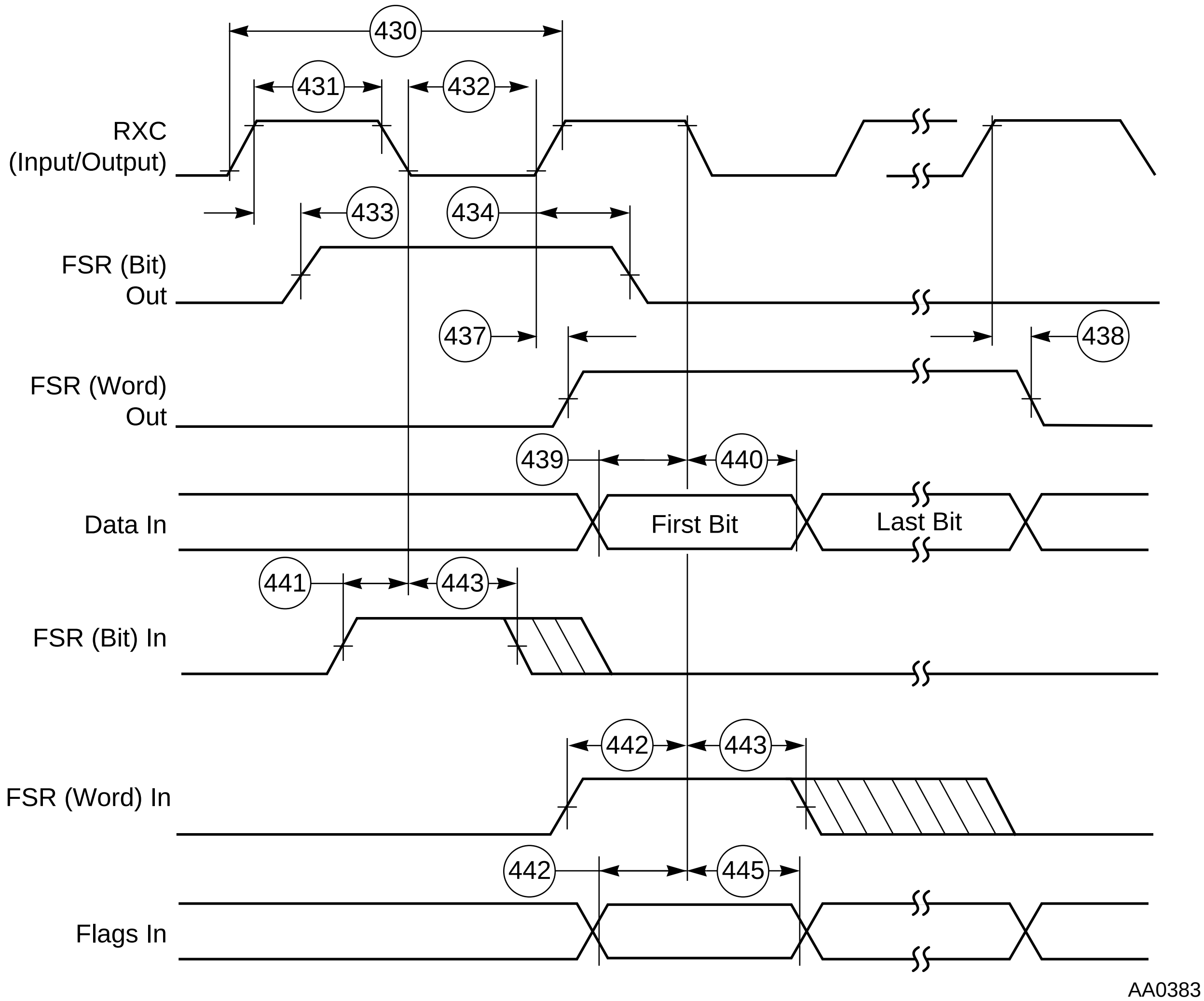


Figure 2-20 SSI Receiver Timing

AC Electrical Characteristics—Timer Timing

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

Table 2-16 Timer Timing

Num	Characteristics	Symbol	Expression	60 MHz		Unit
				Min	Max	
480	TIO low	—	$2 \times T_C + 2.4$	35.7	—	ns
481	TIO high	—	$2 \times T_C + 2.4$	35.7	—	ns
482	Timer setup time from TIO (input) assertion to CLKOUT rising edge	—	T_C	11.0	16.7	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid, caused by first interrupt instruction execution	—	$10.25 \times T_C + 1.2$	172.0	—	ns
484	CLKOUT rising edge to TIO (output) assertion • Minimum • Maximum	—	 $0.5 \times T_C + 4.3$ $0.5 \times T_C + 24.2$	 12.6 —	 — 32.5	 ns ns
485	CLKOUT rising edge to TIO (output) deassertion • Minimum • Maximum	—	 $0.5 \times T_C + 4.3$ $0.5 \times T_C + 24.2$	 12.6 —	 — 32.5	 ns ns

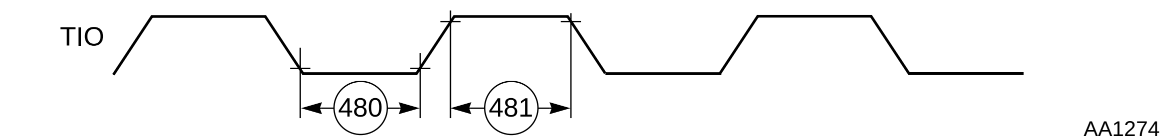


Figure 2-21 TIO Timer Event Input Restrictions

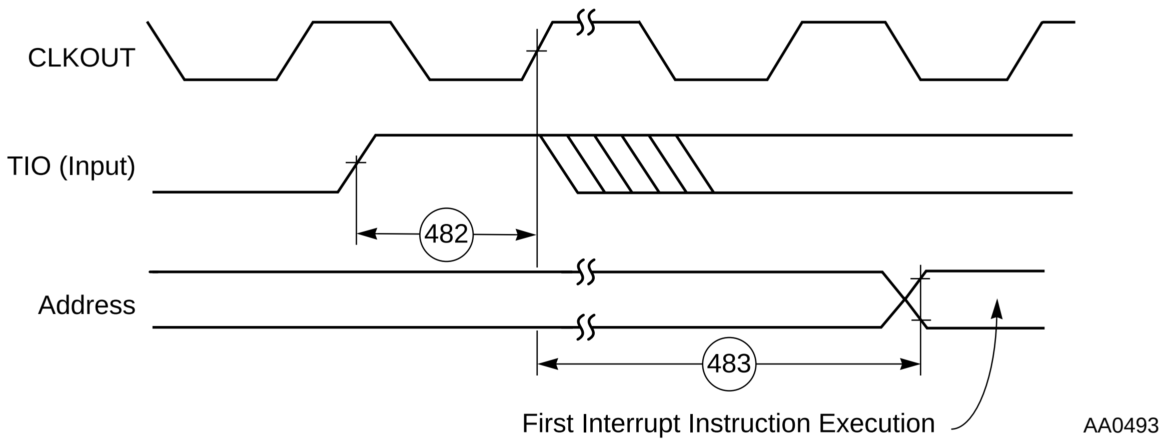


Figure 2-22 Timer Interrupt Generation

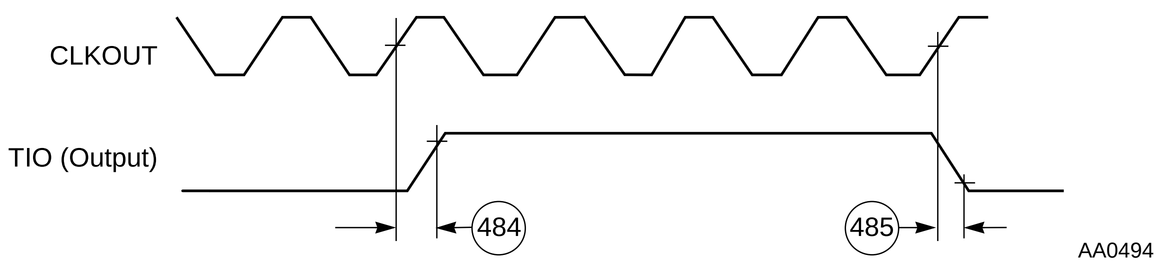


Figure 2-23 External Pulse Generation

AC Electrical Characteristics—GPIO Timing

(V_{CC} = 3.0 V ±0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

Note: GPIO timings apply to all GPIO signals used on the dedicated GPIO pins, HI08 pins, SSI pins, and Timer pins.

Table 2-17 GPIO Timing

Num	Characteristics	Symbol	Expression	60 MHz		Unit
				Min	Max	
490	CLKOUT edge to GPIO output valid (GPIO out delay time)	—	—	—	37.8	ns
491	CLKOUT edge to GPIO output invalid (GPIO out hold time)	—	—	3.6	—	ns
492	GPIO in valid to CLKOUT edge (GPIO in setup time)	—	—	14.6	—	ns
493	CLKOUT edge to GPIO input invalid (GPIO In hold time)	—	—	0.0	—	ns
494	Fetch to CLKOUT edge before GPIO change	—	$6.75 \times T_C$	112.5	—	ns

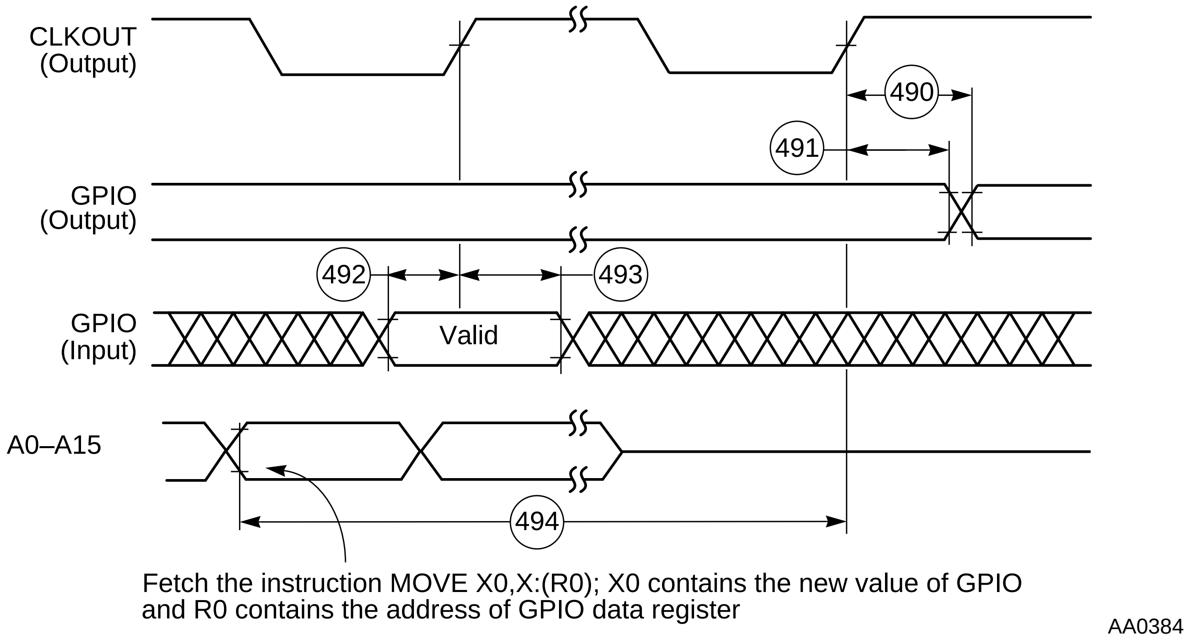


Figure 2-24 GPIO Timing

AC Electrical Characteristics—JTAG Timing

(V_{CC} = 3.0 V ± 0.3 V; T_A = –40° to 85°C, C_L = 50 pF + 2 TTL Loads)

Table 2-18 JTAG Timing

Num	Characteristics	Symbol	Expression	60 MHz		Unit
				Min	Max	
500	TCK frequency of operation	—	$1/(3 \times T_C)$	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	—	—	45.0	—	ns
502	TCK clock pulse width measured at 1.5 V	—	—	20.0	—	ns
503	TCK rise and fall times	—	—	0.0	3.0	ns
504	Boundary scan input data setup time	—	—	5.0	—	ns
505	Boundary scan input data hold time	—	—	24.0	—	ns
506	TCK low to output data valid	—	—	0.0	40.0	ns
507	TCK low to output high impedance*	—	—	0.0	40.0	ns
508	TMS, TDI data setup time	—	—	5.0	—	ns
509	TMS, TDI data hold time	—	—	25.0	—	ns
510	TCK low to TDO data valid	—	—	0.0	44.0	ns
511	TCK low to TDO high impedance*	—	—	0.0	44.0	ns
512	$\overline{\text{TRST}}$ assert time	—	—	100.0	—	ns
513	$\overline{\text{TRST}}$ setup time to TCK low	—	—	40.0	—	ns
514	$\overline{\text{DE}}$ assertion time in order to enter debug mode	—	$1.5 \times T_C + 11.0$	36.0	—	ns
515	Response time when DSP56602 is executing NOP instructions from internal memory	—	$5.5 \times T_C + 33.0$	—	124.7	ns
516	Debug acknowledge assertion time		$3 \times T_C + 11.0$	61.0	—	ns
Note:	* These timings are periodically sampled and are not 100% tested.					

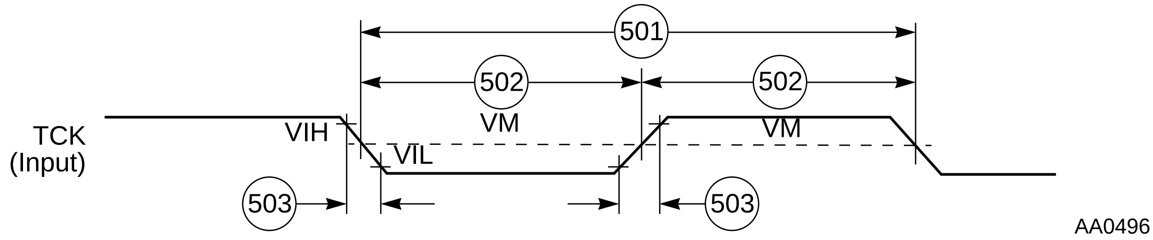


Figure 2-25 Test Clock Input Timing Diagram

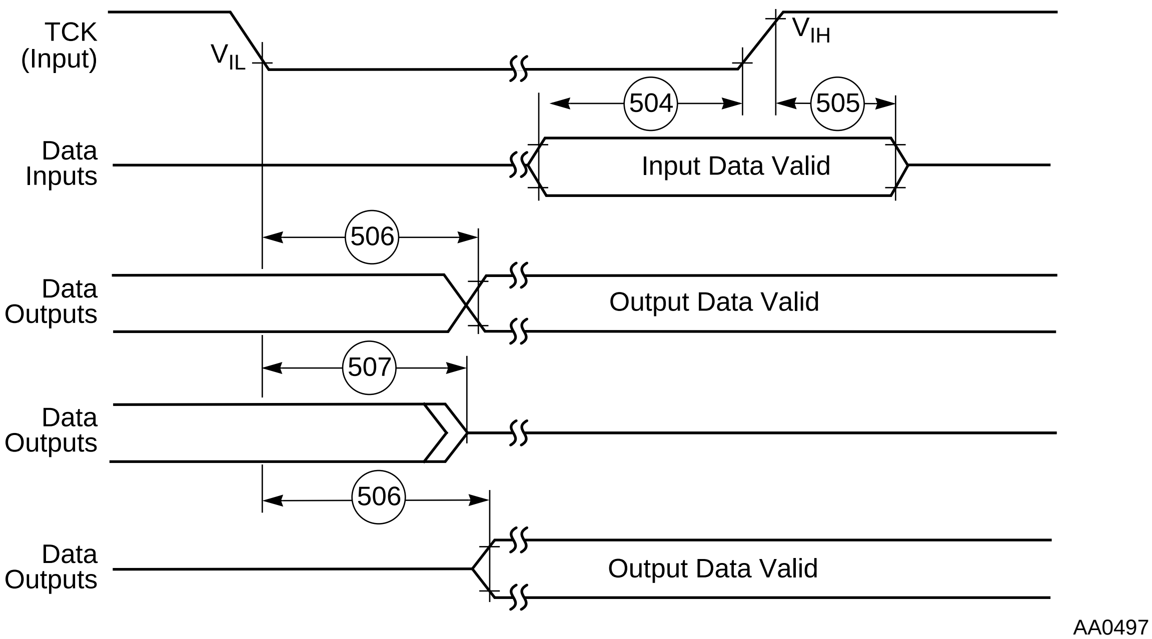


Figure 2-26 Boundary Scan (JTAG) Timing Diagram

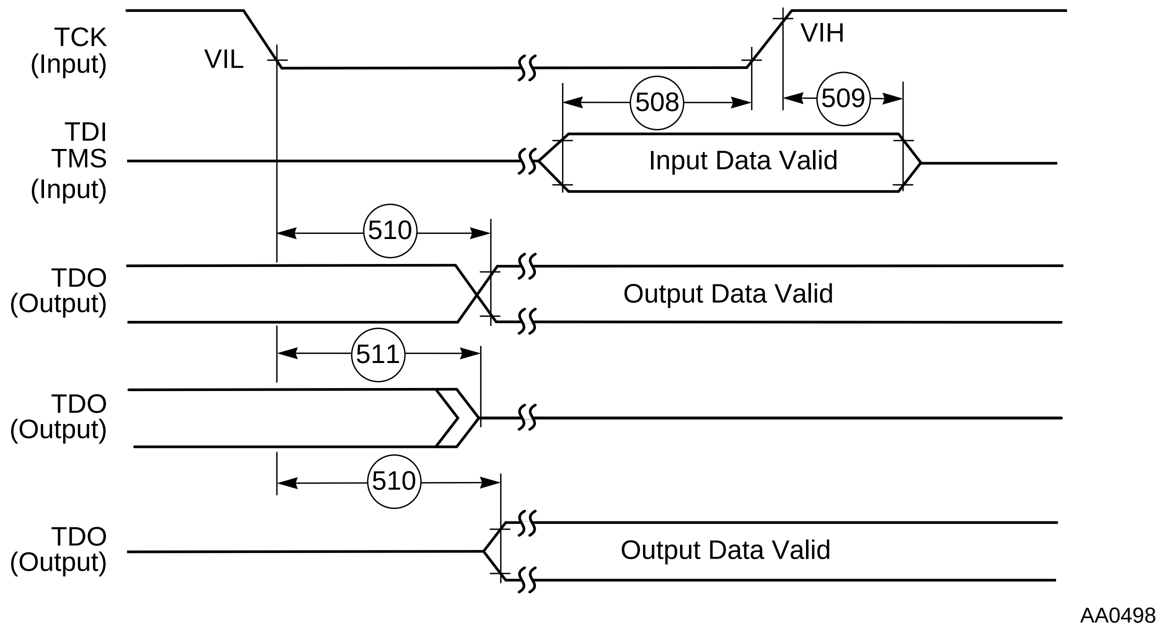


Figure 2-27 Test Access Port Timing Diagram

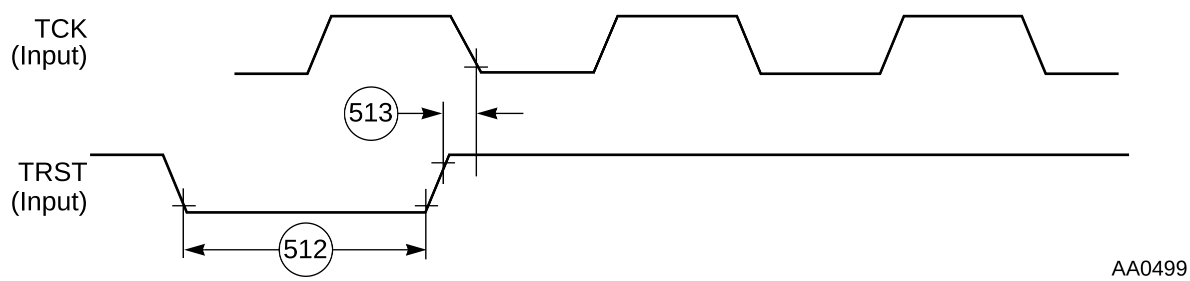


Figure 2-28 $\overline{\text{TRST}}$ Timing Diagram

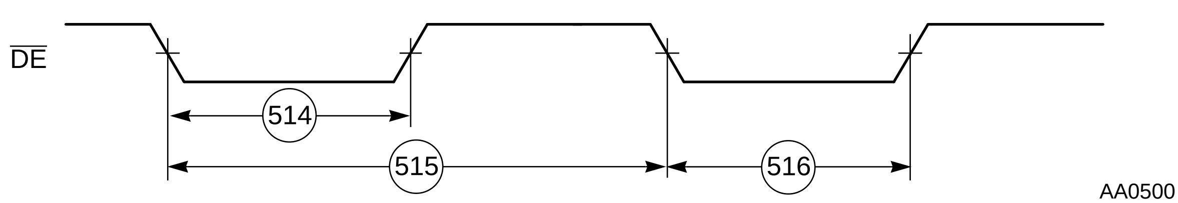


Figure 2-29 OnCE—Debug Request

SECTION 3

PACKAGING

PACKAGE AND PIN-OUT INFORMATION

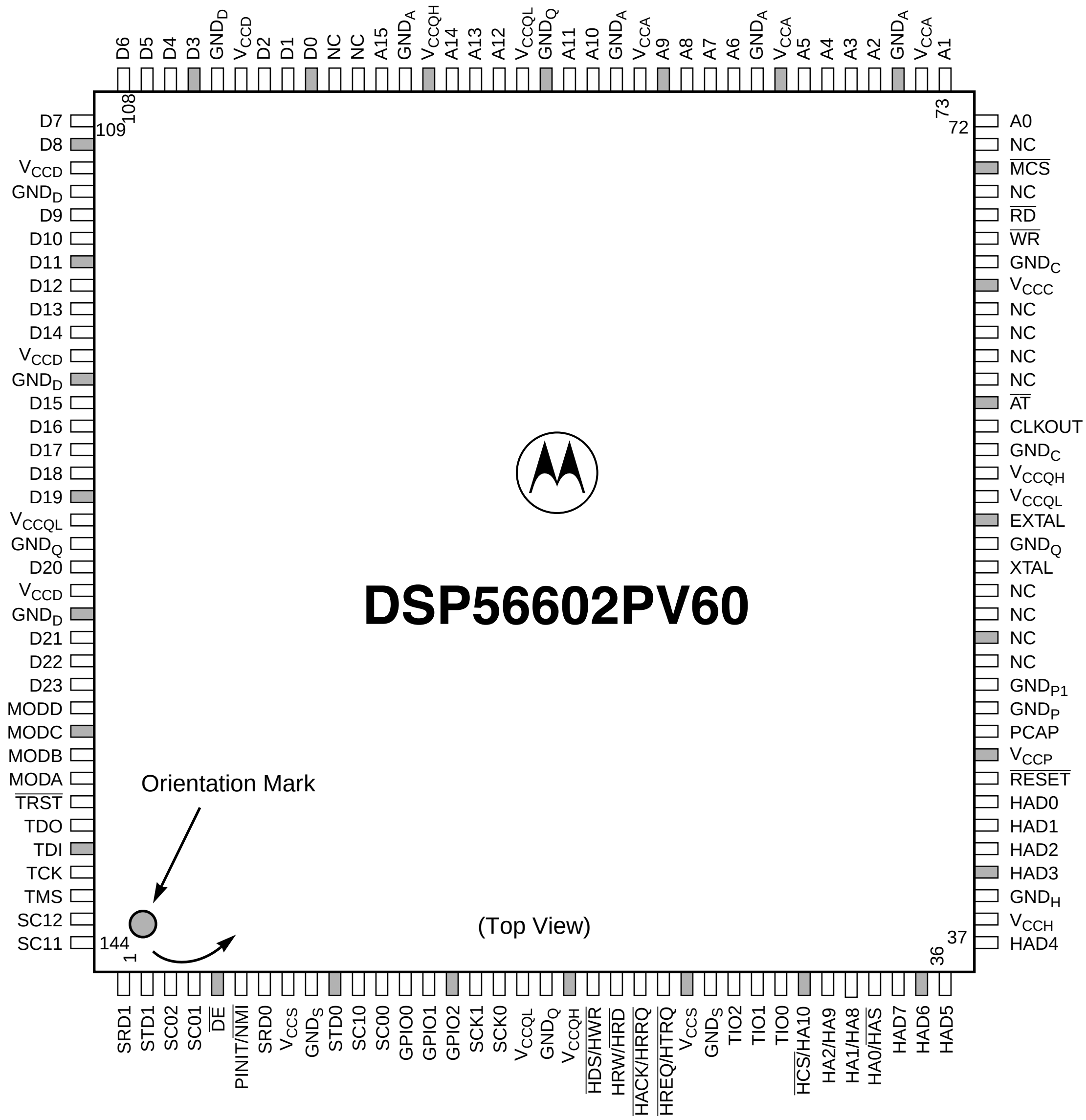
This section contains package and pin-out information for the 144-pin Thin Quad Flat Pack (TQFP) and 144-pin Plastic Ball Grid Array (PBGA) configurations of the DSP56602.

TQFP Package Data

- **Figure 3-1** on page 3-2 and **Figure 3-2** on page 3-3 show the pinout of the TQFP DSP56602.
- **Table 3-1** on page 3-4 identifies the DSP56602 pins on the TQFP package in numeric order.
- **Table 3-2** on page 3-5 identifies the TQFP pins by name order.
- **Table 3-3** on page 3-8 groups power and ground pins for the TQFP package.
- Mechanical drawings of the TQFP package are presented in **Figure 3-3** on page 3-9.

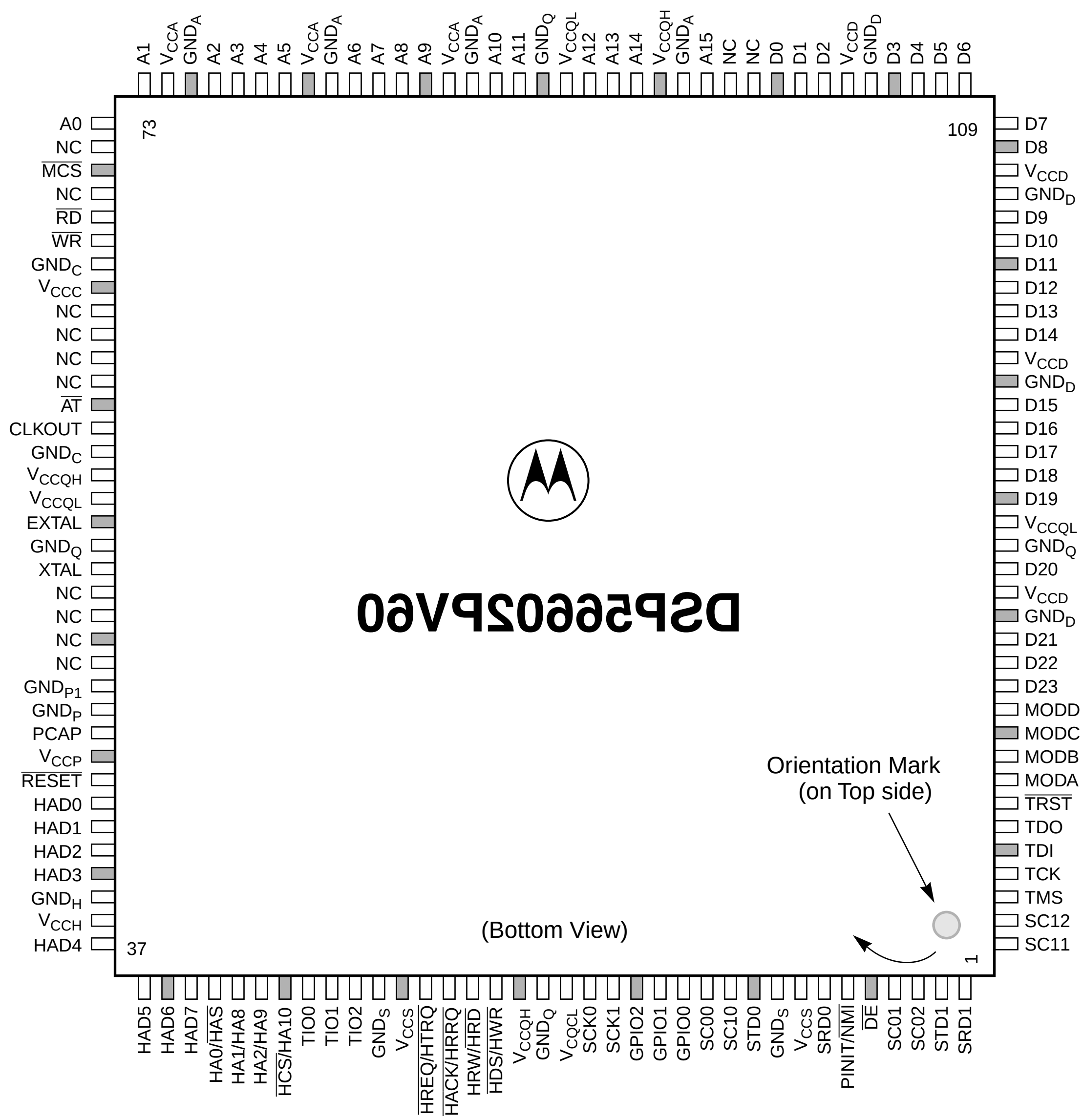
PBGA Package Data

- **Figure 3-4** on page 3-10 and **Figure 3-5** on page 3-11 show the pinout of the PBGA DSP56602.
- **Table 3-4** on page 3-12 identifies the DSP56602 pins on the PBGA package in numeric order.
- **Table 3-5** on page 3-14 identifies the PBGA pins by name order.
- **Table 3-6** on page 3-16 groups power and ground pins for the PBGA package.
- Mechanical drawings of the PBGA package are presented in **Figure 3-6** on page 3-17.



Notes:
1. Pins marked “NC” are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.
2. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 3-1 Top View, DSP56602 144-pin TQFP Package



Notes: 1. Pins marked “NC” are no connection pins that are reserved for possible future enhancements. Do not connect these pins to any power, ground, signal traces, or vias.

2. To simplify locating the pins, each fifth pin is shaded in the illustration.

Figure 3-2 Bottom View, DSP56602 TQFP Package

Table 3-1 DSP56602 144-pin TQFP Pin Identification by Pin Number

UP		RIGHT		DOWN		LEFT	
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
144	SC11	108	D6	72	A0	36	HAD5
143	SC12	107	D5	71	NC	35	HAD6
142	TMS	106	D4	70	$\overline{MCS}$	34	HAD7
141	TCK	105	D3	69	NC	33	HA0/$\overline{HAS}$
140	TDI	104	GND_D	68	$\overline{RD}$	32	HA1/HA8
139	TDO	103	V_{CCD}	67	$\overline{WR}$	31	HA2/HA9
138	$\overline{TRST}$	102	D2	66	GND_C	30	$\overline{HCS}$/HA10
137	MODA	101	D1	65	V_{CCC}	29	TIO0
136	MODB	100	D0	64	NC	28	TIO1
135	MODC	99	NC	63	NC	27	TIO2
134	MODD	98	NC	62	NC	26	GND_S
133	D23	97	A15	61	NC	25	V_{CCS}
132	D22	96	GND_A	60	$\overline{AT}$	24	$\overline{HREQ}$/$\overline{HTRQ}$
131	D21	95	V_{CCQH}	59	CLKOUT	23	$\overline{HACK}$/$\overline{HRRQ}$
130	GND_D	94	A14	58	GND_C	22	HRW/$\overline{HRD}$
129	V_{CCD}	93	A13	57	V_{CCQH}	21	$\overline{HDS}$/$\overline{HWR}$
128	D20	92	A12	56	V_{CCQL}	20	V_{CCQH}
127	GND_Q	91	V_{CCQL}	55	EXTAL	19	GND_Q
126	V_{CCQL}	90	GND_Q	54	GND_Q	18	V_{CCQL}
125	D19	89	A11	53	XTAL	17	SCK0
124	D18	88	A10	52	NC	16	SCK1
123	D17	87	GND_A	51	NC	15	GPIO2
122	D16	86	V_{CCA}	50	NC	14	GPIO1
121	D15	85	A9	49	NC	13	GPIO0
120	GND_D	84	A8	48	GND_{P1}	12	SC00
119	V_{CCD}	83	A7	47	GND_P	11	SC10
118	D14	82	A6	46	PCAP	10	STD0
117	D13	81	GND_A	45	V_{CCP}	9	GND_S
116	D12	80	V_{CCA}	44	$\overline{RESET}$	8	V_{CCS}
115	D11	79	A5	43	HAD0	7	SRD0
114	D10	78	A4	42	HAD1	6	PINIT/$\overline{NMI}$
113	D9	77	A3	41	HAD2	5	$\overline{DE}$
112	GND_D	76	A2	40	HAD3	4	SC01
111	VCC_D	75	GND_A	39	GND_H	3	SC02
110	D8	74	V_{CCA}	38	V_{CCH}	2	STD1
109	D7	73	A1	37	HAD4	1	SRD1

Note: Pins marked NC are not connected.

Table 3-2 DSP56602 144-pin TQFP Pin Identification by Pin Name

Name	Pin #	Functional Group	Name	Pin #	Functional Group
A0	72	Port A Address	D8	110	Port A Data
A1	73		D9	113	
A2	76		D10	114	
A3	77		D11	115	
A4	78		D12	116	
A5	79		D13	117	
A6	82		D14	118	
A7	83		D15	121	
A8	84		D16	122	
A9	85		D17	123	
A10	88		D18	124	
A11	89		D19	125	
A12	92		D20	128	
A13	93		D21	131	
A14	94		D22	132	
A15	97		D23	133	
$\overline{AT}$	60	Port A Control	$\overline{DE}$	5	JTAG/OnCE
CLKOUT	59	Clock/PLL	EXTAL	55	
D0	100	Port A Data	GND_A	75	GND—Port A Address
D1	101		GND_A	81	
D2	102		GND_A	87	
D3	105		GND_A	96	
D4	106		GND_C	66	GND—Port A Control
D5	107		GND_C	58	
D6	108		GND_D	104	GND—Port A Data
D7	109		GND_D	112	

Table 3-2 DSP56602 144-pin TQFP Pin Identification by Pin Name (Continued)

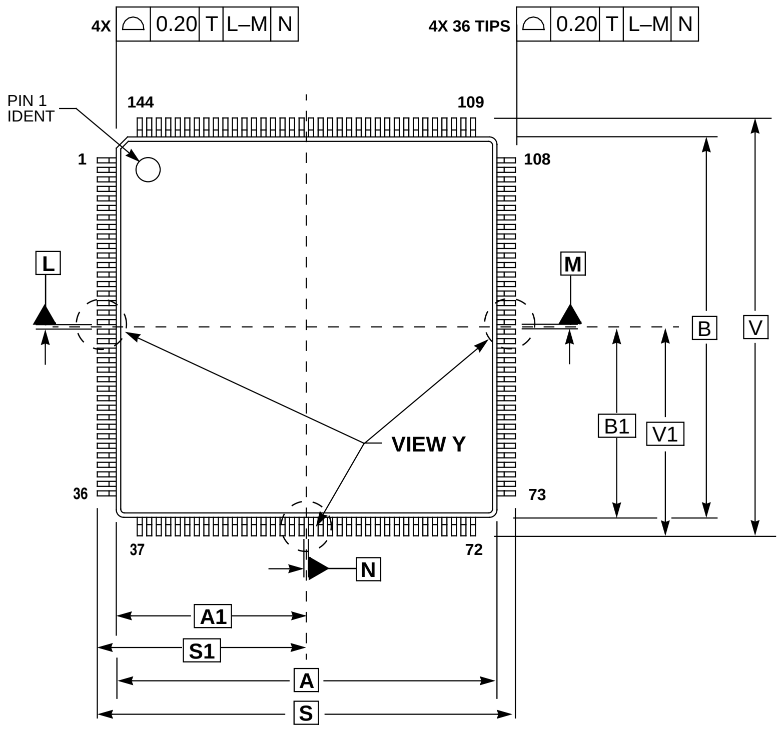
Name	Pin #	Functional Group	Name	Pin #	Functional Group
GND_D	120	GND—Port A Data	$\overline{\text{HCS}}$/HA10	30	Peripherals/HI08
GND_D	130		$\overline{\text{HDS}}$/$\overline{\text{HWR}}$	21	
GND_H	39	GND—HI08 Data	$\overline{\text{HREQ}}$/$\overline{\text{HTRQ}}$	24	
GND_P	47	GND—PLL	HRW/$\overline{\text{HRD}}$	22	
GND_{P1}	48		$\overline{\text{MCS}}$	70	Port A Control
GND_Q	19	Quiet GND (for both V_{CCQH} and V_{CCQL})	MODA/$\overline{\text{IRQA}}$	137	Mode/Interrupt Control
GND_Q	54		MODB/$\overline{\text{IRQB}}$	136	
GND_Q	90		MODC/$\overline{\text{IRQC}}$	135	
GND_Q	127		MODD/$\overline{\text{IRQD}}$	134	
GND_S	9	GND—SSI, Timer, GPIO, HI08 Control	PCAP	46	Clock/PLL
GND_S	26		PINIT/$\overline{\text{NMI}}$	6	
GPIO0	13	Peripherals/GPIO	$\overline{\text{RD}}$	68	Port A Control
GPIO1	14		$\overline{\text{RESET}}$	44	
GPIO2	15		SC00	12	Peripherals/SSI0
HA0/$\overline{\text{HAS}}$	33	Peripherals/HI08	SC01	4	
HA1/HA8	32		SC02	3	
HA2/HA9	31		SC10	11	Peripherals/SSI1
$\overline{\text{HACK}}$/$\overline{\text{HRRQ}}$	23		SC11	144	
HAD0	43		SC12	143	
HAD1	42		SCK0	17	Peripherals/SSI0
HAD2	41		SCK1	16	Peripherals/SSI1
HAD3	40		SRD0	7	Peripherals/SSI0
HAD4	37		SRD1	1	Peripherals/SSI1
HAD5	36		STD0	10	Peripherals/SSI0
HAD6	35		STD1	2	Peripherals/SSI1
HAD7	34		TCK	141	JTAG/OnCE

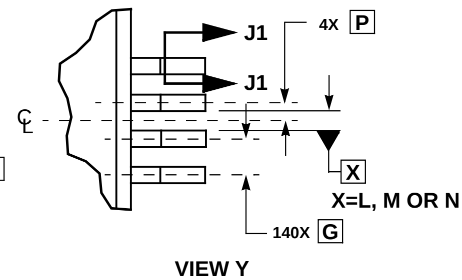
Table 3-2 DSP56602 144-pin TQFP Pin Identification by Pin Name (Continued)

Name	Pin #	Functional Group	Name	Pin #	Functional Group
TDI	140	JTAG/OnCE	V_{CCH}	38	V_{CC}—HI08 Data
TDO	139		V_{CCP}	45	V_{CC}—PLL
TIO0	29	Peripherals/Timer	V_{CCQH}	20	Quiet V_{CC} High
TIO1	28		V_{CCQH}	57	
TIO2	27		V_{CCQH}	95	
TMS	142	JTAG/OnCE	V_{CCQL}	18	Quiet V_{CC} Low
$\overline{TRST}$	138		V_{CCQL}	56	
V_{CCA}	74	V_{CC}—Port A Address	V_{CCQL}	91	
V_{CCA}	80		V_{CCQL}	126	
V_{CCA}	86		V_{CCS}	8	V_{CC} —SSI, Timer, GPIO, HI08 Control
V_{CCC}	65	V_{CC}—Port A Control	V_{CCS}	25	
V_{CCD}	103	V_{CC}—Port A Data	$\overline{WR}$	67	Port A Control
V_{CCD}	111		XTAL	53	Clock/PLL
V_{CCD}	119		Not Connected	49, 50, 51, 52, 61, 62, 63, 64, 69, 71, 98, 99	
V_{CCD}	129				

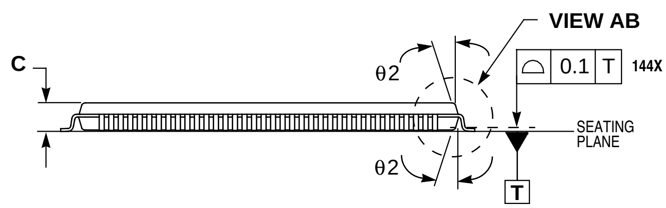
Table 3-3 DSP56602 TQFP Power Supply Pins

Name	Pin #	Functional Group	Name	Pin #	Functional Group
V_{CCA}	74	Core/Port A Address	V_{CCD}	103	Core/Port A Data
V_{CCA}	80		V_{CCD}	111	
V_{CCA}	86		V_{CCD}	119	
GND_A	75		V_{CCD}	129	
GND_A	81		GND_D	104	
GND_A	87		GND_D	112	
GND_A	96		GND_D	120	
V_{CCC}	65	Core/Port A Control	GND_D	130	
GND_C	66		V_{CCP}	45	Core/PLL
GND_C	58		GND_P	47	
V_{CCQH}	20	Quiet V_{CC} High	GND_{P1}	48	
V_{CCQH}	57		GND_Q	19	Quiet GND (for both V_{CCQH} and V_{CCQL})
V_{CCQH}	95		GND_Q	54	
V_{CCLQ}	18	Quiet V_{CC} Low	GND_Q	90	
V_{CCQL}	56		GND_Q	127	
V_{CCQL}	91		V_{CCH}	38	Peripherals/HI08 Data
V_{CCQL}	126		GND_H	39	
GND_S	9	Peripherals/SSI0, SSI1, Timer, GPIO, HI08 Control	V_{CCS}	8	Peripherals/SSI0, SSI1, Timer, GPIO, HI08 Control
GND_S	26		V_{CCS}	25	

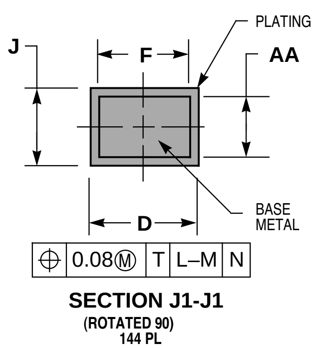


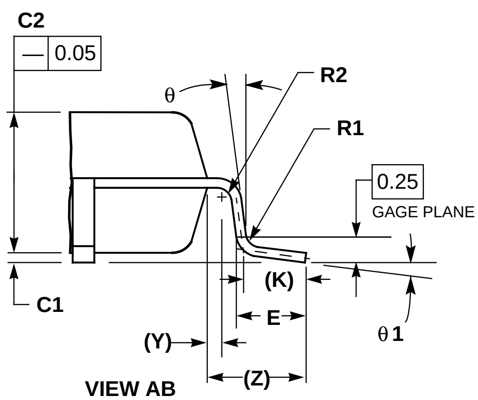


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5-1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCULDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLED DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.35.



DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	–
θ1	0°	7°
θ2	11°	13°





CASE 918-03

Figure 3-3 144-pin Thin Quad Flat Pack (TQFP) Mechanical Information

PBGA Package Description

Top and bottom views of the DSP56602 PBGA package are shown in **Figure 3-5** and **Figure 3-6** with their pin-outs.

Top View

	1	2	3	4	5	6	7	8	9	10	11	12
A	SC11	TMS	TCK	MODA	D22	D20	D18	D14	D12	D11	D8	D7
B	STD1	SRD1	SC12	TDI	MODC	D21	D19	D15	D13	D9	D6	D4
C	SC01	SC02	$\overline{TRST}$	TDO	D23	GND_D	D17	D16	D10	D3	D5	D1
D	$\overline{DE}$	PINIT	MODB	MODD	NC	NC	NC	NC	GND_D	V_{CCD}	D2	D0
E	SRD0	STD0	SC00	NC	V_{CCD}	GND_Q	V_{CCQL}	V_{CCD}	NC	A14	V_{CCQH}	A15
F	SC10	GPIO0	V_{CCQL}	NC	V_{CCS}	NC	NC	GND_A	NC	GND_Q	A12	A13
G	GPIO1	SCK0	V_{CCQH}	NC	GND_S	NC	NC	V_{CCQL}	NC	V_{CCA}	A9	A11
H	GPIO2	HRW	TIO2	NC	GND_S	GND_Q	V_{CCQL}	GND_A	NC	GND_A	A6	A10
J	SCK1	$\overline{HREQ}$	TIO1	V_{CCH}	NC	NC	NC	NC	V_{CCA}	GND_A	A4	A8
K	$\overline{HDS}$	$\overline{HCS}$	HA2	GND_H	V_{CCP}	GND_P	V_{CCQH}	V_{CCC}	GND_C	$\overline{WR}$	A2	A7
L	$\overline{HACK}$	HA0	HAD6	HAD4	HAD1	PCAP	$\overline{RESET}$	EXTAL	$\overline{AT}$	A0	A1	A5
M	TIO0	HA1	HAD7	HAD5	HAD3	HAD2	HAD0	XTAL	CLK OUT	$\overline{RD}$	$\overline{MCS}$	A3

Figure 3-4 Top View, DSP56602 PBGA Package

Bottom View

	12	11	10	9	8	7	6	5	4	3	2	1
A	D7	D8	D11	D12	D14	D18	D20	D22	MODA	TCK	TMS	SC11
B	D4	D6	D9	D13	D15	D19	D21	MODC	TDI	SC12	SRD1	STD1
C	D1	D5	D3	D10	D16	D17	GND_D	D23	TDO	$\overline{TRST}$	SC02	SC01
D	D0	D2	V_{CCD}	GND_D	NC	NC	NC	NC	MODD	MODB	PINIT	$\overline{DE}$
E	A15	V_{CCQH}	A14	NC	V_{CCD}	V_{CCQL}	GND_Q	V_{CCD}	NC	SC00	STD0	SRD0
F	A13	A12	GND_Q	NC	GND_A	NC	NC	V_{CCS}	GND_D	V_{CCQL}	GPIO0	SC10
G	A11	A9	V_{CCA}	NC	V_{CCQL}	NC	NC	GND_S	NC	V_{CCQH}	SCK0	GPIO1
H	A10	A6	GND_A	NC	GND_A	V_{CCQL}	GND_Q	GND_S	NC	TIO2	HRW	GPIO2
J	A8	A4	GND_A	V_{CCA}	NC	NC	NC	NC	V_{CCH}	TIO1	$\overline{HREQ}$	SCK1
K	A7	A2	$\overline{WR}$	C	V_{CCC}	V_{CCQH}	GND_P	V_{CCP}	GND_H	HA2	$\overline{HCS}$	$\overline{HDS}$
L	A5	A1	A0	$\overline{AT}$	EXTAL	$\overline{RESET}$	PCAP	HAD1	HAD4	HAD6	HA0	$\overline{HACK}$
M	A3	$\overline{MCS}$	$\overline{RD}$	CLK OUT	XTAL	HAD0	HAD2	HAD3	HAD5	HAD7	HA1	TIO0

Figure 3-5 Bottom View, DSP56602 PBGA Package

Table 3-4 DSP56602 PBGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	SC11	C1	SC01	E1	SRD0
A2	TMS	C2	SC02	E2	STD0
A3	TCK	C3	$\overline{\text{TRST}}$	E3	SC00
A4	MODA/$\overline{\text{IRQA}}$	C4	TDO	E4	NC
A5	D22	C5	D23	E5	V_{CCD}
A6	D20	C6	GND_D	E6	GND_Q
A7	D18	C7	D17	E7	V_{CCQL}
A8	D14	C8	D16	E8	V_{CCD}
A9	D12	C9	D10	E9	NC
A10	D11	C10	D3	E10	A14
A11	D8	C11	D5	E11	V_{CCQH}
A12	D7	C12	D1	E12	A15
B1	STD1	D1	$\overline{\text{DE}}$	F1	SC10
B2	SRD1	D2	PINIT/$\overline{\text{NMI}}$	F2	GPIO0
B3	SC12	D3	MODB/$\overline{\text{IRQB}}$	F3	V_{CCQL}
B4	TDI	D4	MODD/$\overline{\text{IRQD}}$	F4	NC
B5	MODC/$\overline{\text{IRQC}}$	D5	NC	F5	V_{CCS}
B6	D21	D6	NC	F6	NC
B7	D19	D7	NC	F7	NC
B8	D15	D8	NC	F8	GND_A
B9	D13	D9	GND_D	F9	NC
B10	D9	D10	V_{CCD}	F10	GND_Q
B11	D6	D11	D2	F11	A12
B12	D4	D12	D0	F12	A13

Table 3-4 DSP56602 PBGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
G1	GPIO1	J1	SCK1	L1	$\overline{\text{HACK}}$/$\overline{\text{HRRQ}}$
G2	SCK0	J2	$\overline{\text{HREQ}}$/$\overline{\text{HTRQ}}$	L2	HA0/$\overline{\text{HAS}}$
G3	V_{CCQH}	J3	TIO1	L3	HAD6
G4	NC	J4	V_{CCH}	L4	HAD4
G5	GND_S	J5	NC	L5	HAD1
G6	NC	J6	NC	L6	PCAP
G7	NC	J7	NC	L7	$\overline{\text{RESET}}$
G8	V_{CCQL}	J8	NC	L8	EXTAL
G9	NC	J9	V_{CCA}	L9	$\overline{\text{AT}}$
G10	V_{CCA}	J10	GND_A	L10	A0
G11	A9	J11	A4	L11	A1
G12	A11	J12	A8	L12	A5
H1	GPIO2	K1	$\overline{\text{HDS}}$/$\overline{\text{HWR}}$	M1	TIO0
H2	HRW/ $\overline{\text{HRD}}$	K2	$\overline{\text{HCS}}$/HA10	M2	HA1/HA8
H3	TIO2	K3	HA2/HA9	M3	HAD7
H4	NC	K4	GND_H	M4	HAD5
H5	GND_S	K5	V_{CCP}	M5	HAD3
H6	GND_Q	K6	GND_P	M6	HAD2
H7	V_{CCQL}	K7	V_{CCQH}	M7	HAD0
H8	GND_A	K8	V_{CCC}	M8	XTAL
H9	NC	K9	GND_D	M9	CLKOUT
H10	GND_A	K10	$\overline{\text{WR}}$	M10	$\overline{\text{RD}}$
H11	A6	K11	A2	M11	$\overline{\text{MCS}}$
H12	A10	K12	A7	M12	A3

Note: Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/$\overline{\text{IRQx}}$ pins that select an operating mode after $\overline{\text{RESET}}$ is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as HA0/$\overline{\text{HAS}}$. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. Pins marked NC are reserved and should not be connected.

Table 3-5 DSP56602 PBGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	L10	D11	A10	GPIO0	F2
A1	L11	D12	A9	GPIO1	G1
A2	K11	D13	B9	GPIO2	H1
A3	M12	D14	A8	HA0/$\overline{\text{HAS}}$	L2
A4	J11	D15	B8	HA1/HA8	M2
A5	L12	D16	C8	HA2/HA9	K3
A6	H11	D17	C7	$\overline{\text{HACK}}$/$\overline{\text{HRRQ}}$	L1
A7	K12	D18	A7	HAD0	M7
A8	J12	D19	B7	HAD1	L5
A9	G11	D20	A6	HAD2	M6
A10	H12	D21	B6	HAD3	M5
A11	G12	D22	A5	HAD4	L4
A12	F11	D23	C5	HAD5	M4
A13	F12	$\overline{\text{DE}}$	D1	HAD6	L3
A14	E10	EXTAL	L8	HAD7	M3
A15	E12	GND_A	F8	$\overline{\text{HCS}}$/HA10	K2
$\overline{\text{AT}}$	L9	GND_A	H8	$\overline{\text{HDS}}$/$\overline{\text{HWR}}$	K1
CLKOUT	M9	GND_A	H10	$\overline{\text{HREQ}}$/$\overline{\text{HTRQ}}$	J2
D0	D12	GND_A	J10	HRW/$\overline{\text{HRD}}$	H2
D1	C12	GND_D	C6	$\overline{\text{IRQA}}$	A4
D2	D11	GND_D	D9	$\overline{\text{IRQB}}$	D3
D3	C10	GND_D	K9	$\overline{\text{IRQC}}$	B5
D4	B12	GND_H	K4	$\overline{\text{IRQD}}$	D4
D5	C11	GND_P	K6	$\overline{\text{MCS}}$	M11
D6	B11	GND_Q	E6	MODA	A4
D7	A12	GND_Q	F10	MODB	D3
D8	A11	GND_Q	H6	MODC	B5
D9	B10	GND_S	G5	MODD	D4
D10	C9	GND_S	H5	NC	D5

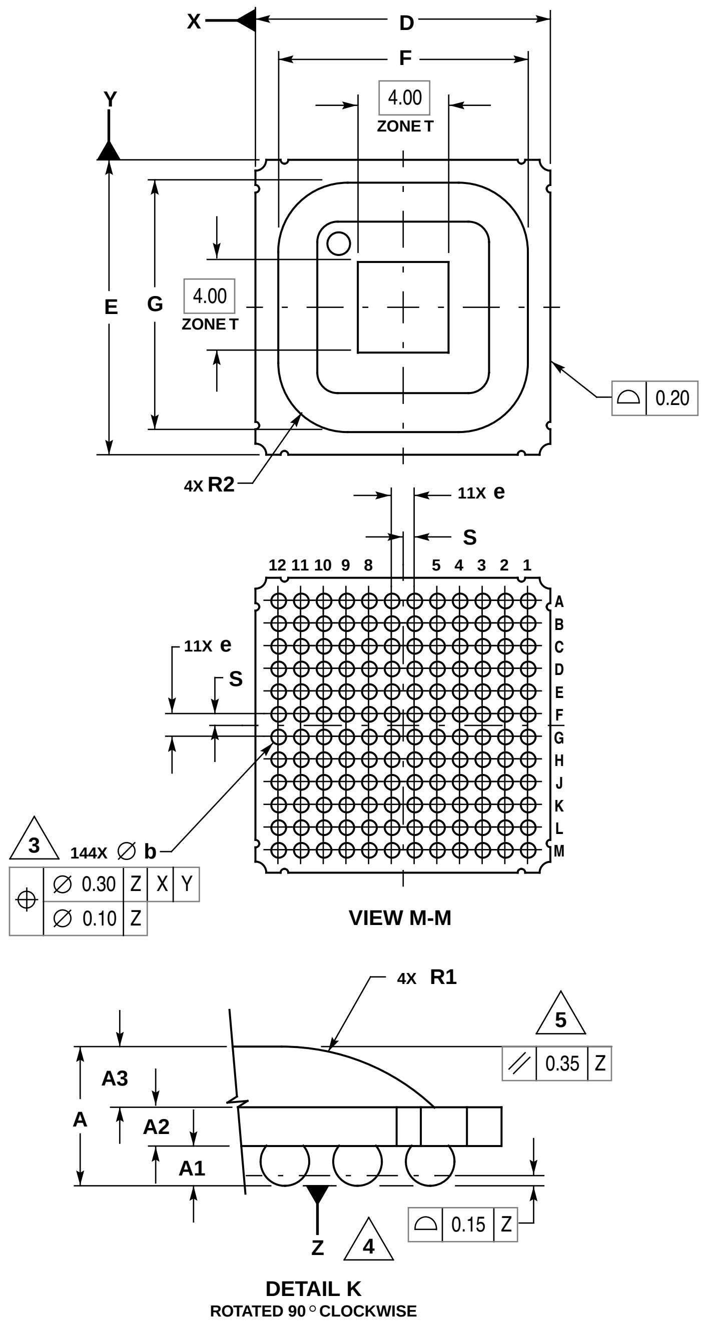
Table 3-5 DSP56602 PBGA Signal Identification by Name (Continued)

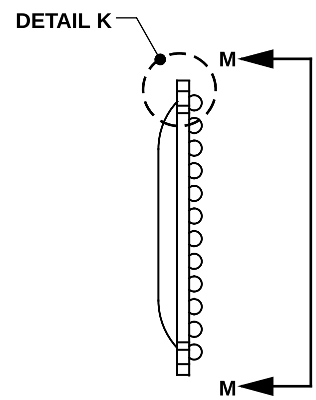
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
NC	D6	$\overline{PINIT}$	D2	TMS	A2
NC	D7	$\overline{RD}$	M10	$\overline{TRST}$	C3
NC	D8	$\overline{RESET}$	L7	V_{CCA}	G10
NC	E4	SC00	E3	V_{CCA}	J9
NC	E9	SC01	C1	V_{CCC}	K8
NC	F4	SC02	C2	V_{CCD}	D10
NC	F6	SC10	F1	V_{CCD}	E5
NC	F7	SC11	A1	V_{CCD}	E8
NC	F9	SC12	B3	V_{CCH}	J4
NC	G4	SCK0	G2	V_{CCP}	K5
NC	G6	SCK1	J1	V_{CCQH}	E11
NC	G7	SRD0	E1	V_{CCQH}	G3
NC	G9	SRD1	B2	V_{CCQH}	K7
NC	H4	STD0	E2	V_{CCQL}	E7
NC	H9	STD1	B1	V_{CCQL}	F3
NC	J5	TCK	A3	V_{CCQL}	G8
NC	J6	TDI	B4	V_{CCQL}	H7
NC	J7	TDO	C4	V_{CCS}	F5
NC	J8	TIO0	M1	$\overline{WR}$	K10
$\overline{NMI}$	D2	TIO1	J3	XTAL	M8
$\overline{PCAP}$	L6	TIO2	H3		

Table 3-6 DSP56602 PBGA Power Supply Pins

Name	Pin #	Functional Group	Name	Pin #	Functional Group
V_{CCA}	G10	Core/Port A Address	GND_A	F8	Ground—Core/Port A Address
V_{CCA}	J9		GND_A	H8	
V_{CCC}	K8	Core/Port A Control	GND_A	H10	
V_{CCD}	D10	Core/Port A Data	GND_A	J10	
V_{CCD}	E5		GND_D	C6	Ground—Core/Port A Data
V_{CCD}	E8		GND_D	D9	
V_{CCH}	J4	Peripherals/HI08 Data	GND_D	K9	
V_{CCP}	K5	Core/PLL	GND_H	K4	Ground—Peripherals/HI08 Data
V_{CCQH}	E11	Quiet V_{CC} High	GND_P	K6	Ground—Core/PLL
V_{CCQH}	G3		GND_Q	E6	Ground—Quiet
V_{CCQH}	K7		GND_Q	F10	
V_{CCQL}	E7	Quiet V_{CC} Low	GND_Q	H6	
V_{CCQL}	F3		GND_S	G5	Ground—Peripherals/SSI0, SSI1, Timer, GPIO, HI08 Control
V_{CCQL}	G8		GND_S	H5	
V_{CCQL}	H7				
V_{CCS}	F5	Peripherals/SSI0, SSI1, Timer, GPIO, HI08 Control			

PBGA Package Mechanical Drawing





	MILLIMETERS	
DIM	MIN	MAX
A	1.32	1.75
A1	0.27	0.47
A2	0.36 REF	
A3	0.70	1.00
b	0.35	0.65
D	13.00 BSC	
E	13.00 BSC	
e	1.00 BSC	
F	9.00	13.00
G	9.00	13.00
R1	2.50 REF	
R2	0.40	2.50
S	0.50 BSC	

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM REQUIREMENT APPLIES TO ZONE T ONLY. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF LASER MARK ON TOP SURFACE OF PACKAGE.

CASE 1210-02 ISSUE A

Figure 3-6 DSP56602 Mechanical Information, 144-pin PBGA Package

ORDERING DRAWINGS

Complete mechanical information regarding DSP56602 packaging is available by facsimile through Motorola's Mfax™ system. Call the following number to obtain information by facsimile:

(602) 244-6609

The Mfax automated system requests the following information:

- The receiving facsimile telephone number including area code or country code
- The caller's Personal Identification Number (PIN)

Note: For first time callers, the system provides instructions for setting up a PIN, which requires entry of a name and telephone number.

- The type of information requested:
  - Instructions for using the system
  - A literature order form
  - Specific part technical information or data sheets
  - Other information described by the system messages

A total of three documents may be ordered per call.

The DSP56602 144-pin TQFP package mechanical drawing is referenced as 918-03. The reference number for the 144-pin PBGA package is 1210-02.

SECTION 4

DESIGN CONSIDERATIONS

THERMAL DESIGN CONSIDERATIONS

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature ˚C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance ˚C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance ˚C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance ˚C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from

$R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.
- Use the value obtained by the equation $(T_J - T_T)/P_D$ where T_T is the temperature of the package case determined by a thermocouple.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual. Hence, the new thermal metric, Thermal Characterization Parameter, or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

Note: **Table 2-3 Package Thermal Characteristics** on page 2-2 contains the package thermal values for this chip.

ELECTRICAL DESIGN CONSIDERATIONS

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

Use the following list of considerations to assure correct DSP operation:

- Each V_{CC} pin on the DSP56602 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground.
- The power supply pins drive distinct groups of logic on-chip as shown in **Table 1-2 Power Inputs** on page 1-3 and **Table 1-3 Grounds** on page 1-4. For best results, separate V_{CC} and GND for each supply is recommended; each with a capacitor to bypass V_{CC} to GND as close as possible to the package. Otherwise, a multi-layer board is recommended, employing two inner layers as V_{CC} and GND planes.
- Two 0.1 μF ceramic capacitors as close as possible to each side of the package (eight capacitors altogether) should be used to bypass the V_{CC} power supply layer to the ground layer. In such cases, there is no separation between the various power and ground supplies, since each one is directly tied to the appropriate plane. Therefore, the capacitors are common to all the V_{CC}/GND pairs.
- The V_{CC}/GND supplies of the PLL should be well-regulated (non-switching regulators), and the pins should be provided with an extremely low impedance path to V_{CC}/GND.
- V_{CCP} should be connected to the main power supply with a special power branch. If required, filtering circuitry should be provided. If V_{CCP} and GND_P are kept separate from the other supplies, an additional larger capacitor (e.g., 47 μF) should be used between these pins.
- An additional large capacitor should be placed next to the power supply itself.

- Because all output pins on the DSP56602 have fast rise and fall times, PCB trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses, as well as to the Port A control signals and Port B pins. Maximum PCB trace lengths on the order of 6 inches (15.24 cm) are recommended.
- Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PCB traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the V_{CC} and GND circuits.
- Drive to a valid value (e.g., connect to pull-up or pull-down resistors) all unused inputs or signals that will be inputs during reset ($\overline{\text{RESET}}$ asserted).
- Every input pin should be driven to a valid value after the $\overline{\text{RESET}}$ deassertion by connecting it to a pull-up or pull-down resistor if not used. Exceptions to this are the $\overline{\text{TRST}}$, $\overline{\text{DE}}$, and TMS pins, which have internal pull-up resistors.
- The $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$ pins must be asserted low after power-up.
- All this data relates to a single DSP56602. If multiple DSP56602 devices are on the same board, check for cross-talk or excessive spikes on the supplies caused by synchronous operation of the devices.

POWER CONSUMPTION CONSIDERATIONS

Power dissipation is a key issue in portable DSP applications. This section describes some of the factors that affect current consumption. Most of the current consumed by CMOS devices is Alternating Current (AC), which is charging and discharging the capacitances of the pins and internal nodes. Therefore, the total current consumption is the sum of these internal and external currents.

This current consumption is described by the formula:

Equation 3: $I = C \times V \times f$

where: C = node/pin capacitance (in Farads)
V = voltage swing (in volts)
f = frequency of node/pin toggle (in Hz)

Example 4-1 Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 2.7 V, and with a 60 MHz clock, toggling at its maximum possible rate of 15 MHz, the current consumption is (for this pin only):

Equation 4: $$I = 50 \times 10^{-12} \times 2.7 \times 15 \times 10^{6} = 2.025 \text{ mA}$$

The Typical Internal Current value (I_{CCI}) reflects the typical switching of the internal buses in a typical DSP-intensive application.

For applications requiring very low current consumption, it is recommended to:

- Set the PCD bit (in the OMR) and do not use the PC-relative instructions.
- Set the EBD bit (in the OMR) when not accessing external memory
- Minimize external memory accesses and use internal memory accesses instead
- Minimize the number of pins that are switching
- Minimize the capacitive load on the pins
- Connect the unused inputs to pull-up or pull-down resistors.
- Disable unused peripherals
- Disable unused pin activity (e.g., CLKOUT, XTAL)

A common way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (i.e., to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm and measure the current consumption at two different frequencies, F1 and F2. Then use the following equation to derive the current per MIPS value:

Equation 5: $$I/MIPS = I/MHz = (I_{typF2} - I_{typF1})/(F2 - F1)$$

where: I_{typF2} = current at F2
I_{typF1} = current at F1
F2 = high frequency (any specified operating frequency)
F1 = low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 60 MHz and F1 could be 30 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

PLL PERFORMANCE ISSUES

The following explanations are provided as general observations on expected PLL behavior. Measurements are preliminary and are subject to change.

Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. For input frequencies greater than 15 MHz and MF ≤ 4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between –1.4 ns and +3.2 ns.

Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF ≤ 4, this jitter is less than ±0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than ±2 ns.

FREQUENCY JITTER PERFORMANCE

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5%. For mid-range MF (10 < MF < 500) this jitter is between 0.5% and approximately 2%. For large MF (MF > 500), the frequency jitter is 2–3%.

INPUT (EXTAL) JITTER REQUIREMENTS

The allowed jitter on the frequency of EXTAL is 0.5%. If the rate of change of the frequency of EXTAL is slow (i.e., it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (i.e., it does not stay at an extreme value for a long time) then the allowed jitter can be 2%. The phase and frequency jitter performance results are only valid if the input jitter is less than the prescribed values.

SECTION 5

ORDERING INFORMATION

Table 5-1 lists the pertinent information needed to place an order. Consult a Motorola Semiconductor sales office or authorized distributor to determine availability and to order parts.

Table 5-1 DSP56602 Ordering Information

Part	Supply Voltage	Package Type	Pin Count	Frequency (MHz)	Order Number
DSP56602	3.0	Plastic Thin Quad Flat Pack (TQFP)	144	60	XC56602PV60*
DSP56602	3.0	Plastic Ball Grid Array (PBGA)	144	60	XC56602GC60*

Note: * The DSP56602 includes a customer-specified factory-programmed ROM. For additional information on future part development, or to request specific ROM-based support, call your local Motorola Semiconductor sales office or authorized distributor

Preliminary

APPENDIX A

POWER CONSUMPTION BENCHMARK

The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL. Then it disables the XTAL generation, external CLKOUT generation, external port, and PC-relative instructions. Finally, it uses repeated Multiplier-Accumulator (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

This synthetic benchmark provides a structure and performance that is similar to a typical DSP-intensive algorithm, as used in the target cellular subscriber market. A typical target application consumes approximately 90% of the current used by this benchmark program.

The two listed equate files, ioequ.asm and intequ.asm, are available in print format in **Appendix B** of the *DSP56602 User's Manual (DSP56602UM/AD)* as well as electronically via the Internet on the Motorola DSP home page. The web page address is provided on the back page of this document.

```
INT_PROG   equu    $0                      ; Internal program memory
                                           ; starting address
INT_XDAT   equ     $0                      ; Internal X-data memory
                                           ; starting address
INT_YDAT   equ     $0                      ; INTERNAL Y-data memory

           INCLUDE "ioequ.asm"
           INCLUDE "intequ.asm"

           list

           org       P:INT_PROG

           movep     #$d0,x:M_PCTL1        ; XTAL disable
                                           ; PLL enable
                                           ; CLKOUT disable
           ori       #$10,omr              ; set EBD
           ori       #$20,omr              ; set PCD

PROG_START
           move      #$0,r0
           move      #$0,r4
           move      #$3f,m0
           move      #$3f,m4

           clr       a
           clr       b
           move      #$0,x0
```

Preliminary

```
            move      #$0,x1
            move      #$0,y0
            move      #$0,y1

            do        forever, _end       ; Main Loop

            mac       x0,y0,a    x:(r0)+,x1   y:(r4)+,y1
            mac       x1,y1,a    x:(r0)+,x0   y:(r4)+,y0
            add       a,b
            mac       x0,y0,a    x:(r0)+,x1
            mac       x1,y1,a    y:(r4)+,y0
            move      b1,x:$ff
_end
            nop
            nop

            org       x:XDAT_START
            dc        $2EB9
            dc        $F2FE
            dc        $6A5F
            dc        $6CAC
            dc        $FD75
            dc        $10A
            dc        $6D7B
            dc        $A798
            dc        $FBF1
            dc        $63D6
            dc        $6657
            dc        $A544
            dc        $662D
            dc        $E762
            dc        $F0F3
            dc        $F1B0
            dc        $829
            dc        $F7AE
            dc        $A94F
            dc        $78DC
            dc        $2DE5
            dc        $E0BA
            dc        $AB6B
            dc        $26C8
            dc        $361
            dc        $6E86
            dc        $7347
            dc        $E774
            dc        $349D
            dc        $ED12
            dc        $FCE3
            dc        $26E0
            dc        $7D99
            dc        $A85E
            dc        $A43F
            dc        $B10C
```

```
dc      $A55
dc      $EC6A
dc      $255B
dc      $F1F8
dc      $26D1
dc      $6536
dc      $BC37
dc      $35A4
dc      $F0D
dc      $BEC2
dc      $E4D3
dc      $E810
dc      $F09
dc      $E50E
dc      $FB2F
dc      $753C
dc      $62C5
dc      $641A
dc      $3B4B
dc      $A928
dc      $6641
dc      $A7E6
dc      $2127
dc      $2FD4
dc      $57D
dc      $3C72
dc      $8C3
dc      $7540

org     y:YDAT_START
dc      $6DA
dc      $F70B
dc      $39E8
dc      $E801
dc      $66A6
dc      $F8E7
dc      $EC94
dc      $233D
dc      $2732
dc      $3C83
dc      $3E00
dc      $B639
dc      $A47E
dc      $FDDF
dc      $A2C
dc      $7CF5
dc      $6A8A
dc      $B8FB
dc      $ED18
dc      $F371
dc      $A556
dc      $E9D7
dc      $A2C4
```

```
        dc      $35AD
        dc      $E0E2
        dc      $2C73
        dc      $2730
        dc      $7FA9
        dc      $292E
        dc      $3CCF
        dc      $A65C
        dc      $6D65
        dc      $A3A
        dc      $B6EB
        dc      $AC48
        dc      $7AE1
        dc      $3006
        dc      $F6C7
        dc      $64F4
        dc      $E41D
        dc      $2692
        dc      $3863
        dc      $BC60
        dc      $A519
        dc      $39DE
        dc      $F7BF
        dc      $3E8C
        dc      $79D5
        dc      $F5EA
        dc      $30DB
        dc      $B778
        dc      $FE51
        dc      $A6B6
        dc      $FFB7
        dc      $F324
        dc      $2E8D
        dc      $7842
        dc      $E053
        dc      $FD90
        dc      $2689
        dc      $B68E
        dc      $2EAF
        dc      $62BC
        dc      $A245
                                        ; End of program
```

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